Dynamic Characterization of a-Si TFT-LCD Pixels

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ABSTRACT

A dynamic analysis of an amorphous silicon (a-Si) Thin-Film-Transistor-Liquid-Crystal-Display (TFT-LCD) pixel is presented using new a-Si TFT model and new Liquid Crystal (LC) capacitance models for SPICE simulators. This analysis is useful to all Active Matrix LCD designers for evaluating and predicting the performance of LCD's. The a-Si TFT model is developed to simulate important a-Si TFT characteristics such as off-leakage current, threshold voltage shift due to voltage stress and temperature, localized states behavior, and bias- and frequency-dependent gate-to-source and gate-to-drain capacitance. In addition, the LC Capacitance model is developed using simplified empirical equations. The modeling procedure is useful to TFT and LCD designers who need to develop their own models. Since our experiments simulate critical TFT-LCD transient effects, such as the voltage drop due to gate-to-source capacitance and dynamic off-leakage current, it is possible to accurately characterize TFT-LCD's in the time domain. The analysis and models are applicable to today's optical characterizations of Flat-Panel-Displays (FPD's).

I. INTRODUCTION

A-Si TFT's are widely used for active matrix liquid-crystal displays. This has led to increasing demand for models that can predict TFT-LCD dynamic behavior with optical characteristics. Accurate a-Si TFT and Liquid Crystal Capacitance models are required for the characterization of TFT-LCD dynamic behavior. This paper presents the experimental results of our TFT-LCD transient analysis and the modeling method for the analysis.

Several papers have already been published regarding the physics [1] and the models [2], [3] of a-Si TFT's. Those authors analyzed and solved the distribution of the localized states [1]-[3], which is divided into two exponential regions for the tail states and the deep states. Khakzar et al. [3] also included the temperature dependency of the current-voltage characteristics. Although those models [2], [3] are well analyzed, they are insufficient for today's advanced LCD simulations, because they do not account for the following characteristics:

- The insulator film capacitance must be calculated from the real dielectric constants of the two layer insulating film in order to keep the mobility consistent with the process parameter.
- The off-leakage current, which affects the sub-threshold-to-off region, must be incorporated in order to simulate the off-screen noise of LCD's.
- The threshold voltage of a-Si TFT's changes with voltage stress and device temperature [4] and must be taken into account.
- The frequency-dependence of the gate-to-source and gate-to-drain capacitances must be taken into account in order to characterize LCD performance.

Because the characteristics of a-Si TFT's vary widely according to the device process, the model needs to be flexible enough to represent different types of a-Si TFT devices. This paper presents an a-Si TFT model which focuses mainly on the inverted staggered type a-Si device structure. The model parameters were extracted from measured data using parameter extraction software developed with the model.

This paper also presents a liquid crystal capacitance model. The liquid crystal capacitance is critical in the simulation of LCD pixels and is voltage-dependent due to the crystal characteristic. Because there are several types of liquid crystal materials and shapes, the liquid crystal model is developed using empirical equations.

As an application example, transient measurement and simulations of a TFT-LCD pixel are shown in this paper. To predict the driving waveform of the LCD, the gate-to-source capacitance effect must be reproduced. This effect has been observed in the simulated results. A few examples of optical characteristics are also described.

Sections II and III describe the equation formulation of the a-Si TFT and Liquid Crystal Capacitance models. In Section IV, some experimental simulation results for a TFT-LCD pixel are presented. Conclusions are summarized in Section V.

II. AN A-SI TFT MODEL

In order to maximize the speed and insure convergence of the TFT-LCD pixel simulations, the model equations were formulated to be as simple as possible without sacrificing accuracy. The model focuses primarily on the following a-Si TFT characteristics as discussed in [5]:

- Because of localized states, TFT's require a higher gate turn-on voltage than MOSFET's.
- Due to photoconductivity and channel leakage current flowing from gate-to-source and drain-to-source, the sub-threshold behavior is different from a MOSFET.

- The threshold voltage varies with the temperature and duration of the voltage applied to the gate (voltage stress).
- Some TFT's have the insulator film that consists of two layers of different materials.
- The gate-to-source and gate-to-drain capacitances are bias- and frequency-dependent.

The current-voltage and capacitance-voltage characteristics of a-Si TFT's strongly depend on the density and distribution of localized states in the energy gap. The position of the carrier Fermi level in an a-Si channel may vary from levels close to the bottom of the conduction band to energies near the top of the valence band depending on the sign and magnitude of the gate voltage [1]. The density of this charge is determined by the density of the localized *tail* states and by the position of the carrier Fermi level. The total density N_{loc} of the localized charge [1] is approximated by

$$N_{loc} = N_{deep} + N_{tail} \ . \tag{1}$$

The localized states charge [1], [2] is calculated by

$$Q_{loc} = q \int_0^{\infty} N_{loc} dx = \sqrt{2\varepsilon q \int_0^{V_0} \left[N_{deep}(V) + N_{tail}(V) \right] dV} \tag{2}$$

where q is the electron charge, x is the vertical distance of the TFT device structure, V_0 is the surface band bending, and ε is the dielectric permittivity of amorphous silicon. A simplified structure of the inverted-stagger type a-Si TFT's is shown in Fig. 1. When V_G and V_D are supplied at each terminal respectively, the conducting channel is produced in the a-Si layer.

The resulting electron concentration causes an accumulation area to expand under the source and drain. The total channel charge is very small and is negligible compared to the surface states charge and localized states charge. The dominant charge in the semiconductor channel are mobile and localized charges. The drain current derivation of a-Si TFT is started with linear region.

A. Current-Voltage Characteristics

Because of the long channel device condition, *dV/dx* is much greater than *dV/dy*,

$$\frac{dV}{dx} \gg \frac{dV}{dy} \ . \tag{3}$$

The gate charge (Q_g) equals the negative sum of mobile charge (Q_m), surface state charge (Q_{ss}), and localized charge (Q_{loc})

$$Q_g = -Q_m - Q_{ss} - Q_{loc} = C_{fm}\left(V_g - V_s - \phi\right) \ . \tag{4}$$

Current density is given by (5)

$$J_n = -q\left(\mu_n n + \mu_p p\right)\frac{d\phi}{dy} \tag{5}$$

where ϕ is the potential and μ_n and μ_p are the effective mobilities of the electrons and holes, respectively.

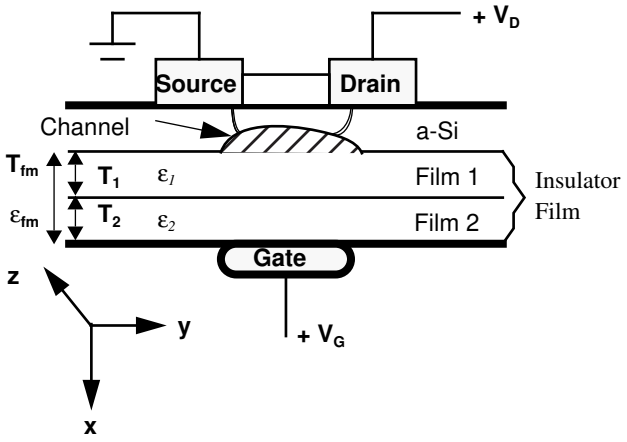


Fig. 1. A simplified inverted-stagger type a-Si TFT structure. Here T_{fm} is the total film thickness and ε_{fm} is the dielectric constant of the insulated film. Also, T_1, T_2, ε_1, and ε_2 are the film thickness and dielectric constants of Film1 and Film2, respectively.

The total current of the drain-to-source is solved by

$$I_{DS} = \iint J_n \cdot dxdz = -Z \cdot \frac{d\phi}{dy} \cdot \mu_{eff} \cdot Q_m \tag{6}$$

$$I_{DS} \int_0^L dy = -W \int_0^{V_D} \left(\mu_{eff} \cdot Q_m\right) d\phi \ . \tag{7}$$

Here, Z is replaced with W (channel width) in (7), μ_{eff} is the field effect mobility and L is the channel length. Substituting (4) into (7) and integrating with respect to V from 0 to V_D, we obtain

$$I_{DS} = \frac{W}{L} \cdot \mu_{eff} \left\{ C_{fm} \left[\left(V_{GS} - V_{TO}\right) V_{DS} - \frac{{V_{DS}}^2}{2} \right] + Q_{loc} \cdot V_{DS} \right\} . \tag{8}$$

where V_{TO} is a threshold voltage without localized states charge, which is extracted from the measured I_D versus V_G curve at low

V_D (e.g. 50 mV). The field effect mobility (μ_{eff}) is a function of gate bias and is given by

$$\mu_{eff} = \frac{\mu_O}{1.0 - q \cdot \left(V_{GS} - V_{TH}\right)} \tag{9}$$

where μ_o is the band mobility and θ is the mobility reduction. Because the expansion of Q_{loc} (2) includes a large number of logarithms and exponents, an approximation is used to decrease computation time. For the surface band bending in Fig. 2, it is necessary to charge and discharge any localized states around the Fermi level. Larger numbers of localized states make it more difficult to bend the energy band and the threshold voltage increases. Using some device measurements, it can be shown that the threshold voltage increases in proportion to drain voltage, as shown in (10). In our threshold analysis, we found that the localized charge could be included in the threshold voltage as shown in (11).

$$V_{TH} = V_{TO} + \eta \cdot V_{DS} \tag{10}$$

where η is a fitting parameter to express static feedback effect

$$Q_{loc} = C_{fm} \cdot V_{DS} \cdot \eta \quad . \tag{11}$$

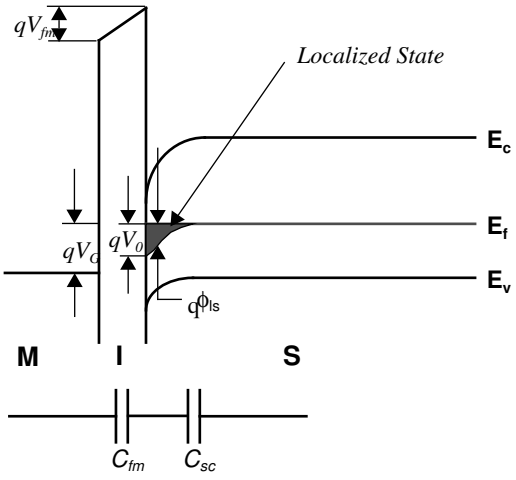


Fig. 2. Energy band diagram of a-Si TFT and its equivalent circuit.

The final drain current equation for the linear region is

$$I_{DS} = \frac{W}{L} \cdot \mu_{eff} \cdot C_{fm} \left[\left(V_{GS} - V_{TO} - \eta \cdot V_{DS} \right) \; V_{DS} - \frac{{V_{DS}}^2}{2.0} \right]. \tag{12}$$

As shown in Fig. 1, a typical a-Si insulated thin film consists of two layers of different types of materials [8], T_1 and T_2. The capacitance and the electrical constants are calculated in a traditional manner as shown in

$$C_{fm} = \frac{\varepsilon_0 \cdot \varepsilon_1 \cdot \varepsilon_2}{T_2 \cdot \varepsilon_1 + T_1 \cdot \varepsilon_2} \tag{13}$$

$$\varepsilon_{fm} = C_{fm} \cdot T_{fm} \tag{14}$$

where ε_o is the permittivity of a vacuum.

Due to traps, carriers reach maximum velocity slowly in the region beyond pinchoff. The electrons are not traveling at a saturation velocity in an amorphous silicon TFT. The saturated velocity (v_{sat}) was defined to represent the drain saturation voltage. The derivation of the drain current equation is similar to the UCB MOS level 3 model[7]. The drain current for the saturation region becomes

$$I_{DS}^{sat} = I_{DS} \cdot \frac{v_{sat} \cdot L}{\left(1.0 + V_{DS}\right) \mu_{eff}} \quad . \tag{15}$$

Temperature effects are critical for accurate a-Si TFT modeling. For example, μ_{eff} and V_{TH} are functions of temperature. Since the physical theory is not fully understood, empirical equations are used in the model to represent those temperature effects. Field effect mobility (μ_{eff}) has a simple temperature effect

$$\mu_{eff}^{TEMP} = \mu_{eff} \cdot \left(\frac{T_{DEV}}{T_{NOM}} \right)^{T_{REF}} \tag{16}$$

where T_{NOM} is the room temperature that is defined in the model, T_{DEV} is the device temperature available in SPICE simulation, and T_{REF} is a fitting parameter.

One of the most important properties of a-Si TFT's is the threshold instability which is generally considered the result of the insertion of electrons into the S_iN_x of gate insulated films or MOS interfaces [4], [6]. We analyzed the temperature characteristic of the threshold voltage using Ibaraki, et al. [6] and our measured data (Fig. 3). An inverted staggered a-Si: H-TFT with a SiNx gate insulator film was used for the measurement. The dc bias stress was supplied at TFT gate and drain terminals. Our measured data and Ibaraki, et al. [6] show that threshold voltage (V_{TH}^{eff}) is a function of $V_{GS,}$ $V_{DS,}$ voltage supplying time (t_{vst}), and T_{DEV}. A simple partial differential equation is obtained as

$$\frac{\partial V_{THD}}{\partial t_{log}} = - \frac{q \cdot V_x}{k \cdot T_{DEV}} \cdot V_{THD} \quad , \tag{17}$$

with

$$V_{THD} = V_{TH}^{eff} - V_{TH} \quad \texttt{and} \quad t_{\log} = \log\left(t_{vst}\right) \tag{18}$$

where k is the Boltzmann constant and V_x is a fitting parameter.

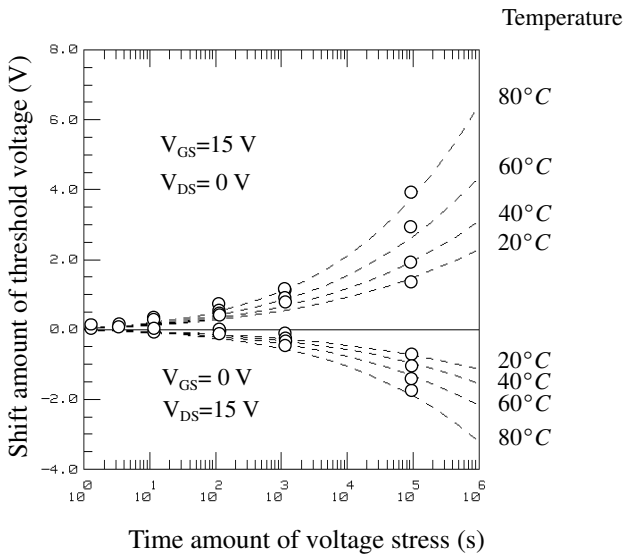


Fig. 3. Threshold voltage shift measurement and simulation with voltage stress and temperature. Here the step variable is temperature. The circle indicates measured data of an a-Si:H TFT device described in Section IV.

As an initial condition,

$$V_{THD} = f\left(V_{GS}, V_{DS}\right) \quad \texttt{for} \quad t_{\log} = 0 \tag{19}$$

the $f\left(V_{GS}, V_{DS}\right)$ is empirically approximated by

$$f\left(V_{GS}, V_{DS}\right) = V_{THD}\Big|_{t_{vst}=1} = \nu \cdot \left(V_{GS}{}^{\psi} - \frac{V_{DS}{}^{\psi}}{2}\right). \tag{20}$$

After solving (17) with (18), (19), and (20), V_{TH}^{eff} is given by

$$V_{TH}^{eff} = V_{TH} + \nu \cdot \left(V_{GS}{}^{\psi} - \frac{V_{DS}{}^{\psi}}{2.0}\right) \cdot exp\left[-\frac{q \cdot V_x}{k \cdot T_{DEV}} \cdot log\left(t_{vst}\right)\right] \tag{21}$$

where ν is the first order temperature gradient and ψ is an empirical parameter. Every parameter used in the simulation shown in Fig. 3 is directly extracted from the measured data (Table 1). Since the measurement was performed under dc bias condition, the analysis and associated equations (17)-(21) account for steady state stressing. In a TFT-LCD the TFT gate is pulsed with very low duty cycles (0.01% ~ 1%), which will change an a-Si TFT behavior.

Table 1. Extracted (a) a-Si TFT and (b) LC Capacitor Model Parameters

(a)	(b)
L = 11 μm	L = 152 μm
W = 41 μm	W = 148 μm
μ_O = 0.450 cm^2/Vs	D = 10.02 μm
V_{TO} = 1.699 V	δ = 51.0 mm^2/s
ϕ = 0.620 V	γ = 51.2 ms/mm^2
N_{FS} = 1.925x10^{21} cm^{-2}	D_{TIME} = 100 ms
V_{sat} = 2,783 m/s	V_C = 1.887 V
θ = 17.8 mV^{-1}	ε_{PL} = 3.1
η = 410.8μ	
T_1 = 300 nm	
T_2 = 0	
ε_1 = 3.9	
ε_2 = 0	
g_o = 9.728x10^{-15} Ω^{-1}	
T_{REF} = 1.5	
C_{GSO} = 52.03 fF	
C_{GDO} = 42.21 fF	
C_{SC} = 158.8 μF/m	
R_D = 8,030 Ω	
R_S = 8,030 Ω	
f = 100 KHz	
D_{EFF} = 1.968	
τ = 10.7 ns	
f_{EFF} = 0.302	
ν = 0.008	
ψ = 0.2	
V_x = 0.033 V	
t_{vst} = 100 ms	
T_{NOM} = 300.15 K	

In the sub-threshold region, when the Fermi level at the interface exists in the energy range corresponding to the *deep* states, the drain current rises exponentially with gate voltage. Unlike MOSFET devices, the sub-threshold current characteristic is affected by the amount of interfacial traps and the bulk states throughout the a-Si film. The more interfacial traps, the more gentle the slope of the sub-threshold current curve. This leads to discontinuity in the transition region from sub-threshold to linear. In order to avoid this phenomenon, another threshold voltage, v_{on}, is defined. The sub-threshold equation is given in (22).

$$I_{DS}^{subth} = I_{DS} \cdot exp\left(\frac{V_{GS} - V_{TH}^{eff}}{xn \cdot vt} + 1.0\right),$$

where

$$v_{on} = V_{TH}^{eff} + \eta \cdot V_{DS} + xn \cdot vt \tag{22}$$

$$xn = 1.0 + \frac{q \cdot N_{FS} \cdot L \cdot W}{C_{fm}} \tag{23}$$

where N_{FS} is the effective fast surface state density which is affected by the bulk states and the deep states.

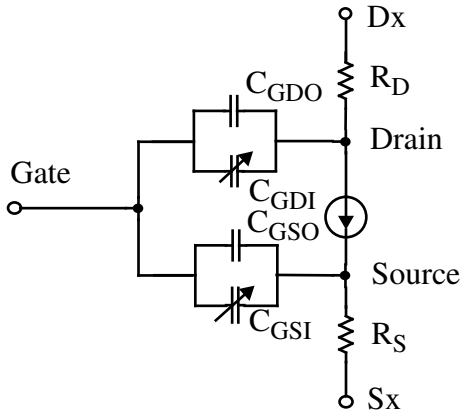


Fig. 4. Equivalent circuit of an a-Si TFT.

The off-leakage current affects the sub-threshold to off-region current characteristics. The drain leakage current linearly increases in proportion to the gate and drain voltages, which is represented by

$$I_{DS}^{off} = I_{DS}^{subth} + g_o \cdot \left(V_{GS} + D_{eff} \cdot V_{DS}\right) \tag{24}$$

where g_o is the conductance and D_{eff} is the coefficient of drain leakage which depends on the a-Si TFT process.

B. Capacitance-Voltage-Frequency Characteristics

As shown in Fig. 4, the equivalent circuit of an a-Si TFT is very simple. C_{GS} and C_{GD} are divided into overlap capacitance (C_{GSO}, C_{GDO}) and insulated film and intrinsic a-Si capacitance (MIS capacitance). The dielectric constants of the MIS capacitance (C_{GSI}, C_{GDI}) are bias- and frequency-dependent. The MIS capacitance (C_{MIS}) is calculated as shown in (25) [9]

$$C_{MIS}(V) = \frac{\partial Q_{SC}}{\partial V_G} = \frac{\partial Q_{SC}}{\partial\left(V_{fm} + \phi_{ls}\right)} \tag{25}$$

where Q_{SC} is the space charge, ϕ_{ls} is the surface potential at a certain gate voltage, and V_{fm} is the potential drop across the insulated thin film. From the equivalent circuit in Fig. 2, C_{MIS} in (25) is rewritten as shown in

$$C_{MIS}(V) = \frac{C_{fm} \cdot C_{SC}}{C_{SC} + C_{fm}}\ . \tag{26}$$

Here C_{SC} is the maximum space charge capacitance.

From Fig. 4, the gate-to-source and gate-to-drain capacitance are directly given by

$$C_{GS} = C_{GSO} + C_{GSI} \tag{27}$$

$$C_{GD} = C_{GDO} + C_{GDI}\ . \tag{28}$$

Using Meyer's modeling approach [10], C_{GSI} and C_{GDI} are written as

$$C_{GSI} = \left.\frac{\partial Q_G}{\partial V_S}\right|_{V_D = Const} = -\frac{\partial\left(Q_m + Q_{ss} + Q_{loc}\right)}{\partial V_S} \tag{29}$$

and

$$C_{GDI} = \left.\frac{\partial Q_G}{\partial V_D}\right|_{V_S = Const} = -\frac{\partial\left(Q_m + Q_{ss} + Q_{loc}\right)}{\partial V_D} \tag{30}$$

for $V_{GS} \geq V_{TH}$.

C_{GSI} and C_{GDI} in the linear region are calculated using (26), (29), and (30) as follows:

$$C_{GSI} = C_{MIS} \cdot \left[1.0 - \frac{V_{DS}^2}{12.0 \cdot \left(2.0V_{GS} - 2.0V^{eff}{}_{TH} - V_{DS}\right)^2}\right] \tag{31}$$

$$C_{GSI} = C_{MIS} \cdot \left[0.5 - \frac{2.0 \cdot V_{DS}\left(2.0V_{GS} - 2.0V^{eff}{}_{TH} - V_{DS}\right) + V_{DS}^2}{6.0 \cdot \left(2.0V_{GS} - 2.0V^{eff}{}_{TH} - V_{DS}\right)^2}\right] \tag{32}$$

Below the threshold voltage,

$$C_{GSI} = C_{GDI} = 0.0 \,. \tag{33}$$

However, the simulated result using (31), (32), and (33) has a discontinuity in the transition region around the threshold voltage. Also, the capacitance value in the region is dominant for TFT-LCD transient simulations. Therefore, the model equations are modified by using exponential functions, which are

$$C_{GSI} = C_{MIS} \cdot \exp\left[-A \cdot \left(V_{GS} - V_{TH}^{eff}\right)\right]^{-1} \tag{34}$$

and

$$C_{GDI} = C_{MIS} \cdot \exp\left[-A \cdot \left(V_{GS} - V_{TH}^{eff} - V_{DS}\right)\right]^{-1} \tag{35}$$

for $V_{DSAT} > V_{DS}$, where A is a capacitance slope in the transition region.

The measured capacitance depends also on the frequency of the supplied gate signal both because of the thermal release time of the states, which is their response time to the change in potential, and because of the high-resistivity material, which requires the intrinsic resistance of the a-Si TFT to be taken into account. However, such effects are not as critical as bias voltage effects. Because the SPICE simulator used does not support frequency-dependent capacitance, frequency is treated as a model parameter for transient analysis. The frequency effect is implemented by using the dielectric constant of amorphous silicon as follows [11].

$$\varepsilon_f = \varepsilon_{fmac} + \left[\frac{\varepsilon_{fm} - \varepsilon_{fmac}}{1.0 + \left(2.0 \cdot \pi \cdot f \cdot \tau\right)^2}\right] \tag{36}$$

where ε_{fm} is the nominal dielectric constant of a-Si, ε_{fmac} is the dielectric constant at the highest frequency, f is the signal frequency, and τ is the relaxation time constant. (37) implies a pure capacitance unit.

$$C_{MISlw} = \frac{C_{fm} \cdot C_{SC}}{C_{SC} + C_{fm}} \cdot L \cdot W \,. \tag{37}$$

By using (34), equations (35) and (36) are modified to support frequency dependencies. Now the intrinsic capacitances are derived as follows.

For $V_{DS} < V_{DSAT,}$

$$C_{GSI} = C_{MISlw} \cdot \frac{\varepsilon_{fmac}}{\varepsilon_{fm} \cdot \exp\left[-F_{eff} \cdot \varepsilon_f \cdot \left(V_{GS} - V_{TH}^{eff}\right)\right]} \tag{38}$$

and

$$C_{GDI} = C_{MISlw} \cdot \frac{\varepsilon_{fmac}}{\varepsilon_{fm} \cdot \exp\left[-F_{eff} \cdot \varepsilon_f \cdot \left(V_{GS} - V_{TH}^{eff} - V_{DS}\right)\right]} \tag{39}$$

where F_{eff} is the frequency effect compensation of each a-Si device.

For $V_{DS} \geq V_{DSAT,}$

$$C_{GSI} = 0.5 \cdot C_{MISlw} \tag{40}$$

and

$$C_{GDI} = C_{MISlw} \,. \tag{41}$$

III. A LIQUID CRYSTAL CAPACITANCE MODEL

A simple Liquid Crystal (LC) capacitance model in combination with the a-Si TFT model is used to simulate the transient response of LCD pixels.

Because of the anisotropy of LC material, the liquid crystal capacitance (C_{lc}) is not constant. It varies from a minimum capacitance when no voltage is applied across the LC cell to a maximum capacitance when the LC cell is fully turned on [12]. Thus, the liquid crystal capacitance C_{lc} is bias- and time-dependent. This mechanism has been thoroughly analyzed by liquid crystal manufacturers and some laboratories. However, the formulation is very dependent on the specific liquid crystal type. An empirical approach is used to support various types of liquid crystal in this model.

The permittivity factor, $\varepsilon_{PS,}$ of the model is bias-dependent. The model equation is formulated based on $\varepsilon_{PL,}$ the dielectric permittivity base value. The viscosity of liquid crystals is expressed by δ. D_{TIME} is delay time at each bias step. γ is a fitting parameter used to account for the change in slope due to threshold voltage. V_C is a threshold voltage that expresses the starting value of increasing ε_{PS} as

$$\varepsilon_{PS} = \varepsilon_{PL} + \delta \cdot \gamma \cdot exp\left(D_{TIME}\right) \cdot \sqrt{\frac{V}{V_C} - 1.0} \,. \tag{42}$$

The total amount of LC capacitance (C_{lc}) is calculated from ε_{PS} and the geometry of the LC cell as

$$C_{lc} = \frac{\varepsilon_0 \cdot \varepsilon_{PS} \cdot L \cdot W}{D} \quad (43)$$

where L and W are used to calculate the total area of the LC cell which is connected to each TFT, D is the thickness of the LC cell (cell gap), and $\varepsilon_0 = 8.854 \cdot 10^{-12}$ F/m.

IV. Experiments of TFT-LCD Characterization

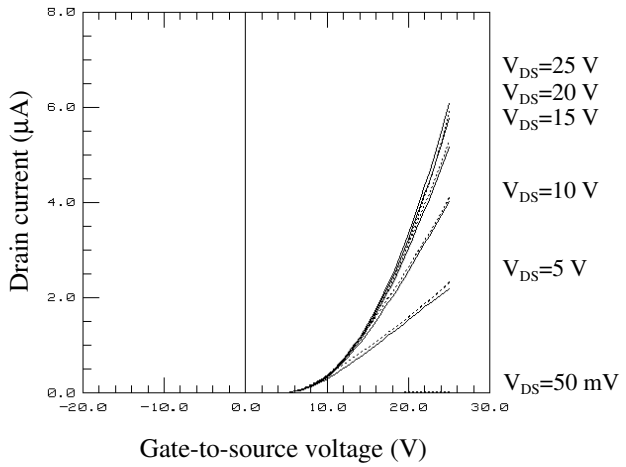
A TFT-LCD pixel measurement and simulation and some analysis have been made using the a-Si TFT and LC capacitance models. The following experiments employ a TN type LCD pixel based on a typical inverted staggered a-Si: H TFT with a SiNx gate insulator film.

A. TFT and LC Capacitance Model Measurement and Extractions

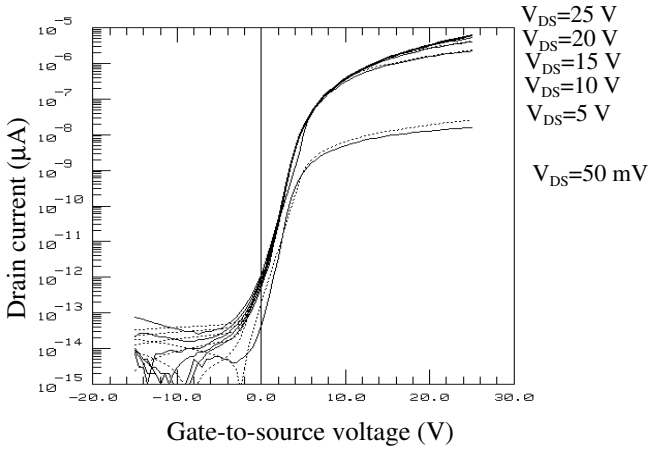
The model parameters for the a-Si: H TFT and the LC capacitance were extracted using the extraction and optimization functions of the IC-CAP software. IC-CAP is an integrated circuit and device characterization software system, which supports measurement, device and circuit modeling, model parameter extraction, and SPICE simulation. A list of extracted parameters for every simulation and geometry of both the a-Si: H TFT and the liquid crystals cell devices used in those measurements is shown in Table 1. The *dc* measurements were made using a pA Meter/Voltage Source (HP4140B) which has 1 fA current resolution. The capacitance measurements of the a-Si: H TFT and liquid crystals were made using a *C* meter (HP4284A). The extraction functions, which calculate all a-Si TFT and LC capacitance model parameters directly from measured data, were developed especially for the a-Si TFT and the LC capacitance models. The extractions took a few seconds to run.

In order to simulate TFT-LCD pixels accurately, the a-Si TFT model must be able to support most of the known TFT process devices. For time domain simulations, it is especially important that the model represent the following characteristics:

- The charging state which is driven by the on-current of an a-Si: H TFT
- The holding state which is affected by the off-current of an a-Si: H TFT
- The voltage drop characteristic which is controlled by the gate-to-source capacitance of an a-Si: H TFT and LC capacitance



(a)



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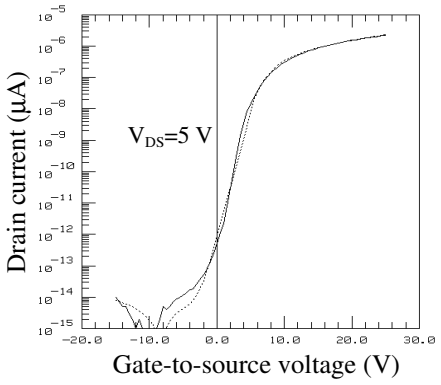

(c)

Fig. 5. Measured (—) and simulated (- - -) drain current comparison plot of a typical a-Si: H TFT in the (a) linear region, (b) sub-threshold region, and (c) sub-threshold region at V_{DS} = 5 V.

Fig. 5 (a) and 6 show the model accuracy of the on-current characteristics. Fig. 5 (b) plots I_{DS} *vs.* V_{GS} for the a-Si: H TFT on a semilogarithmic scale using the same measured and simulated data as Fig. 5 (a). The sub-threshold and off-region current characteristics are clearly shown in Fig. 5 (b). The drain bias dependency of the off-leakage current is demonstrated in this plot. One of the I_{DS} *vs.* V_{GS} curves from Fig. 5 (b) is used to check the accuracy of the model in the sub-threshold and off-region (Fig. 5 (c)). The gate bias dependency of the off-leakage current is sufficient to simulate the holding state behavior. Also, the gate-to-source capacitance of an a-Si: H TFT was characterized as shown in Fig. 7. No discontinuity is observed because the equation (38) is continuous from below to over the threshold voltage. The result of the C_{lc} extraction is plotted in Fig. 8. It shows good agreement between measured and simulated data. Fig. 7 and Fig. 8 are good indicators that the model will be useful for simulating the voltage drop characteristic.

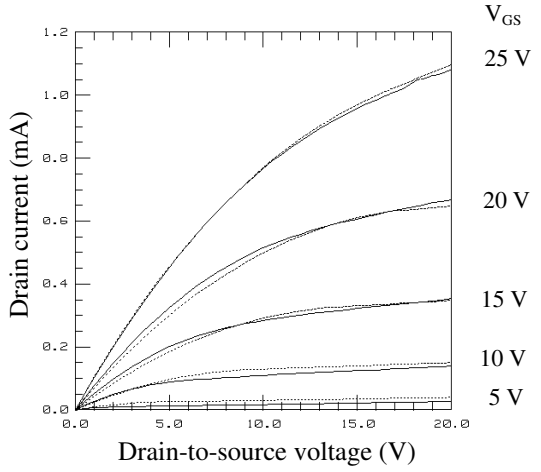

Fig. 6. Measured (—) and simulated (- - -) drain current comparison of a typical a-Si: H TFT in the saturation region.

B. Drive-Voltage Timing Measurement and Simulations of TFT-LCD

Timing measurement and simulations are used to analyze V_S waveforms and voltages when the gate pulse signal and drain pulse signal are supplied. A pulse generator (HP 8112A) and a digitizing oscilloscope (HP 54501A) were used for the timing measurement. The V_S timing information is applicable for TFT-LCD designers to the analysis of LCD switching characteristics, holding characteristics, gate pulse delay, voltage drop characteristics, common voltage (V_{com}) definition, and optical characteristics.

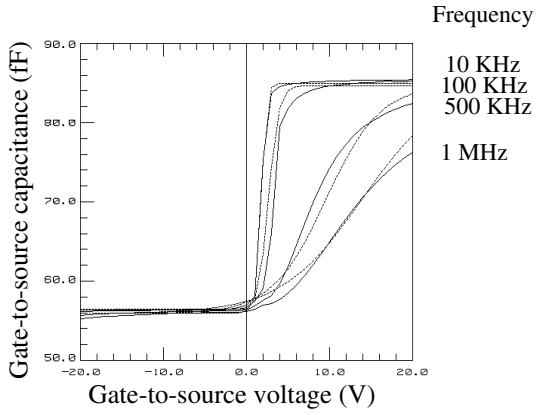

Fig. 7. Measured (—) and simulated (- - -) frequency variation of the V_{DS} = 0 gate-to-source capacitance.

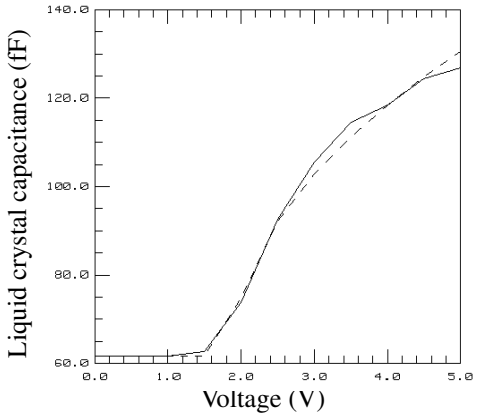

Fig. 8. Measured (—) and simulated (- - -) TN liquid crystal capacitance comparison of a sample device.

An equivalent circuit of a typical TFT-LCD pixel is shown in Fig. 9. The Liquid Crystal Cell consists of R_e (electrode resistance), C_o (surface plate capacitance), R_{lc} (liquid crystal resistance), and C_{lc} (liquid crystal capacitance).C_{st} (storage capacitance) is formed at the source terminal of the TFT. The scanning pulse signal (V_G) is supplied at the gate terminal of the TFT device. The video voltage signal (V_D) is supplied at the drain terminal of the TFT device.

Fig. 10 shows the supplied V_G and V_D waveforms and the simulated V_s waveform of the TFT-LCD pixel using the new TFT and LC capacitance models. The measured and simulated V_s waveforms are shown in Fig. 11. R_e, C_o, and C_{st} were optimized using the measured data. Geometry of the test devices and the parameters used for simulation are listed in Table 1. Theoretically, V_s must be driven by half of V_{D_HIGH} minus V_{D_LOW}. However, the

Vs waveform has a voltage drop in each cycle (Fig. 11) because the C_{lc} charging time delay and the voltage drop caused by C_{GS}, become dominant. Here, V_{D_HIGH} and V_{D_LOW} are the maximum and minimum voltage of V_D, respectively. The voltage drop characteristic is tested using two different C_{GSO} values in Fig. 12. If the voltage is defined as ΔV, it is calculated by

$$\Delta V = C_{GS} \cdot \frac{V_{G_HIGH} - V_{G_LOW}}{C_{GS} + C_{total}} \quad (44)$$

$$C_{total} = C_{st} + \frac{C_o \cdot C_{lc}}{C_{lc} + C_o} \quad (45)$$

where V_{G_HIGH} and V_{G_LOW} are the maximum and minimum voltage of V_G, respectively.

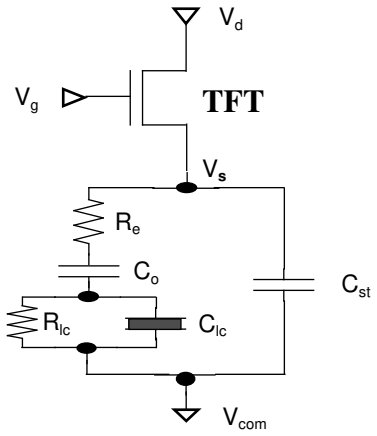

Fig. 9. Equivalent circuit of a TFT-LCD cell. Here R_e = 1.28 KΩ, C_o = 317 fF, R_{lc} = 10 GΩ, and C_{st} = 1.06 pF.

The other important state of LCD dynamic behavior is the holding state which is dominated by the TFT reverse leakage current. When the a-Si: H TFT is in a holding state, the potential drop is caused by the leakage current of the TFT itself. In this case, the amount of leakage current is given by

$$I_{leak} = C_{total} \cdot \frac{dV}{dt}. \quad (46)$$

By using (46) and the transient simulation result, the dynamic off-current can be calculated.

Using the TFT-LCD timing simulation results, V_{rms} (rms voltage of V_s) can also be calculated from the V_s signal, as shown in (47) [13].

$$V_{rms} = \sqrt{\frac{1}{t_F}\int_0^{t_F} \left(V_S - V_{COM}\right)^2 dt}. \quad (47)$$

The optical characteristics are controlled by V_{rms}, which is the voltage supplied to the liquid crystals. An accurate value of V_{rms} is necessary to analyze the optical performance of the FPD. The optical characteristics are usually defined by transmittance versus V_{rms} curves. Other optical parameters such as optical threshold voltage and contrast ratio can also be calculated using V_{rms}. As described above, the simulation results are directly applicable to TFT-LCD design evaluation.

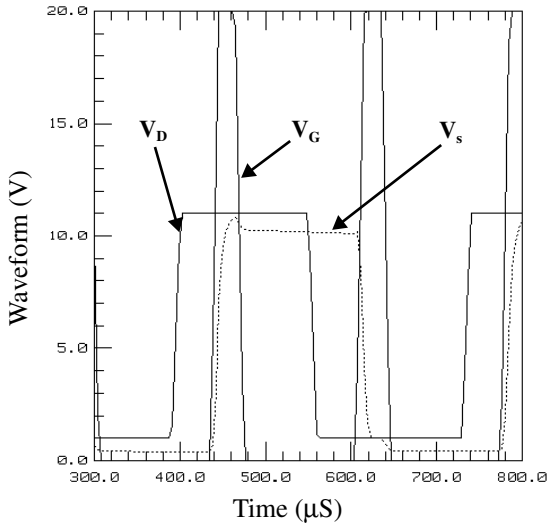

Fig. 10. A TFT-LCD cell transient characteristic. The input signals are drawn with solid (—) line and the output signal is drawn with dotted (- - -) line.

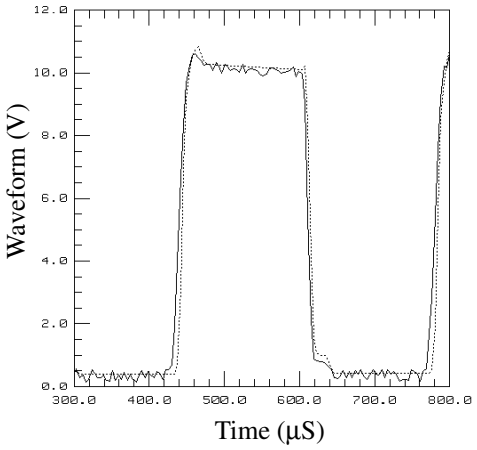

Fig. 11. Measured (—) and simulated (- - -) V_S waveform of a typical TFT-LCD cell which is shown in Fig. 9.

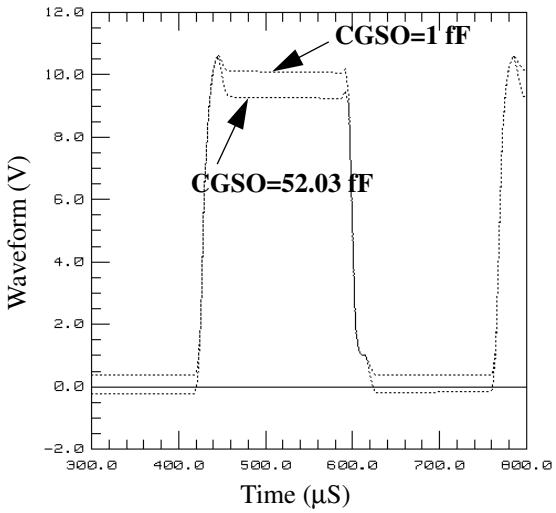

Fig. 12. The effect of the gate-to-source overlap capacitance on a TFT-LCD cell. The simulation is performed under the same condition as Fig. 10.

V. Conclusions

This paper presented new a-Si TFT and LC capacitance models and the procedures for characterizing TFT-LCD pixels. The model parameters for both a-Si TFT and LC capacitance models were extracted using the IC-CAP system. The results show good agreement between measured and simulated data. TFT-LCD timing simulation and characterization examples were shown using those extracted parameters. Three important transient states of a TFT-LCD pixel, charging, holding, and voltage drop, were analyzed successfully. The simulated driving voltage waveforms can be used in calculating V_{rms} voltage, which is one of the most important LCD design parameters for optical characterizations. These models and the modeling process are practical to use for today's advanced TFT-LCD simulations.

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