A scaling scheme for interconnect in deep-submicron processes

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In this paper, we study the requirements for interconnect in deep-submicron technologies and identify critical factors that will require innovations in process technology, process integration and circuit-and-system design techniques. We also propose a scaling scheme to optimize the interconnect for a given application domain such as microprocessors, ASIC's or memory. Two regimes of interconnect are considered: *local interconnect* which is used within a cell or a block using the finest pitch metal allowed by the design rules; *global interconnect* which is used for inter-block communication using the upper metal layers.

To identify trends in interconnect and transistor technology we use the SIA (Semiconductor Industry Association) Roadmap as a guideline [1]. The key transistor and interconnect parameters we have used in our study are shown in Tables 1 and 2 and Fig. 1. All simulations were done using a SPICE circuit consisting of a driver and a wire with two neighbors, with either one or two ground planes. Coupling capacitances were obtained from a two-dimensional field solver.

The major criteria for interconnect design that we considered are cross-talk noise, electromigration and delay, especially for global lines. Fig. 2 shows that the maximum interconnect length, with a fixed geometry, that can be switched in a clock period is a decreasing fraction of the chip-side length for future technologies. The maximum interconnect length is calculated based on the required clock frequency for each technology generation, as shown in Fig. 3. Note that this length cannot be increased significantly by increasing the driver size as most of the limitation is in the interconnect. New materials that reduce the interconnect RC time constant will reduce the delay problem, as shown in Fig. 4, but may not be sufficient nor cost-effective to fully solve it by themselves. To address the delay problem we propose a scaling scheme which incorporates the system requirements (die size, frequency) along with material constraints and process innovations.

For each layer of interconnect we use the space of horizontal pitch (line width and spacing) and vertical pitch (line thickness plus dielectric thickness) to plot contours of constant delay and cross-talk noise for a given interconnect length and driver size [2]. The optimal interconnect parameters can then be obtained directly using the graphical technique shown in Figs. 5 and 6. The optimal point, which is defined as the minimum horizontal-pitch point, meets the circuit and layout constraints, though process constraints will, of course, need to be included. In Fig. 7, the loci of the optimal interconnect design for each generation of technology, using the SIA clock cycle, are plotted on the same axes, thus providing a guideline for reverse scaling of global interconnect. Variations such as new materials can be easily incorporated in this scheme as shown in Fig. 8.

For local lines (especially in array structures such as cache RAMs) a key limitation is cross-talk (see Fig. 9). In Fig. 10, the maximum allowed wire length for a 20% induced noise, in a signal wire, is shown for different technology generations along with the electromigration limit. In this figure, we show the impact of using two driver size scaling scenarios. If unscaled drivers are used then the maximum interconnect length is longer than the scaled driver case, although there is greater power dissipation, as shown in Fig. 11. The impact of new materials on cross-talk is shown in Fig. 12. Finally, a technique that allows designers to trade-off noise immunity for transistor area is shown in Figs. 13 and 14.

In this study, we have used realistic parameters for transistors, interconnect and system performance for future technology generations to show that delay and cross talk will be severe constraints for global lines. To meet these limits we propose a scheme, which includes the impact of new materials, for optimally designing global interconnect. For local interconnect, cross-talk is the major challenge which can be addressed by selectively using larger drivers to reduce cross-talk noise when necessary.

[1] *SIA semiconductor technology – Workshop Working Group Reports*, SIA, 1994.
[2] P. Raje, *Hewlett-Packard Journal*, p. 97, February 1995.

Topic Area: Device and Interconnect Technology/Modeling and Simulation.
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TABLE 1 Interconnect Technology Parameters

Parameter	Technology					
	0.35um	0.25um	0.18um	0.13um	0.10um	0.07um
Local Line Width (um)	0.40	0.30	0.22	0.15	0.11	0.08
Local Line Spacing (um)	0.60	0.45	0.33	0.25	0.16	0.12
Local Line Thickness (um)	0.60	0.60	0.55	0.45	0.39	0.32
Dielectric Thickness (um)	1.00	0.84	0.70	0.59	0.57	0.50
Chip-side Length (mm)	15.8	17.3	19.0	20.7	22.8	24.9
Power Supply (V)	3.3	2.5	1.8	1.5	1.2	1.0
Frequency (MHz)	300	450	600	800	1000	1100

TABLE 2 Device Technology Parameters

Parameter	Technology					
	0.35um	0.25um	0.18um	0.13um	0.10um	0.07um
L_{eff} (um) †	0.28	0.18	0.10	0.08	0.07	0.06
Gate Oxide Thickness (A)	80	60	45	40	35	30
Threshold Voltage (V)	0.65	0.60	0.50	0.45	0.40	0.35

† Note that L_{eff} is not given in the SIA roadmap but is based on extrapolation from technology trends.

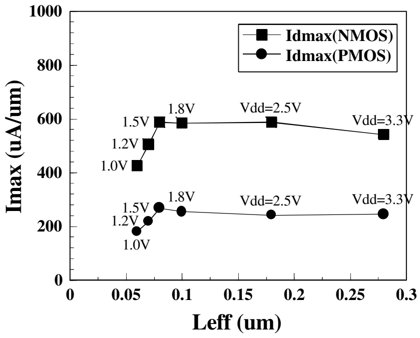

Fig. 1: Maximum drain current for NMOS and PMOS transistors of different technology generations used in this study.

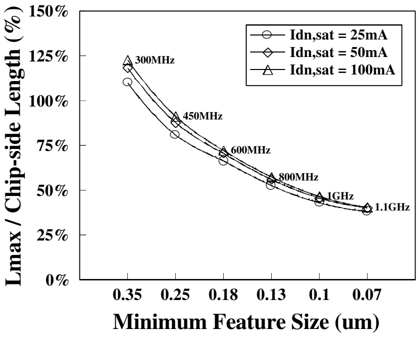

Fig.2: Maximum interconnect length / chip-side length for different driver sizes and technology generations with line width= line spacing=2um and line height=interlevel dielectric thickness=1um

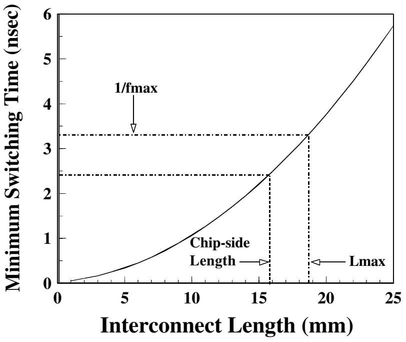

Fig. 3: Minimum switching time vs. interconnect length for 0.35um technology generation. Minimum switching time is the sum of rise and fall time. The minimum switching time = 1/f (300MHz) at Lmax.

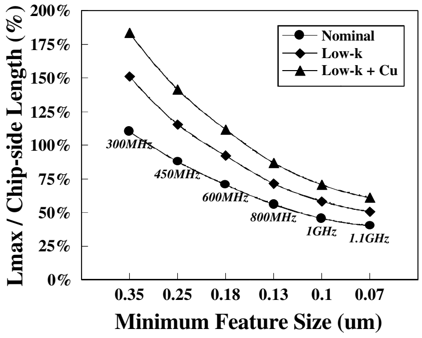

Fig. 4: Maximum interconnect length / chip-side length for new interconnect materials. Significant improvement is seen with new interconnect materials. (k=2.5)

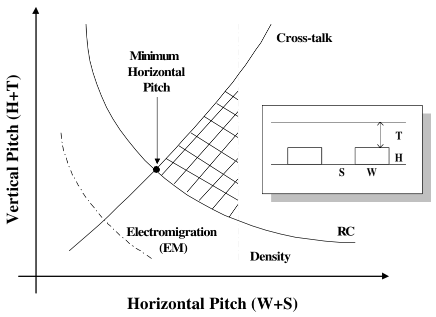

Fig. 5: Constant RC and Cross-talk noise contours in a horizontal and vertical pitch plane. H=T and W=S are assumed in the following plots for simplicity. The intercept minimizes the horizontal pitch.

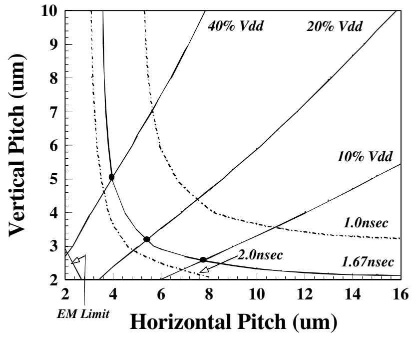

Fig. 6: Constant minimum switching time and cross-talk contours (40%, 20%, and 10% Vdd) for 0.18um technology gene-. ration. The SIA roadmap targets 1/f = 1.67nsec.

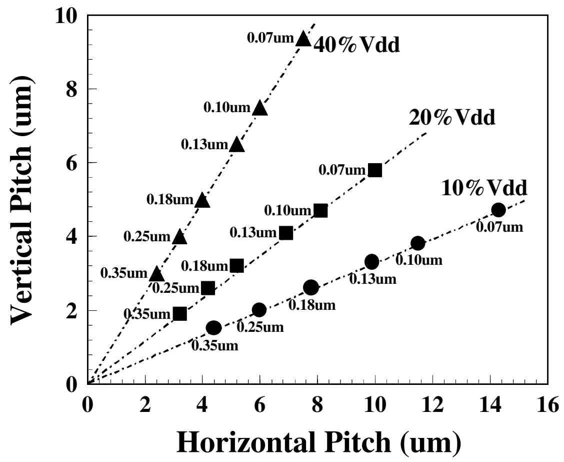

Fig. 7: Minimum-pitch design loci for chip-side length interconnect. Note that global interconnect must be scaled up to meet the SIA road map as the technology generation advances.

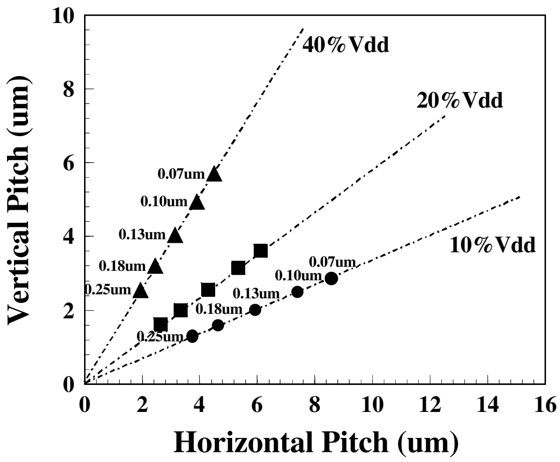

Fig. 8: Minimum-pitch design loci for chip-side length interconnect with low-k interlevel dielectric (k=2.5) and copper. Both the vertical and the horizontal pitches are approximately 30% smaller with new materials.

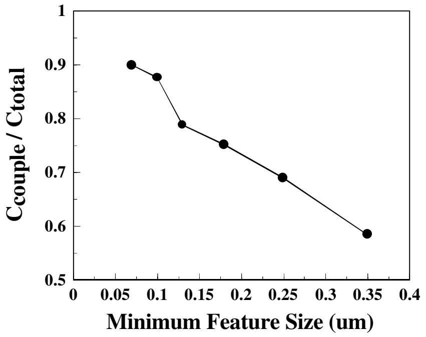

Fig. 9: Ratio of interlayer capacitance to total capacitance assuming long, uniform minimum spacing lines with ground planes above and below.

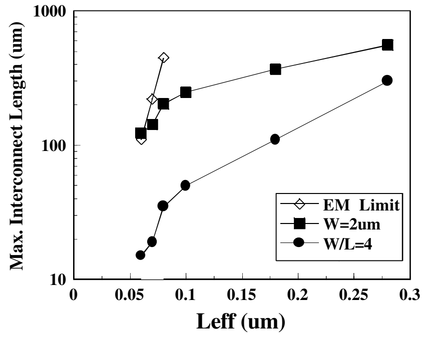

Fig.10: Maximum interconnect length for 20% Vdd cross-talk noise and the electromigration limit using a maximum average current of $2 \times 10^5 Acm^{-2}$

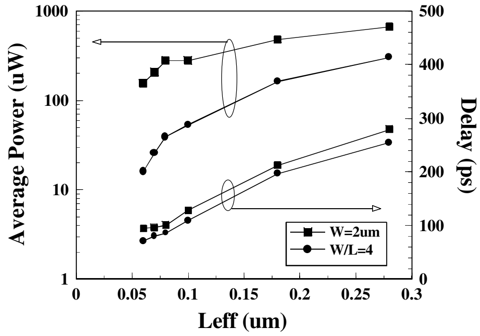

Fig. 11: Average power dissipation and delay/stage driving the max. interconnect length shown in Fig. 10. The difference in power is due to the difference in interconnect and load capacitance.

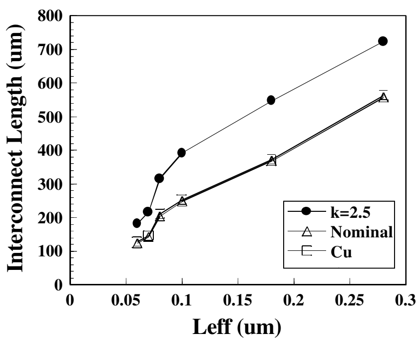

Fig12: The effect of Copper and low-k interlevel dielectric on the maximum interconnect length for cross-talk noise of 20% Vdd for a fixed driver size of 2um.

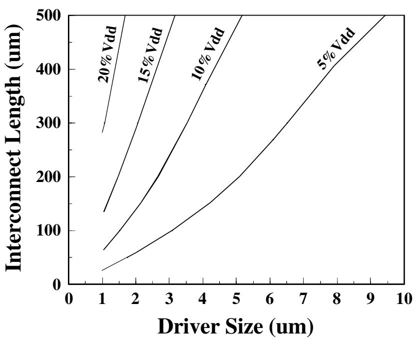

Fig. 13: Contours of constant cross-talk noise for 0.35um technology using minimum spacing lines.

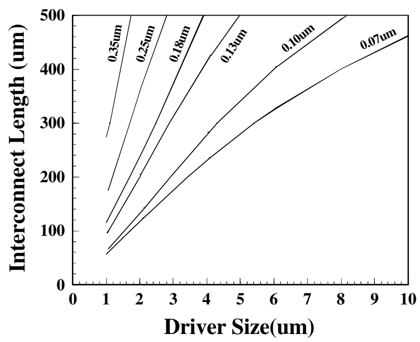

Fig.14: Contours of 20% Vdd cross-talk noise for different technology generations using minimum spacing lines.