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EMC Issues Relating to the Design of Communicating Appliances

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The development of commercial products combining both digital electronics and RF (Radio Frequency) circuits gives rise to some important EMC (Electromagnetic Compatibility) challenges. These can broadly be categorized into two main areas, namely: Does RF interference from the transmitter of the radio cause upset of the digital circuits? Will the sensitivity of a receiver be reduced if it is placed in close proximity to some digital circuitry? This paper reports explorative measurements in both these areas. Comparative measurements of susceptibility of logic gates to RF interference are presented. These results indicate that the use of HC (High speed CMOS) devices can considerably reduce susceptibility to RF interference. In addition measurements have been taken to show how receiver sensitivity can become degraded when operating in close proximity to digital circuitry.

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1 ABSTRACT

The development of commercial products combining both digital electronics and RF (Radio Frequency) circuits gives rise to some important EMC (Electromagnetic Compatibility) challenges. These can broadly be categorised into two areas, namely:-

- Does RF interference from the transmitter of the radio cause upset of the digital circuits?
- Will the sensitivity of a receiver be reduced if it is placed in close proximity to some digital circuitry?

This paper reports explorative measurements in both these areas. Comparative measurements of susceptibility of logic gates to RF interference are presented. These results indicate that the use of HC (High speed CMOS) devices can considerably reduce susceptibility to RF interference. In addition measurements have been taken to show how receiver sensitivity can become be degraded when operating in close proximity to digital circuitry.

2 INTRODUCTION

In recent years we have witnessed a rapid growth in the use of mobile communications and the emergence of digital radio technologies. In parallel with this PDAs (Personal Digital Assistants) are now starting to enter the market place. It is envisaged that an important element of many of these PDAs will be their ability to communicate. Which implies that future PDAs may well have "built-in" digital radios. The successful integration of both RF and digital circuitry requires close consideration of their EMC interaction. In this paper some of the problems are described and supported through measurement.

3 RFI UPSET OF DIGITAL CIRCUITS

Digital circuits use logic gates which are non-linear devices and engineered to have a threshold at the input and thus operate in one of two states. Digital circuits are therefore by definition resilient to noise in that they only register a degradation in the performance if the noise is able to exceed the threshold and change the state of an input or output. Once this happens however, the degradation will not be graceful and the equipment is likely to stop working or perform highly erratically.

If a logic gate is subjected to large amounts of RFI then they can begin to exhibit diode like properties and rectify the signal, Whalen et al[1]. This gives rise to a dc offset in the signal which ultimately will exceed the threshold and give rise to errors in the device.

3.1 EMC Susceptibility Measurements for Several Logic Families

An experiment was devised in order to assess the EMC susceptibility of individual logic gates from different families. This was done by submitting digital gates to RF interference for a variety of different digital inputs. No effort was taken to match the RF power into the device, instead couplers were used to measure the forward and reflected powers.

Experimental set-up. Figure 1 shows the experimental set up which was used to perform the measurements. An RF signal generator was used to generate CW (Continuous Wave) signals over a frequency range from 50 MHz to 2 GHz. This was then combined with a square wave generated by a bit error rate tester (BERT, HP3784A) and then passed through a pair of directional couplers, and a bias tee, before finally being applied to the gate. The two directional couplers were used to measure both forward and reverse power and thus it was possible to calculate the power absorbed in the device. The signal coming from the BERT was a.c. coupled to be combined with the RF source, and the bias tee was used to provide a dc level such that the wave represented a useful digital signal for testing. A clock recovery board was built and this was used to recover a clock from the square wave output of the DUT, both these signals were then passed into the BERT and an error test was done. Whilst it would have been preferential to use a PN sequence and not a square wave when testing for errors this was not possible as it was necessary, because of the couplers, to use a wave whose d.c. component was static when averaged over a very short time.

Both the input and output were tested for susceptibility to RFI. For the output the RF power was applied via a 150 Ω resistor (chosen to represent the impedance of a digital line), which was necessary in order to enable the gate to output a logic high.

All measurements were taken with NAND gates. Whilst some measurements were tested for repeatability, no effort was made to test many samples of the same gate from the same and different batches. The authors were looking for fundamental differences and trends which would arise in single measurements

of different gates and not for an accurate characterisation of each family.

The maximum powers available for generating the RFI were 21 dBm for all frequencies except 1.87 GHz where a power amp was used to achieve 40 dBm output power.

Care was taken to decouple the supply of the gate under test.

Measured Results. Figure 2 shows a failure signature for a 74ALS00 gate. This graph indicates the power absorbed into the chip for the BERT to indicate an error (error rate greater than $1x10^{-5}$) for the gate over a frequency range.

This shows that the digital gate is potentially upset by quite low signal powers. A cellular hand-set operating around 1 GHz may typically transmit 1W or 30 dBm, this curve indicates that if the coupling loss between the transmit antenna and the digital circuitry is less than 25 dB then the digital circuit may exhibit upset performance.

However the ALS family was found to be the most susceptible and with the other families it was not possible to measure a similar curve as the powers required were too high.

One observation made in the measurements has been both modelled and measured by others, Whalen et al[1][2]. This was that the digital gate was rectifying the RF wave at its input/output and this was giving rise to an increased d.c. level. It was therefore decided to measure the d.c. level at the point of interference and observe this rectification. An initial measurement was taken with no gate to establish that there were no other rectification effects taking place elsewhere.

Consideration was given to the driving impedance for both the static and clocked sources. The d.c path of the bias tee was measured to have a resistance of only 3Ω, and the voltage setting on the bias tee was set from a potential divider with a total resistance of 1 MΩ. This therefore means that for static low input the dc resistance to earth is low. For the static high input, the resistance is approximately 220 kΩ (3V was used for a static high and the source was 4.5V), and for a clocked input the resistance is also high. In addition for clocked inputs the BERT has to drive the RF combiner and directional couplers in addition to the bias tee. This is an important point as the source impedance may affect the circuits "hardness" to RF.

For the output susceptibility measurements an additional 150 Ω was placed in series with the bias tee in order that the output circuit was not short circuited and therefore able to drive a logic high.

Measured d.c. rectification at the input. Figures 3 through to 6 show measured d.c. rectified voltage vs absorbed power (at the input) for different logic families with different input waveforms.

Several observations can be made from studying these curves, namely:-

- the ALS family is the most susceptible to RFI
- the input becomes less susceptible for higher frequencies of RFI
- a clocked input is arguably more susceptible than a static high or static low (see discussion).
- Most of the curves exhibit "diode like" exponential characteristics and these are shown on a logarithmic scale to demonstrate this.

At a frequency of 1.87 GHz, similar to that used by both DECT (Digital European Cordless Telephone) and DCS1800 the measured required power for failure of a clocked input is given in table 1.

Table 1: Absorbed power for gate error at the input with a clocked signal

Logic Family	Absorbed power (dBm)
ALS00	17
F00	21
AS1000	23
HC00	>29

This indicates that a PDA which used, for example, DCS1800 and had a transmit power of 30 dBm would not suffer from RF interference should HC devices be used. However in the event of using ALS devices then if the coupling loss is less than 13 dB (which is highly unlikely) then malfunction would be possible.

Measured dc Rectification at the Output. Figures 7 through to 10 show the rectified dc levels (at the output) for different families, with different inputs for different frequencies.

The following observations can be made from these measurements:-

- the output seems less susceptible than the input
- RFI rectification model does not seem valid with several curves not exhibiting diode like properties. Due to the offsets sometimes having negative values the curves have not been shown on a logarithmic scale.
- the greatest overall change is only 300 mV
- effect reduces with increasing frequency
- clocked input does not always give the largest error

Discussion. These results are interesting in that they demonstrate that there is an EMC issue over the upset of digital circuits when subjected to moderate levels of RFI. They have also demonstrated some important

trends which offer useful information to a system designer. The measurements have shown that different families have different susceptibilities, such that a digital designer who is operating in an RFI environment would benefit from using HC devices.

The effect has also been found to be reduced with increasing frequency.

The measurements show that clocked inputs (with RFI applied to the input) are the most susceptible. Whilst this is a valuable result, it is felt that this may arise due to the different source impedances of the driving waves. For an input static low the gate is loaded to ground by the bias tee with low resistance and hence the signal will be difficult to load with a rectified source. In the two cases of a logic high (3V) and a varying input then the bias tee is set such that it has a high source impedance and may therefore be more susceptible to an RF rectified source. This suggests that both the logic high input and the clocked waves should be more susceptible, however the measurements indicate that the clocked wave was significantly more susceptible than that of the logic high input.

In a paper by Whalen et al [1] they report that for a 7400 the scenario of RFI on the output with the inputs high as being the most susceptible. This contrasts with the measurements taken here for two possible reasons. Firstly the paper by Whalen only considers static inputs, and also the discrepancy may arise due to different source impedances.

Finally, subsequent measurements performed at a system level have found circuits to be more susceptible to burst RF power than to CW signals. It is not clear whether this trend would be exhibited with the digital circuits in this experiment and this is an area for further work. For baseband analogue circuitry it is understandable that they are more susceptible to burst RF. An analogue circuit which is a.c. coupled would block a rectified d.c. level. However for burst RF interference the rectified signal would have an a.c component and hence could cause interference.

4 RECEIVER MALFUNCTION DUE TO DIGITAL INTERFERENCE.

The other EMC issue relating to the communicating appliances is that of the digital circuitry radiating significant energy in the band of the radio receiver. If the PDA emits interference at this frequency then the receiver will be desensitized and the only cure for this will be to shield the digital circuits in the PDA or improve the layout of the digital board.

Measurements have been carried out for the emitted power from a commercially available PDA. These were performed using a magnetic close field probe which was inserted into the PCMCIA slot of the device. Figure 11 shows the experimental set up used.

The results of these experiments are shown in figure 12. The measurements were all taken at harmonics of 15.837 MHz, which is the fastest clock within the PDA. The measurements quote field strength in dBμV/m. In order to understand these figures it is useful to relate them to the sensitivity of a typical receivers, which is around -104 dBm, Lehtinen [3] for a GSM handset and -125 dBm for a paging receiver, Wilson et al [4]. This figure can be related to a field strength from the effective aperture of the antenna. The maximum effective aperture of an antenna is related to its directivity or gain by, Paul[5]:-

$$G(\theta,\phi) = \frac{4\pi}{\lambda^2} A_{em}(\theta,\phi)$$

where G(q,f) = the directivity of the antenna

A_{em}(q,f) = the effective aperture of the antenna

q = the angle in the horizontal plane

f = the angle in the vertical plane

Assuming a gain of 0dB, A.P.L.[6] implies a maximum effective aperture of 8.8×10^{-3} m². Given that the power in dBms at the input to the pre-select is equal to the power density multiplied by the effective aperture of the antenna, the sensitivity is approximately 22 dBμV/m for a GSM handset and 2.5 dBμV/m for a pager. Figure 6 shows the measured RFI from the PDA and indicates fields of around 100 dBμV/m at paging frequencies and an extrapolated value of 65 dBμV/m at 900 MHz. This suggests that if the antenna was located inside the PCMCIA slot of the PDA the power would be sufficient to desensitize the paging receiver. Indeed measurements at 450 MHz have shown this to be the case, with the sensitivity degradation as much as 20 dB in the worst case.

However there will be a significant radiation loss from the PCMCIA slot to the location of the handset antenna. In addition the maximum value for the effective aperture of the antenna was used and hence the sensitivity will typically be worse than that quoted. Given these points it is unclear whether a GSM handset would be desensitized by a PDA. Practical measurements have found no evidence of the PDA causing upset of the GSM phone.

It is also possible that power at other frequencies could be either demodulated as a spurious frequency in the mixer and desensitize the receiver. This should not be too much of a problem as the spurious rejection within the radio should be sufficient. In addition other frequencies could feed directly into the IF(Intermediate frequency) of a receiver, although the receiver design should have avoided this.

5 CONCLUSIONS AND FURTHER WORK

This paper has addressed the problems of EMC integration for radio communicating appliances. Measurements have been performed to show the extent

of the problems. The results have been discussed and some explanations given. Comparative measurements of different logic families suggest that HC devices are the least susceptible to RF interference.

In additions measurements have been taken which show that sensitive receivers can potentially suffer from close interaction of digital circuits.

The paper has also highlighted the importance of considering the impedances of the driving source, when considering its resilience to RF. This remains an extraneous variable within this work and further work could be done to investigate variation of the source impedance or comparisons of digital signals with equal source impedances.

Finally further work could be done to investigate the effect of gating the RF power. Measurements taken at a system level (not reported here) have found baseband circuits to be more susceptible to burst RF interference.

6 ACKNOWLEDGEMENTS

The authors would like to thank their colleagues Tom Gardner and Graeme Proudler for their enlightening analysis of this work.

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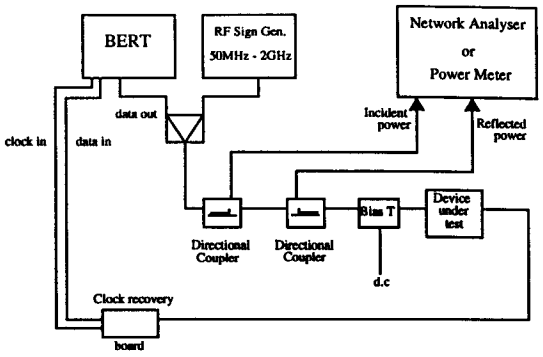

Figure 1 Test set up for measurements of RFI upset of digital gates

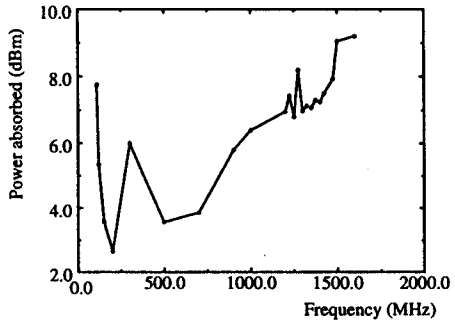

Figure 2 Failure signature for 74ALS00 with RFI applied to the input and the input clocked.

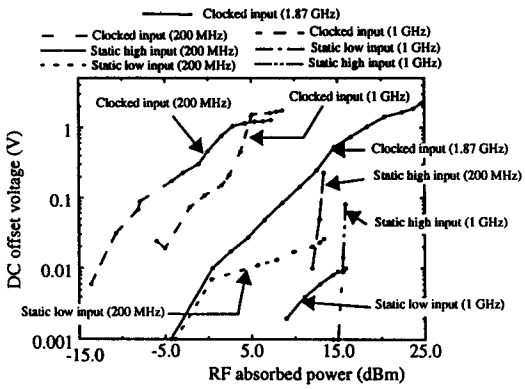

Figure 3 Rectified DC voltage vs absorbed RF power (at the input) for a74ALS00 gate with different input waveforms

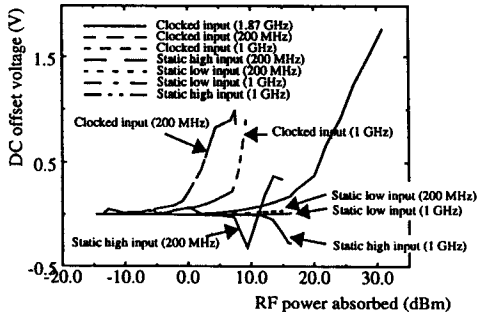

Figure 4 Rectified DC voltage vs absorbed RF power (at the input) for a 74AS1000 gate with different input waveforms

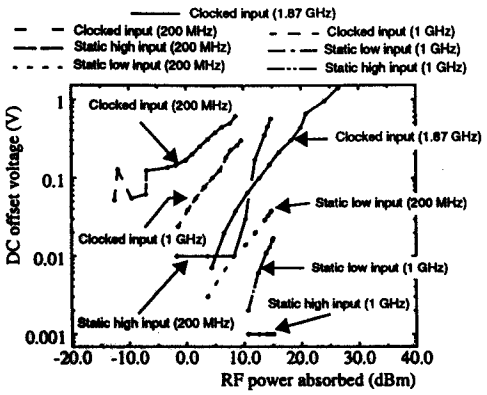

Figure 5 Rectified DC voltage vs absorbed RF power (at the input) for a 74F00 gate with different input waveforms

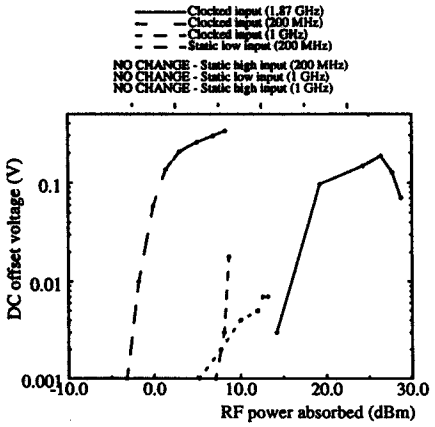

Figure 6 Rectified DC voltage vs absorbed RF power (at the input) for a 74HC00 gate with different input waveforms

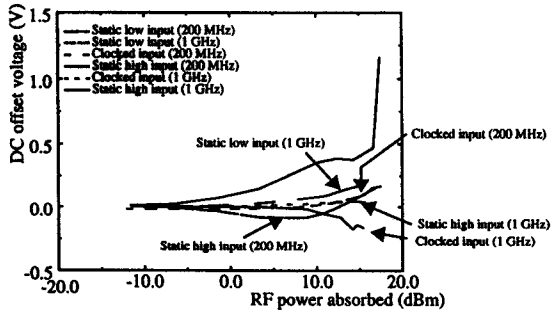

Figure 7 Rectified DC voltage vs absorbed RF power (at the output) for a 74ALS00 gate with different input waveforms

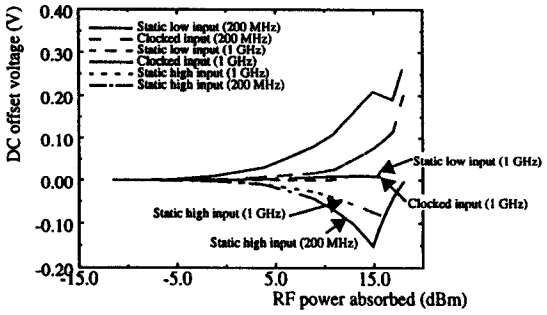

Figure 8 Rectified DC voltage vs absorbed RF power (at the output) for a 74AS1000 gate with different input waveforms

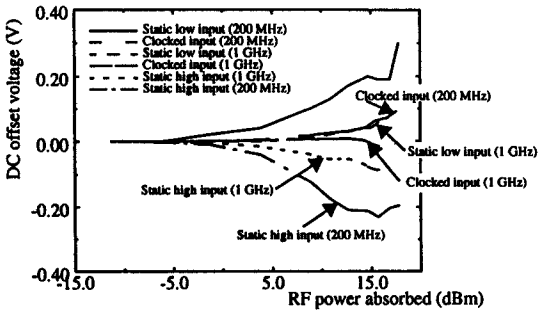

Figure 9 Rectified DC voltage vs absorbed RF power (at the output) for a 74F00 gate with different input waveforms

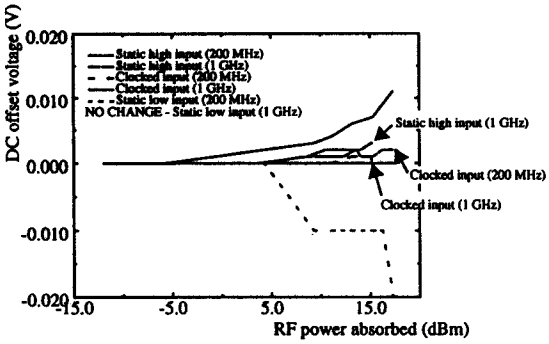

Figure 10 Rectified DC voltage vs absorbed RF power (at the output) for a 74HC00 gate with different input waveforms

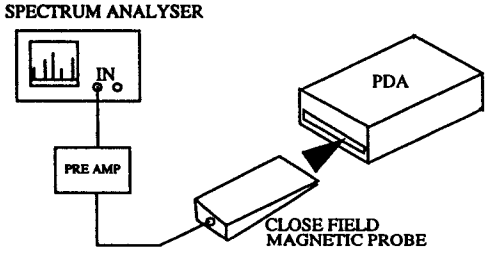

Figure 11 Set up for measuring RFI inside a PDA whilst in use.

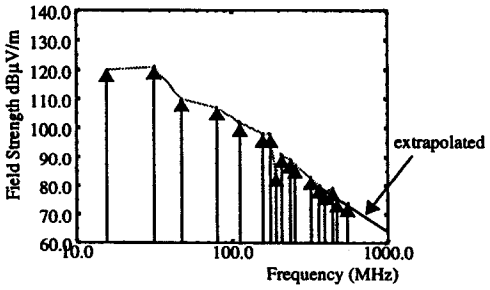

Figure 12 Measured RFI from a 200 LX