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Modeling and Analysis of Multichip Module Power Supply Planes

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HPL–94–32
March, 1994

power supply, multi chip module, thin film, thick film, plane, bypass capacitor, switching noise, ground bounce, SPICE

Abstract — A method that would allow accurate modeling of arbitrarily shaped planes with bypass capacitors has been developed. It is compatible with a SPICE based modeling method for the rest of the power supply hierarchy and the devices.

A modified SPICE is used to accommodate distributed circuits. The distributed circuits are built with microwave analysis software and connected to SPICE by s-parameter files. The modeling process is described and examples of thick and thin film power supply planes are presented with comparison to measured results. The method is used to explore potential design choices for a large MCM with many simultaneously switching drivers.

Internal Accession Date Only

1 Introduction

It has long been recognized that power supply noise induced by large numbers of simultaneously switching digital circuits can limit their performance [Davi82]. The distribution of power within digital systems must be done in a manner which both provides a low impedance voltage and ground connection to the devices and also minimizes their coupling to each other. Stated another way, the ideal power distribution network, consisting of elements local to the devices (Z_l in Figure 1(a)) and common to the devices (Z_c in Figure 1(a)), would present a voltage source of zero impedance at all frequencies to the devices. Failure to meet this goal at high frequency will result in voltage spikes when fast current edges are demanded by the devices. Failure to meet it at low frequencies will result in voltage droop when long duration surges of current are demanded by the devices. Additionally, this ideal network will present zero coupling at all frequencies between devices. Failure to meet this goal will result in the spikes or droops produced by one device affecting neighbor devices and thus limiting the maximum number of active devices allowable for reliable circuit operation.

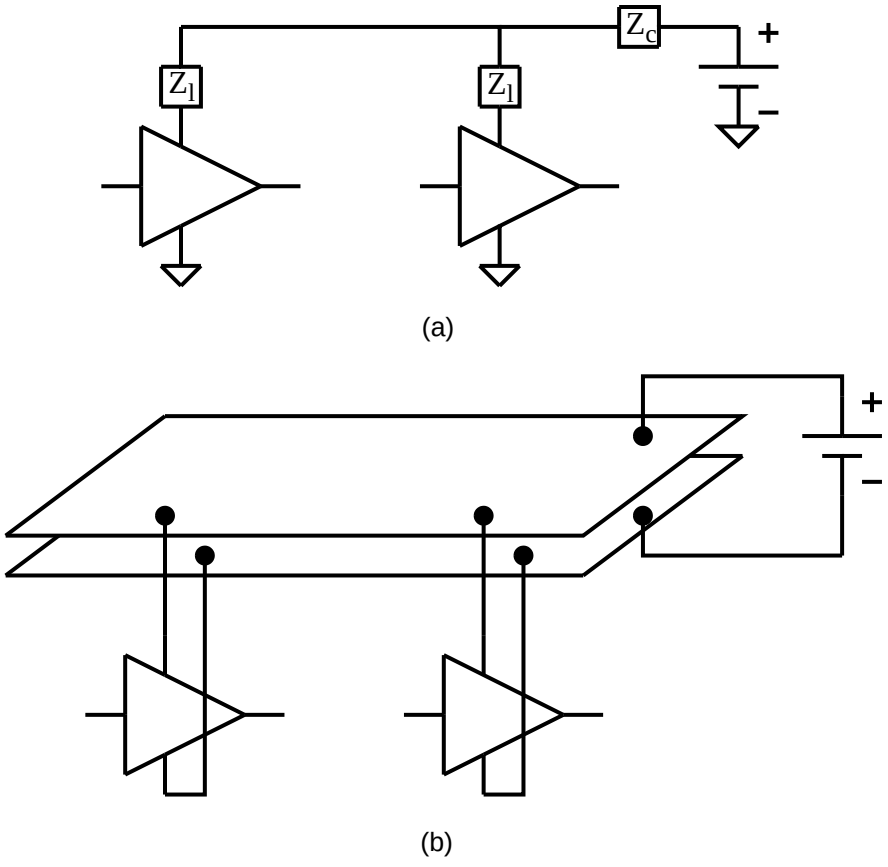


Figure 1. Power distribution networks. (a) generalized; (b) planar structures used for high frequency performance.

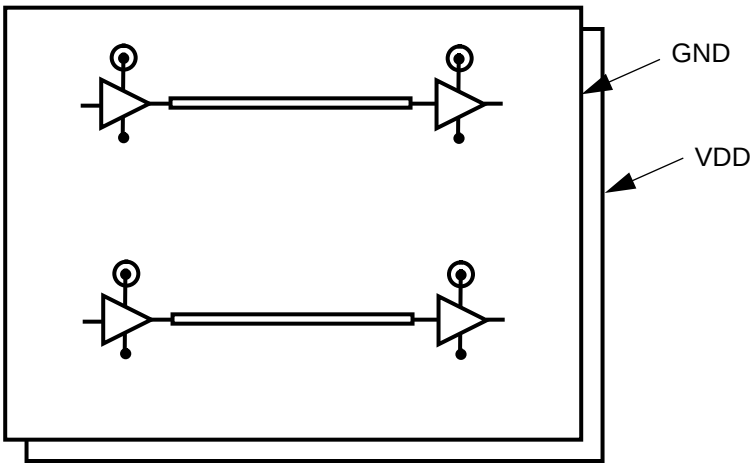
The principles for designing such a network, described in [Davi82], suggest a hierarchy of elements beginning with the power supply unit itself and proceeding through the cables, PWB's, and pins to the planes or wires doing local distribution within a package or module. The goals of low impedance and isolation are achieved at low frequency by the element lowest on the hierarchy, the power supply itself, typically through use of negative feedback. At medium frequencies they can be achieved with large value bypass capacitors placed near the devices. At the highest frequencies the goals are achieved by placing very small, and consequently modest value, bypass capacitors very close to the devices in an attempt to reduce their parasitic inductance, and thus high frequency impedance, to a minimum value [Down93]. The skillful designer will integrate this hierarchy in a way that achieves these goals seamlessly from DC to the highest frequency necessary for the bandwidth or risetime of the devices.

In high speed digital multichip modules (MCM's) planes are used for local power distribution, Figure 1(b), to achieve the necessary high frequency performance. The behavior of these planes has been successfully modeled using lumped elements [Beck93][Schm88]. However, the accuracy of such models will naturally be limited to risetimes much longer than the propagation time across the plane. Only a distributed circuit can accurately model the effects of high frequency noise coupled into these planes, reflected from its boundaries, and arriving at another device some time later. Distributed models of the planes have been used in [Sent93][Prin92]. However, only the current flow parallel to a signal trace has been considered. Two-dimensional current flow in the plane has been included in the work of [Naka92], but only with respect to a signal trace. We sought a method that would allow accurate modeling of arbitrarily shaped planes with bypass capacitors and yet be compatible with our modeling method for the rest of the power supply hierarchy and the devices — SPICE.

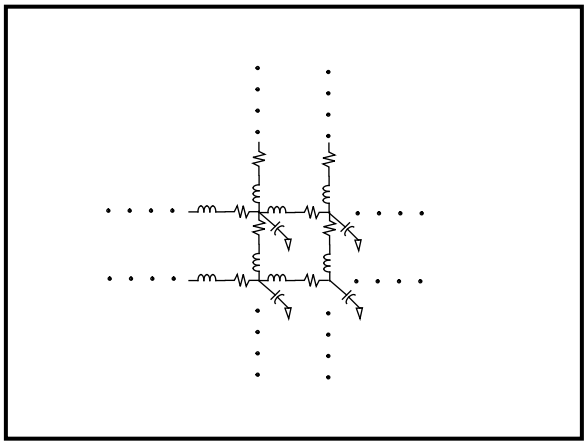
The result was a modification to SPICE to accommodate distributed circuits. The distributed circuits are built with microwave analysis software and connected to SPICE by s-parameter files. The modeling process will be described and simple examples presented with comparison to measured results. The method will be used to explore potential design choices for a large MCM with many simultaneously switching drivers.

2 Modeling methodology

Figure 2(a) is a schematic drawing of drivers and receivers connected to power supply planes. When a driver pulls current from the VDD and GND plane the current creates a voltage drop according to the impedance formed by the plane pair. This impedance has been modeled as an effective inductance, L_{eff} [Davi82]. However, for high speed systems this impedance cannot be represented with a lumped inductor, but it should be treated as a distributed element. The distributed plane model can be built with a two-dimensional array of C's, R's, and L's as shown in Figure 2(b).



(a)



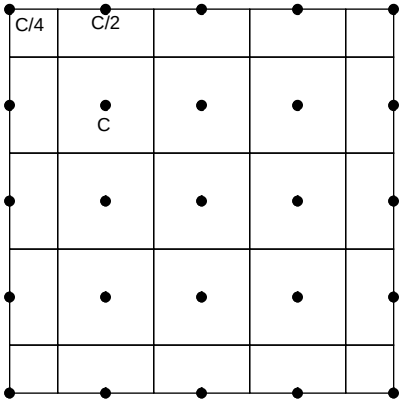
(b)

Figure 2. Power supply planes and the equivalent circuit. The nodes on the equivalent circuit represent the node on VDD plane with respect to GND plane.

The values of the lumped elements can be calculated as follows. Figure 3(a) shows a plane pair divided into square capacitive cells. The array of dots represents the locations of electrical nodes of the corresponding CRL array model. The capacitance of an internal cell, C, is

$$C = \varepsilon \frac{l^2}{d}$$

where ε, l and d are the permittivity of the dielectric, the side dimension of the cell, and the thickness of the dielectric, respectively. The size of the discretized cells, l, should be much (about ten times) smaller than the wavelength of the highest frequency component of interest in order to obtain a good approximation of the distributed element with the lumped elements. The cells on the boundary are assigned with a half or quarter of the capacitance of an internal cell. The same plane

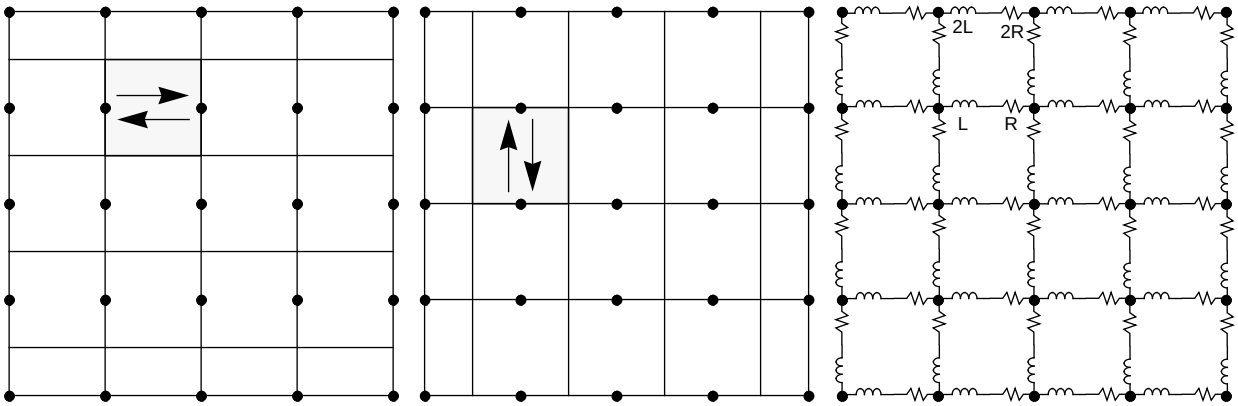


$$C = \varepsilon \frac{l^2}{d}$$

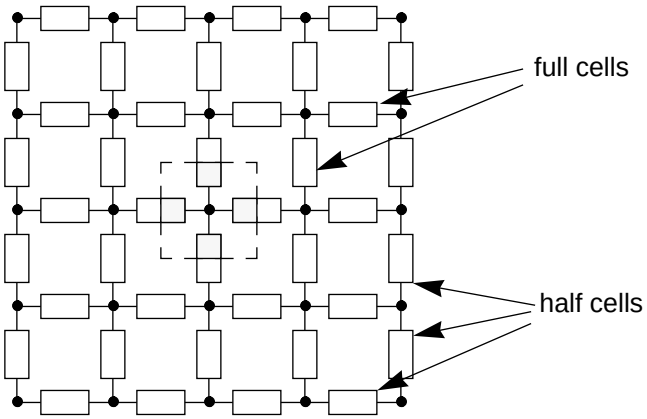
$$R = 2\frac{\rho}{t}$$

$$L = \mu d$$

(a)



(b)



$$Z = \sqrt{2}\sqrt{\frac{L}{C}}$$

$$V = \sqrt{2}\,\frac{1}{c\sqrt{\mu\varepsilon}}$$

$$Z = 2\left(\sqrt{2}\sqrt{\frac{L}{C}}\right)$$

$$V = \sqrt{2}\,\frac{1}{c\sqrt{\mu\varepsilon}}$$

(c)

Figure 3. Equivalent circuit of a plane pair: (a) Capacitive cells.
(b) Horizontal and vertical resistive/inductive cells.
(c) Equivalent circuit with transmission line models.

pair is divided into the same size cells but with a half pitch offset for resistive/ inductive cells as shown in Figure 3(b). The values of the resistance and inductance of an internal cell are calculated as

$$R = 2\frac{\rho}{t}$$

$$L = \mu d$$

where ρ, μ, and t are the resistivity of planes, the permeability of substrate, and the thickness of the planes, respectively. The factor 2 in R is to include the resistance of both planes.

A meshed plane pair, which is commonly used in MCM substrates, can be modeled as a solid plane pair with effective CRL values since the size of the mesh is usually much smaller than the wavelength of interest. The effective capacitance is obtained from a three dimensional static field calculation including the fringing fields in the mesh. The effective inductance is calculated from the capacitance knowing the wave propagation velocity in the dielectric and the effective resistance is calculated from the mesh pattern geometry.

Using this lumped array model the propagation of switching noise between the two planes can be simulated with a circuit simulator such as SPICE. A shortcoming of this model is that it does not include skin effect, which is important for the high frequency signals of our interest. In order to include the skin effect, a new model was built with a two-dimensional array of the lossy transmission line model in HP MDS (microwave design system) as shown in Figure 3(c). Each rectangular box in Figure 3(c) is a lossy transmission line shown in Figure 4. Its characteristic impedance(Z) and relative

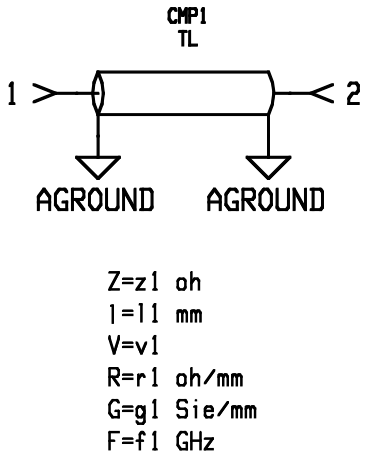


Figure 4. MDS transmission line model with skin effect. Z, l, V, R, G, and F are characteristic impedance, length, relative velocity, DC series resistance, shunt conductance, and skin effect reference frequency, respectively.

propagation velocity (V) are calculated by

$$Z = \sqrt{2}\sqrt{\frac{L}{C}}$$

$$V = \sqrt{2}\,\frac{1}{c\sqrt{\mu\varepsilon}}$$

where c is the speed of light. The $\sqrt{2}$ is multiplied in the above equations in order to compensate for the double counting of the plane capacitance in the two-dimensional array of the transmission lines. It is because four halves, or two, transmission line sections fall into one cell area as shown in Figure 3(c) with shaded areas.

MDS is a frequency-domain based simulator and its standard output is n-port s-parameters. Because meaningful noise calculations should be done with the accurate models of active circuits (drivers and receivers) using a time-domain simulator, we used a modified version of SPICE, SSPICE, which can take circuit elements described in n-port s-parameters [Troy94].

As shown in Sec.5 and Sec.6, we extract the n-port s-parameter model of a power supply structure including planes using MDS and connect it to the active circuits in SSPICE for the transient analysis of power supply noise. In the next two sections we experimentally will verify the accuracy of the power supply model built with MDS.

3 Thick film test module

In order to verify the model of power supply planes discussed in the previous section, test structures were built with a thick film substrate. Figure 5 shows one of the test structures. Two planes are separated by 280 μm thick alumina and the bottom plane is connected to the pads in the cutouts of the top plane with vias as shown in the cross section in Figure 5. The frequency response of the plane pair was measured with a vector network analyzer (HP8510C) by probing the pad connected to the bottom plane with respect to the top plane. The probing pads were probed with Cascade microwave probes with GSG or GS configuration which were calibrated from 50 MHz to 20.05 GHz.

This experimental circuit was simulated with the MDS model of Figure 6, an array of transmission lines as described in Section 2. The values of the transmission line elements are as follows:

Z = 47.58 Ω
l = 1 mm
V = 0.457
R = 0.02 Ω/mm
G = 0 Sie/mm
F = 0.1 GHz

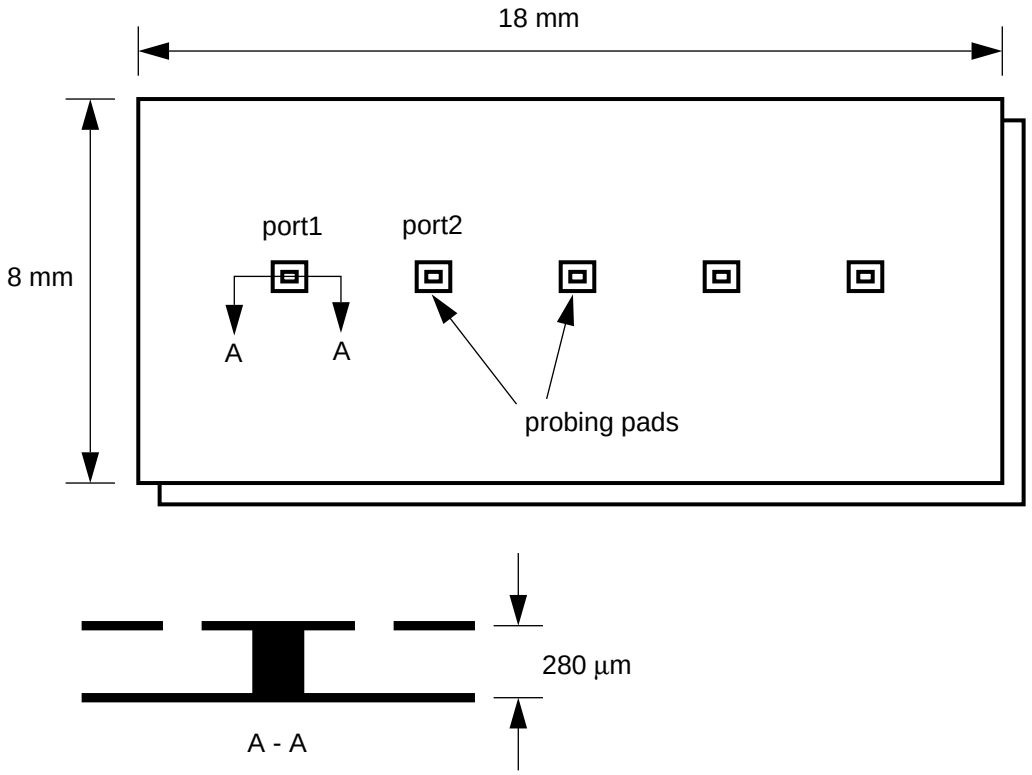


Figure 5. Thick film test structure. The planes are made with 16 mΩ/sq. tungsten and the dielectric is alumina with a relative dielectric constant of 9.6.

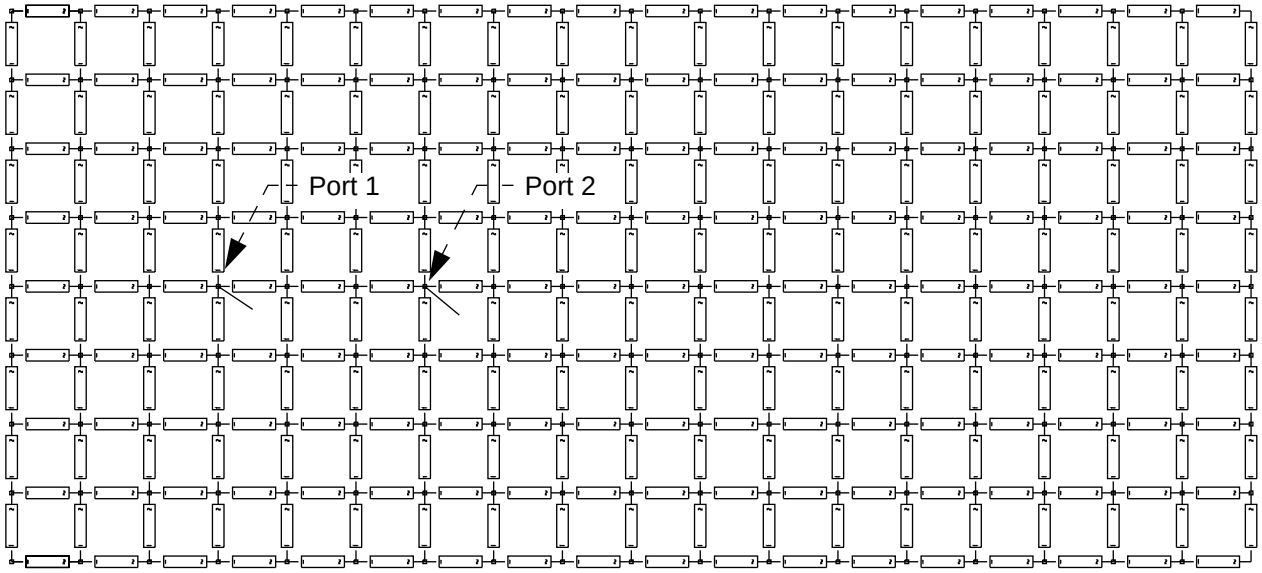


Figure 6. Model used to simulate the plane pair of Figure 5. Each square represents 1 mm square in the plane.

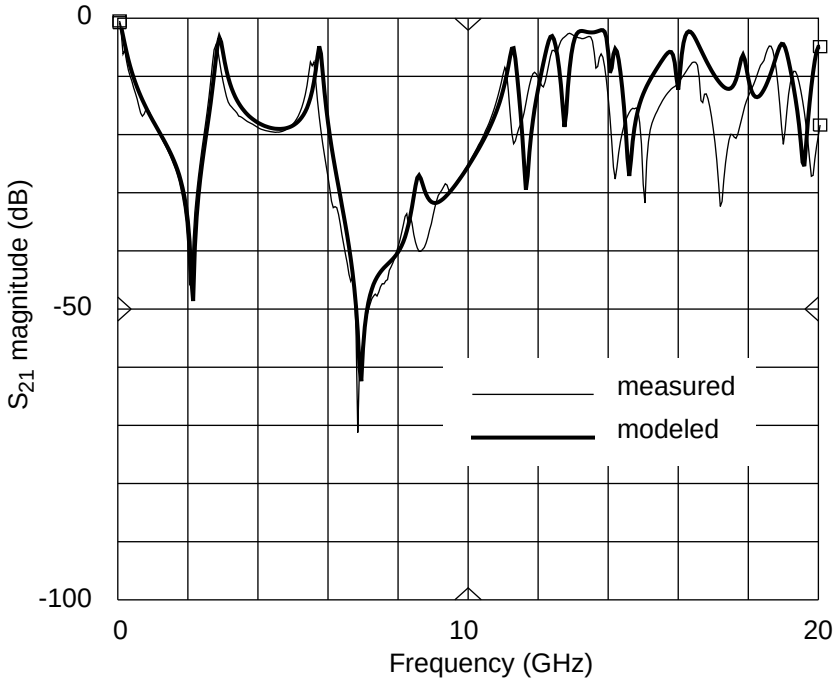


Figure 7. Measured and modeled results for plane pair of Figure 5 using model of Figure 6.

The measured and modeled results of S_{21} (magnitude only) between port 1 and port 2 are shown in Figure 7. Good agreement is evident to 10 GHz with some deviation in detail above that frequency. Potential sources of high frequency error include dispersion, dielectric loss, matrix granularity, probe discontinuities, and edge radiation.

The presence of peaks and nulls in the S_{21} response of Figure 7 is due to standing waves within the planes. One value of this model is the capability to visualize these standing waves as an aid to understanding the coupling between drivers through the power supply. Figure 8 shows a simple example, based on this thick film test module, of the standing waves present at 2.15 GHz, the frequency of the first S_{21} null of Figure 7. It can be seen that the physical position of port 2 corresponds to one location of this standing wave null. Thus there is no coupling from port 1 to port 2 at this frequency. The position of this null is determined by the quarter wave spacing from the open circuit right hand edge of the structure. If port 2 could be moved closer to that edge, the frequency of this null would increase. Similarly, peaks in this S_{21} response occur either at antinodes of the standing wave pattern or at any position other than a node but at a frequency where the whole structure resonates. An example of the latter is shown in Figure 9, the standing wave picture at 2.9 GHz, the frequency of the first peak of Figure 7. Here the whole structure is one half wavelength long and the magnitude of the standing waves is at a local maximum. Thus coupling between any two ports not located along the node is maximum at this frequency.

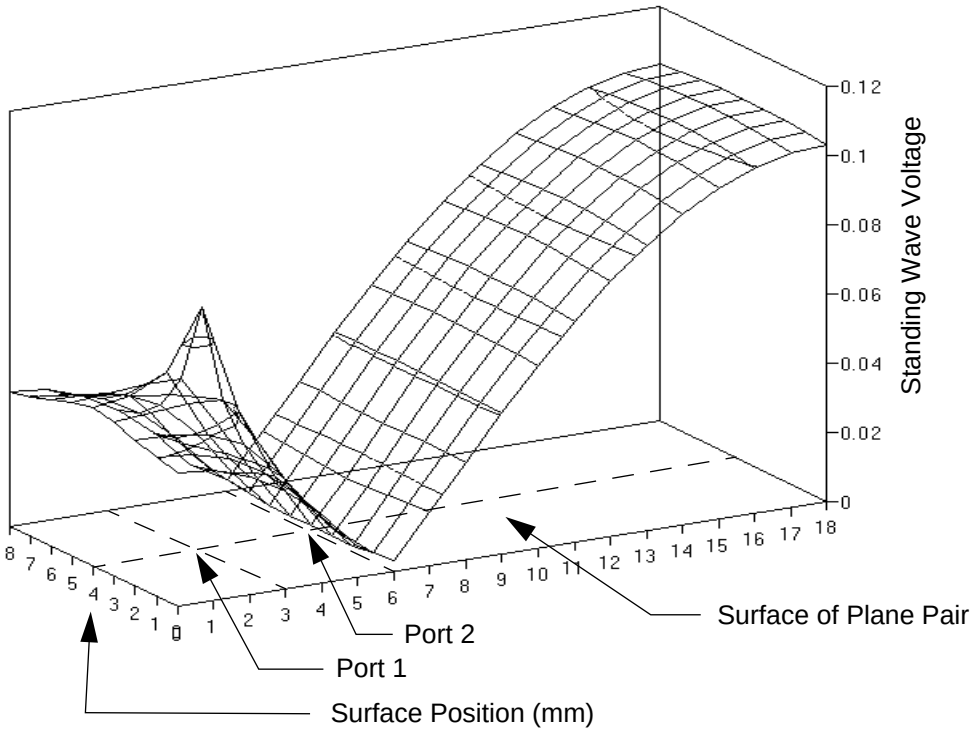


Figure 8. Standing wave pattern within plane pair driven at Port 1 at the frequency of the first null of Figure 7 (2.15 GHz).

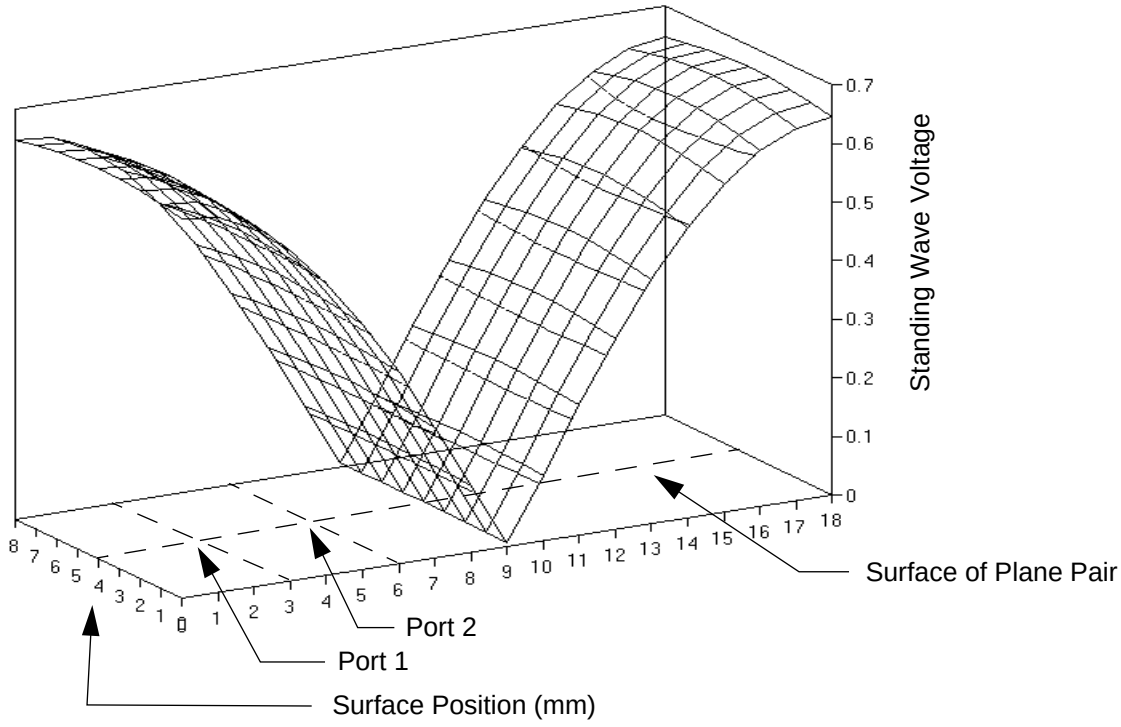


Figure 9. Standing wave pattern within plane pair driven at Port 1 at the frequency of the first peak of Figure 7 (2.9 GHz).

4 Thin film test module

The frequency response of power supply planes of a membrane probe was measured and compared with the calculated response of an MDS model. The membrane probe [Barb94] is made with Cu/polyimide thin film technology and has four metal layers: pad, signal, GND, and split VDD. Figure 10 schematically shows the shape of the split VDD plane. The planes are made with 9 mΩ/sq. copper and the dielectric is 3.5 μm thick polyimide with a relative dielectric constant of 3.5. The membrane probe has an array of contacting bumps in the center area and a diced chip is pressure contacted

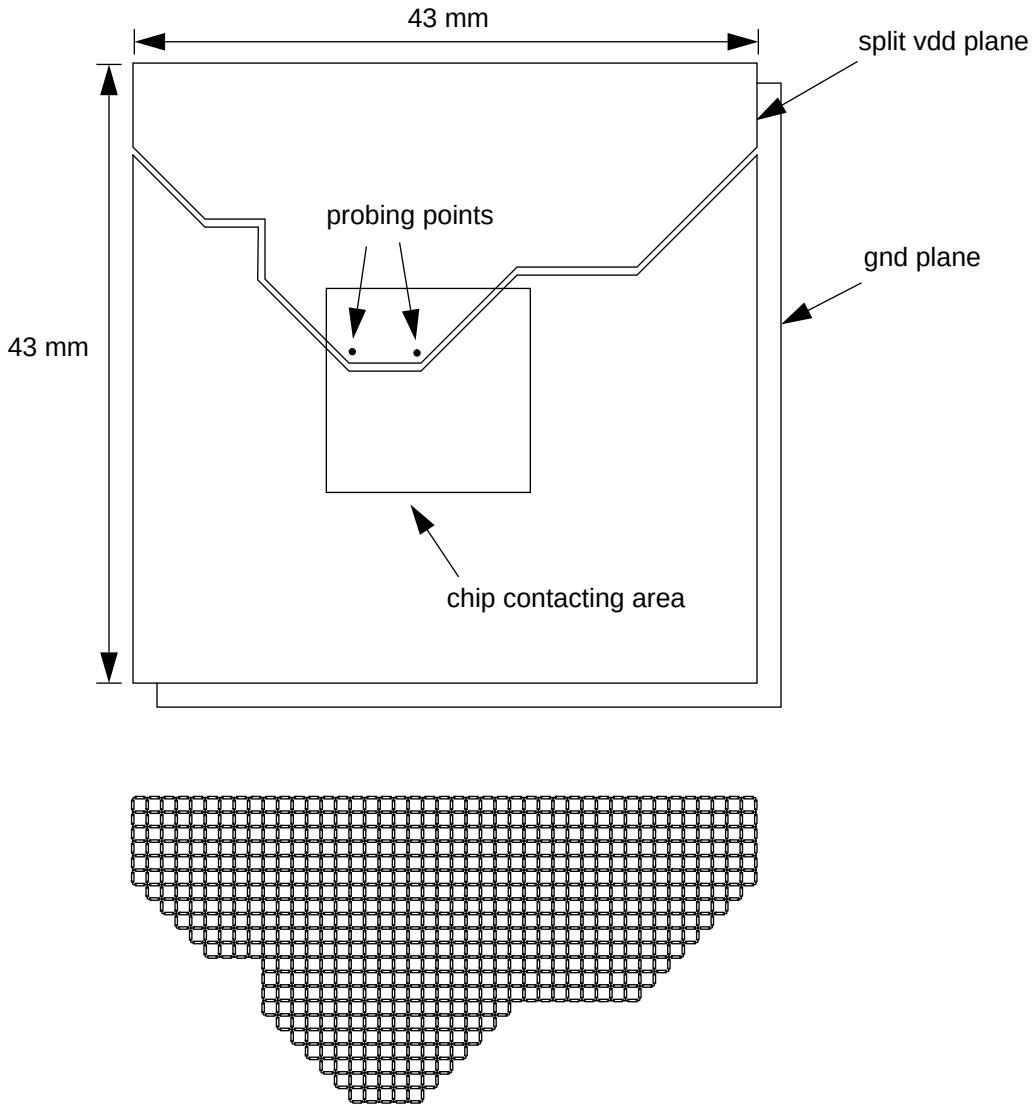


Figure 10. Thin film substrate. The planes are made with 9 mΩ/sq. copper and the dielectric is 3.5μm thick polyimide with a relative dielectric constant of 3.5. The equivalent circuit with lossy transmission line is shown at the bottom.

for high speed probing. The frequency response of the power supply plane of this thin film structure was measured by probing a VDD bump in the chip contacting area with reference to an adjacent GND bump while no chip is attached to the membrane. By probing two VDD pads with reference to two adjacent GND pads simultaneously, two-port s-parameters were measured using an HP8510C. Probing the chip contacting pads allows us to measure the frequency response of the power supply planes exactly in the same environment as an active chip sees it when it is being tested on the membrane probe.

The corresponding MDS model is shown in Figure 10. Each segment of the MDS model is a 1 mm long lossy transmission line like shown in Figure 4. The values of the transmission line parameters are as follows.

Z = 0.996 Ω
l = 1 mm
V = 0.756
R = 0.018 Ω/mm
G = 0 Sie/mm
F = 1.14 GHz

Two 130 μm long lossy transmission lines with the following parameters are included in the model between plane probing points and 50 Ω ports in MDS because there are 130 μm long traces connecting the planes and probing bumps on the membrane probe.

Z = 50Ω
l = 0.130 mm
V = 0.535
R = 0.5 Ω/mm
G = 0 Sie/mm
F = 1.14 GHz

Figure 11 shows the measured and simulated s-parameters. The simulation matches the measurement very well except for S_{11} above 10 GHz. The excessive loss in the measurement compared to the simulation may be due to the frequency dependent dielectric loss which was not included in the model. The same data is shown on a Smith chart in Figure 12. S_{21} is too small to be plotted properly in the scale, but S_{11} shows inductive phase angles. The deviation between the measured and modeled S_{11} is again above 10 GHz as shown in Figure 11. It is found that the inductive behavior of S_{11} is due to the 130 μm long lossy transmission lines. A simulation without the short transmission lines, which is the response of the plane pair itself, is shown in Figure 13. It shows almost no deviation in phase from an ideal short. Unlike S_{11}, the difference in S_{21} with and without the short transmission lines is minimal.

The membrane probe has a site for a bypass capacitor connecting VDD and GND on the segmented plane and the measured s-parameters with a bypass capacitor attached on the membrane is shown in Figure 14. As discussed in the following sections, the bypass capacitor has less effect on the frequency response of power

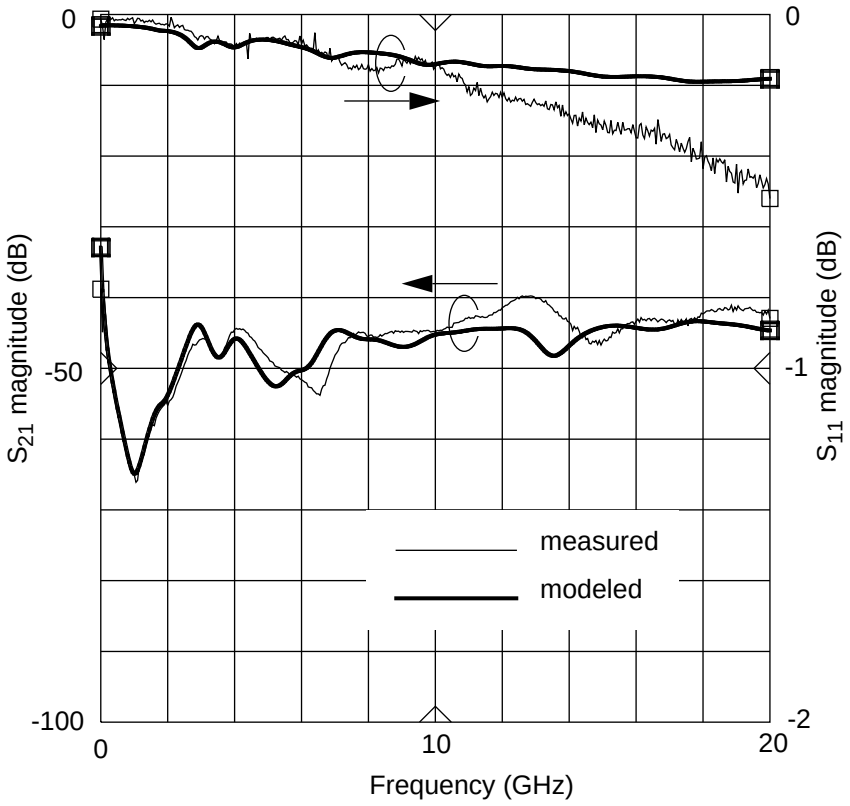


Figure 11. Measured and modeled s-parameters of thin film substrate.

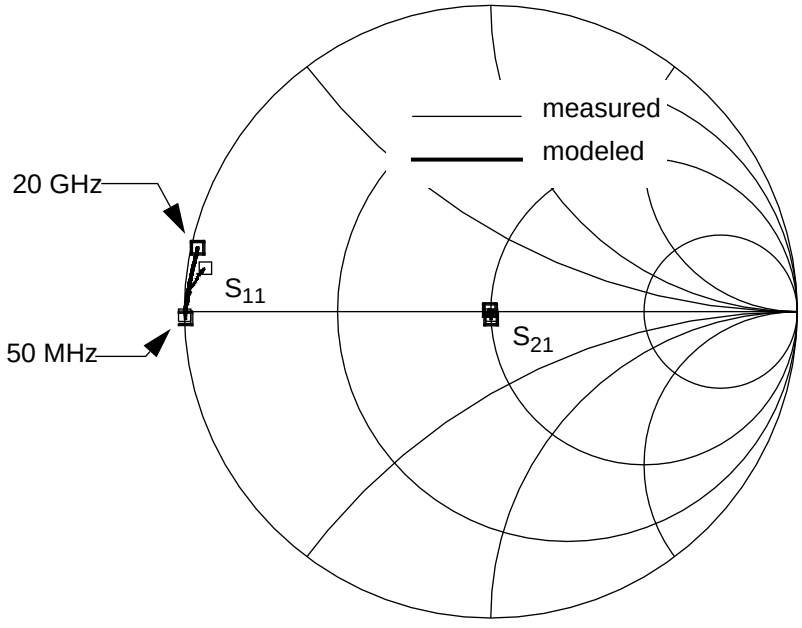


Figure 12. Measured and modeled s-parameters of thin film substrate.

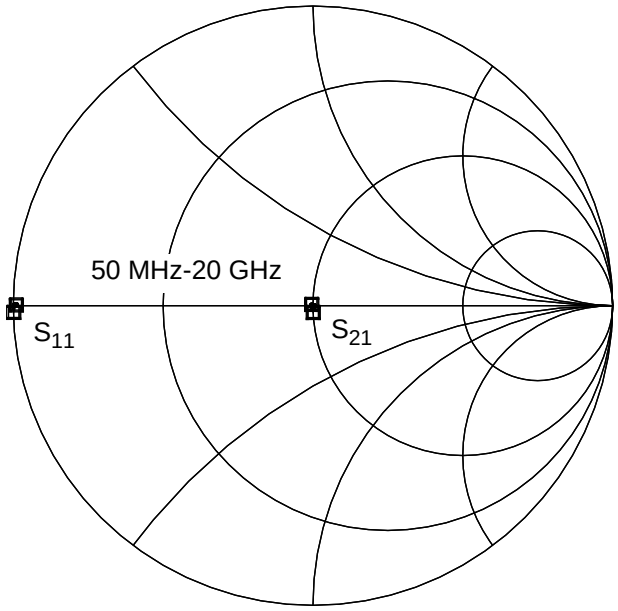


Figure 13. Modeled s-parameters of thin film substrate - Plane only.

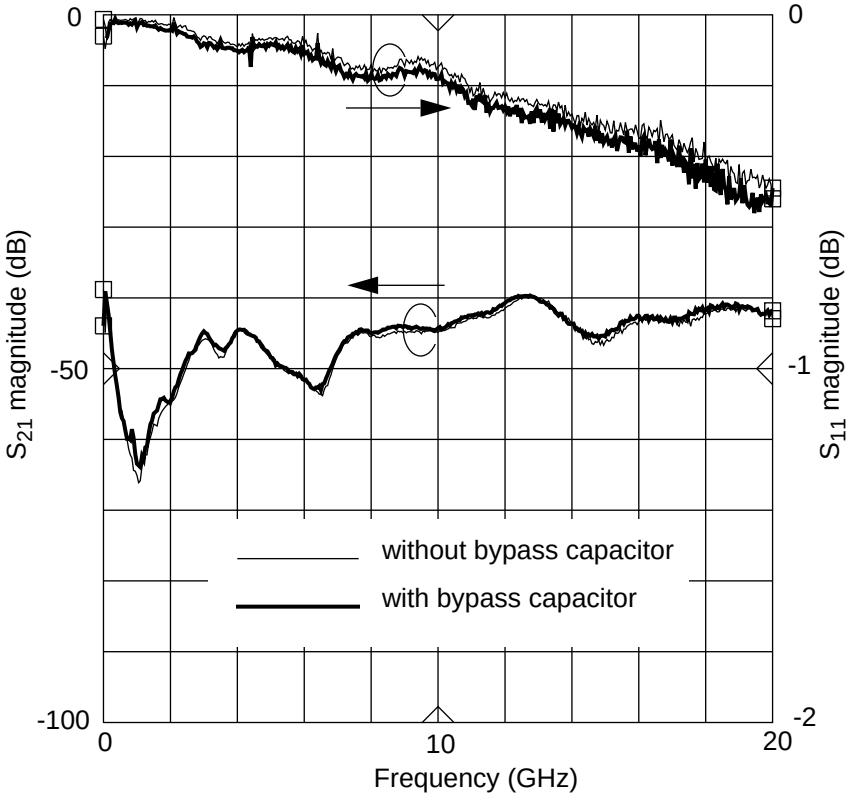


Figure 14. Measured s-parameters of thin film substrate with and without a bypass capacitor.

supply planes as the dielectric thickness between the planes becomes thinner. In this membrane probe case, the dielectric thickness is so thin (3.5 μm) that the measured data show no difference in the frequency range of 50 MHz-20.05 GHz.

This thin film measurement and modeling prove that the newly developed plane model is very accurate for the power supply planes with a very thin dielectric layer.

5 Comparison of thick film and thin film

A comparison of the S_{21} results of Figures 7 and 11 suggests that a thin film power distribution network may have inherent advantages over a thick film one. That this is so seems intuitive if one imagines a planar structure of power and ground as a low impedance transmission line interconnecting devices, as in Figure 1(b). As one device injects current into the power and ground network the voltage magnitude appearing across the planes, and propagating to neighboring devices, will be proportional to the impedance presented. This impedance in turn is dependant on the dielectric thickness; thin film structures with a thin dielectric have less inductance and more capacitance, and thus lower impedance, than structures with thick dielectric. This simple picture is complicated by reflections from edges and the presence of bypass capacitors, so it is instructive to explore these effects further.

A plane pair arranged as in Figure 15 was used for this purpose. Only the transmission line parameters were kept different for the thin and thick film cases:

	Thin Film	Thick Film
Physical Parameters		
Dielectric Thickness	15 μm	280 μm
Dielectric Constant	3.5	9.6
Perforated Plane Coverage	43.8%	100%
Element Electrical Model Parameters		
Z (characteristic impedance)	3.539 Ω	47.58 Ω
l (length)	1.0 mm	1.0 mm
V (relative propagation velocity)	0.756	0.457
R (DC series resistance)	0.032 Ω/mm	0.02 Ω/mm
G (shunt conductance)	0 Sie/mm	0 Sie/mm
F (skin effect frequency)	0.203 GHz	0.10 GHz

Table 1. Thin and Thick Film Comparison Parameters.

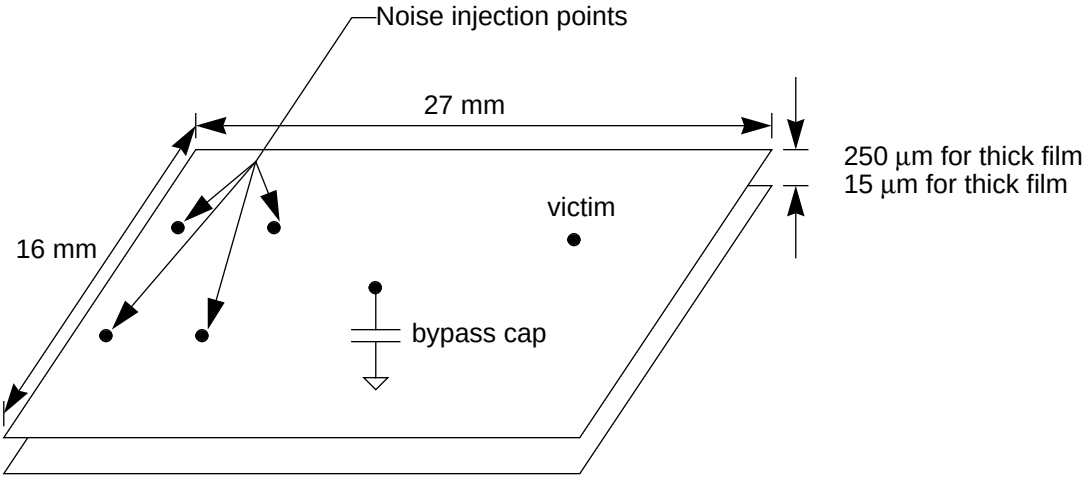


Figure 15. Substrate layout used to study noise propagation properties of thin film and thick film structures.

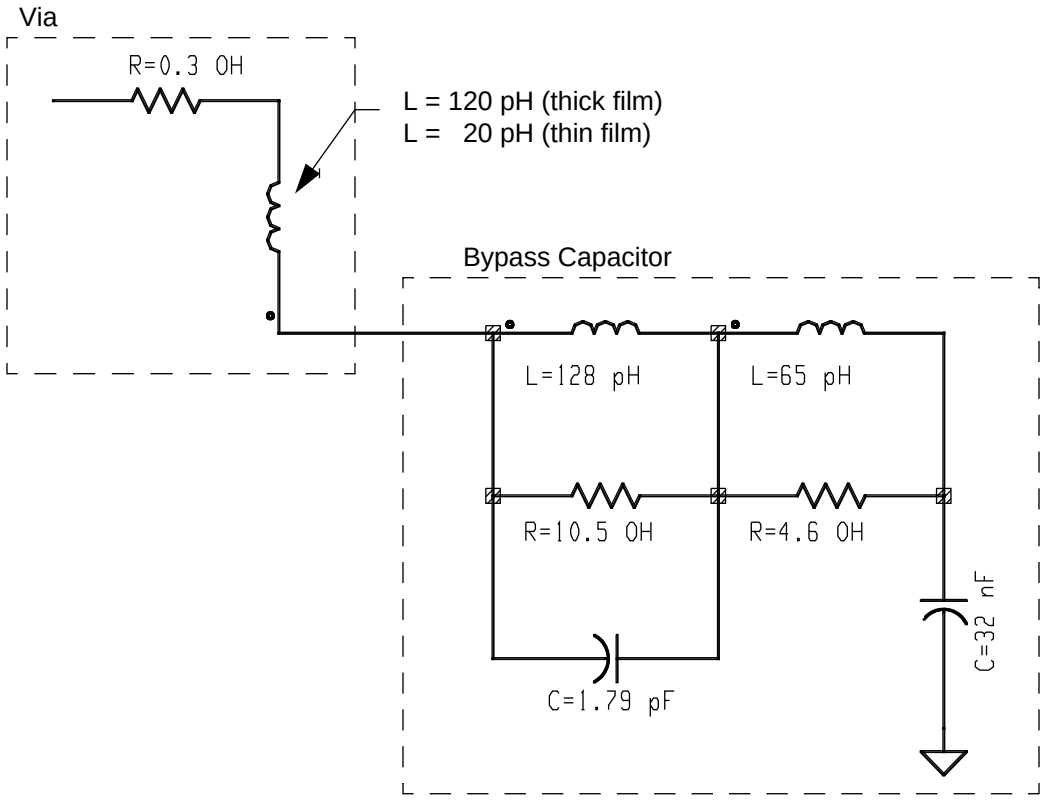


Figure 16. Equivalent circuit for the bypass capacitor of Figure 15.

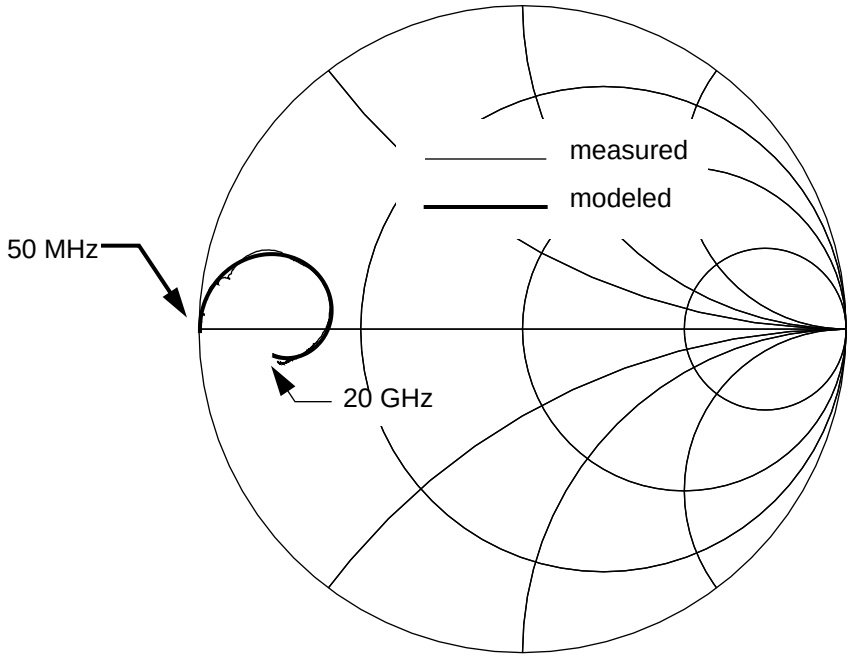


Figure 17. Modeled and measured results of bypass capacitor S_{11}.

A bypass capacitor of 32 nF was placed between the victim and the noise injection points. The model for this capacitor was derived by "guessing" a circuit configuration and then fitting component values to optimize the match between measured and simulated S_{11} response of an actual bypass capacitor. The capacitor chosen was a "LICA" model from AVX Corporation and has solder bump terminations [Beke93]. The resulting model is shown in Figure 16. The measured and simulated values of S_{11} are shown in Figure 17. The model differs between the thick and thin film case only in the value of the via inductance as shown because of the longer length via in the thick film case. Noise was injected into the plane pair at the points indicated in Figure 15 by shorting the four points together and driving with a 50 Ω source. The resulting noise was measured by sensing the voltage across the planes at the "victim" point with a 50 Ω load. The magnitude of this transfer function, S_{21}, is shown in Figure 18 for both the thin film and thick film case. The values track very closely at very low frequencies, up to about 300 MHz, then diverge sharply with the thin film performance about 20 dB better at most frequencies. At low frequencies the performance is determined by the voltage divider effect between the 32 nF bypass capacitor and the source impedance. At higher frequencies the distributed nature of the planes dominates. Less energy is coupled into the thin film plane pair because of its lower impedance relative to the 50 Ω source impedance of the measurement.

Likewise in the time domain, for slow risetimes the performance of the thick and thin film structures is about the same but for fast risetimes less energy is coupled into the thin film structure. This is indicated by the results of SPICE modeling using this model with a fast (100 psec) and a slow (3200 psec) risetime edge, shown in Figure 19.

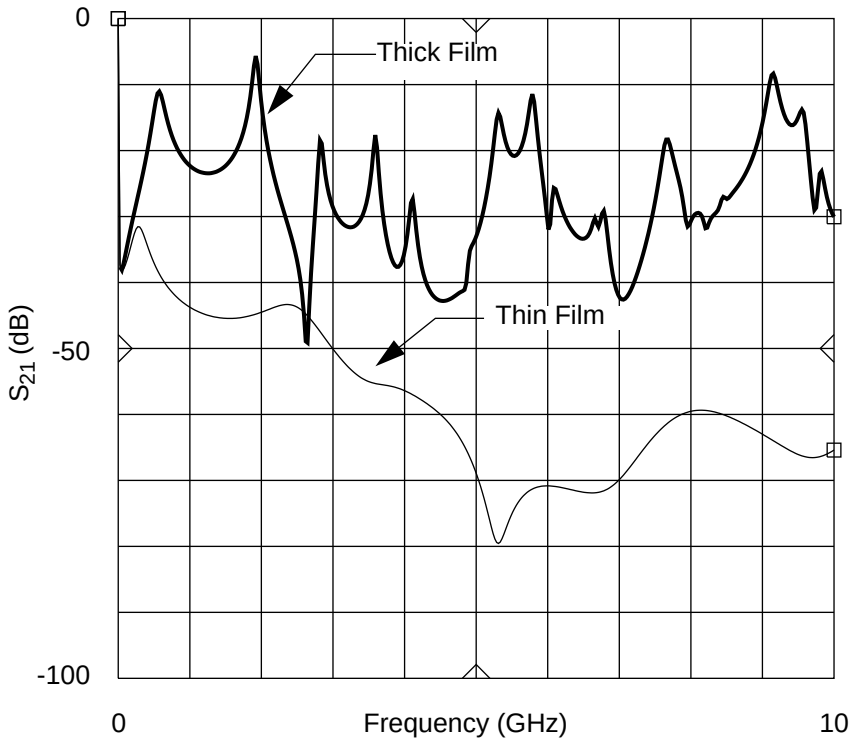


Figure 18. Coupling between noise injection points and victim in circuit of Figure 15.

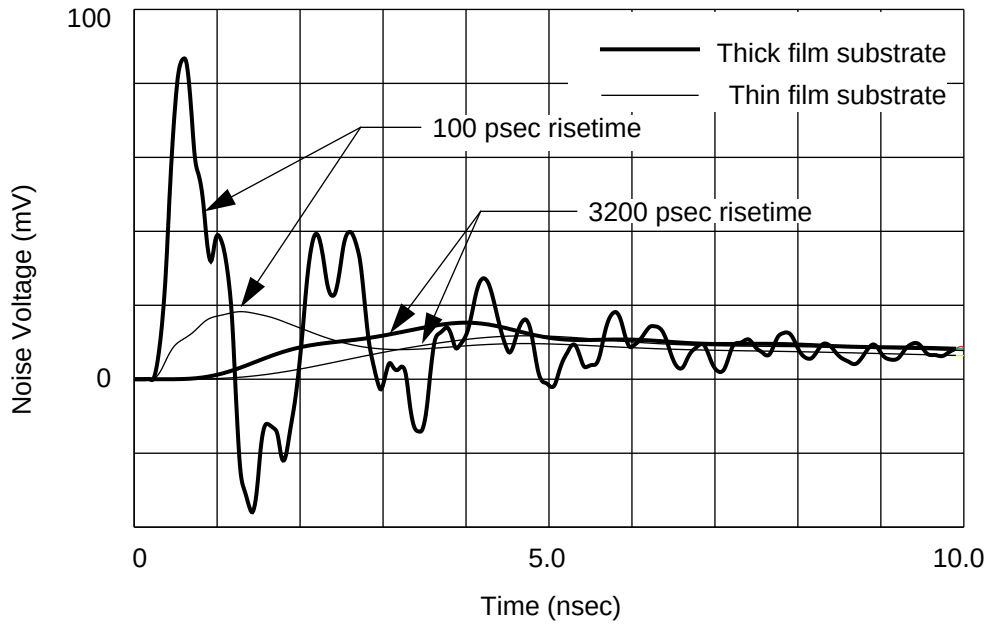


Figure 19. Waveforms of resulting noise at victim position due to injected pulse edge (Figure 15).

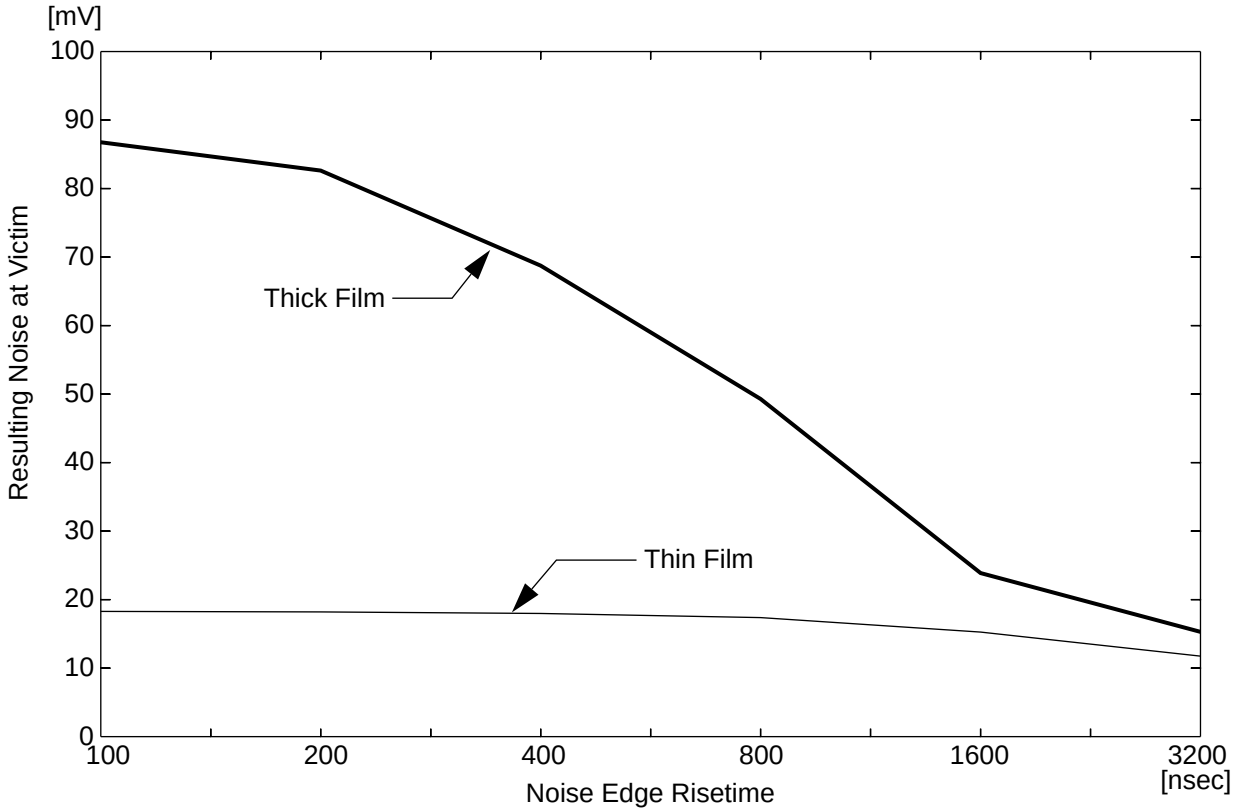


Figure 20. Noise induced at victim position (Figure 15) due to 1 volt injected noise of indicated risetime.

At 100 psec risetime the resulting noise at the victim position is over three times as great in thick film as in thin film, and roughly equal at 3200 psec risetime. Figure 20 shows that the largest increase in victim noise occurs as risetimes decrease below 1000 psec.

6 Simulation of a 19-chip thin film module

Using the modeling methodology discussed in the previous sections, the power supply performance of a large MCM design shown in Figure 21 was simulated. The purpose of this exercise was to predict the noise on the power supply when all the drivers on the proposed MCM switch simultaneously. The MCM substrate has two pairs of VDD/ GND planes, one in thin film and the other in thick film. A case where the MCM has only the thick film plane pair was also examined. The electrical characteristics of these two plane pairs in terms of the parameters of a lossy transmission line cell are shown in Table 2.

	Thin Film	Thick Film
Physical Parameters		
Dielectric Thickness	15 μm	90 μm
Dielectric Constant	3.5	5.0
Perforated Plane Coverage	43.8%	30.6%
Element Electrical Model Parameters		
Z (characteristic impedance)	3.539 Ω	29.60 Ω
l (length)	1.0 mm	1.0 mm
V (relative propagation velocity)	0.756	0.633
R (DC series resistance)	0.032 Ω/mm	0.020 Ω/mm
G (shunt conductance)	0 Sie/mm	0 Sie/mm
F (skin effect frequency)	0.203 GHz	0.043 GHz

Table 2. Thin and Thick Film Comparison Parameters.

All the planes are mesh planes with a mesh pitch of 100 μm for the thin film and 450 μm for the thick film. Since the mesh pitches are much smaller than the wavelengths of interest, the characteristic impedances were calculated from static three-dimensional capacitance calculations which include the fringing fields in the mesh planes.

Because the impedance of the thick film is almost an order of magnitude larger than thin film, simulations showed that the thick film plane pair does not contribute to the high frequency performance of the MCM power supply. Therefore only the thin film model was used for simulations when both thin and thick film plane pairs exist in the MCM. Only a quarter of the MCM was simulated as shown in Figure 22, exploiting the symmetry which is true for the case when all the drivers switch simultaneously.

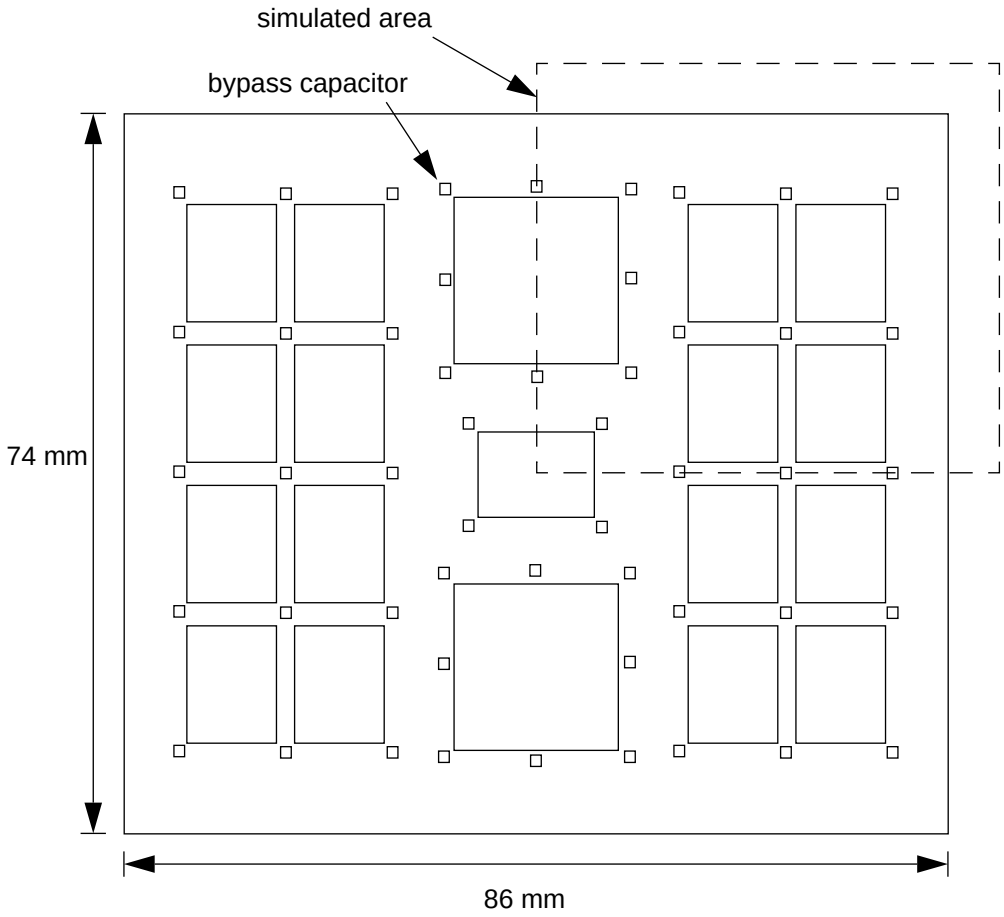


Figure 21. 19-chip MCM. Two large chips have 380 drivers each and 17 small chips have 45 drivers each. Substrate has one vdd/gnd pair of thin film planes and one vdd/gnd pair of thick film planes.

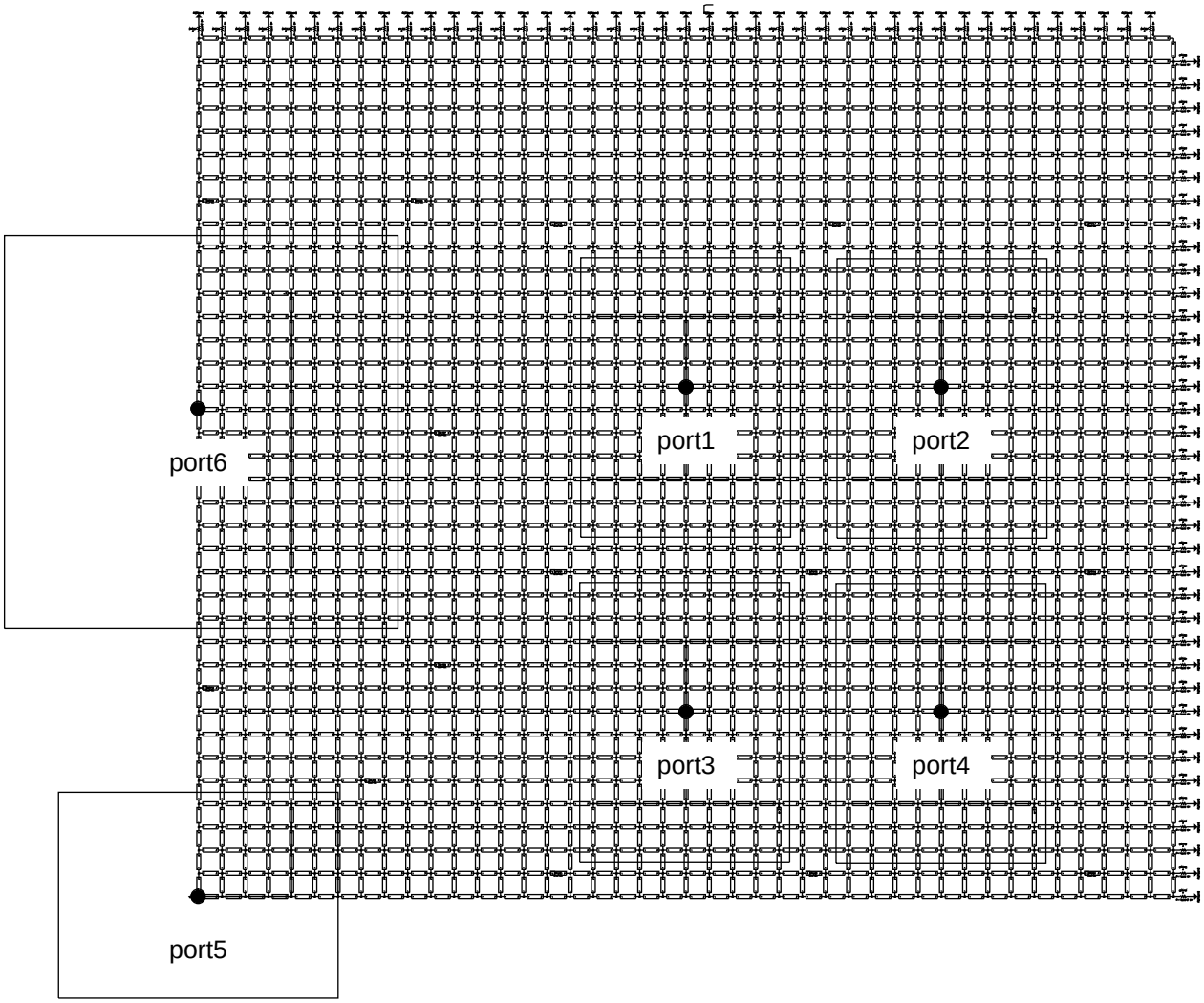


Figure 22. Plane model of 1/4 of 19-chip MCM.

The model also includes bypass capacitors as shown in Figure 21. Instead of a lumped equivalent circuit model of the capacitor, its measured s-parameter was directly used on the MDS plane model. Six ports were defined on the six chip sites as shown in Figure 22 and 6×6 s-parameters for a frequency range of 50 MHz - 10.05 GHz were calculated with a 50 MHz interval. The module boundary was assumed to be an open circuit for the frequency range and the DC values of the s-parameters were calculated with the module boundary shorted to the ground. This simulates a case where the power supply to the module has a very low DC impedance but has a very high AC impedance. Simulations showed that it is a valid assumption, since for the DC to mid frequency range the bypass capacitors on the module dominate over any effects from the boundary and for the high frequency range the boundary has much higher impedance than the plane.

Using SSPICE, each port of this 6-port s-parameter model was connected with a CMOS driver and a current-dependent current source which represents the simultaneously switching drivers on the same chip. The two large chips have 380 drivers each and the 17 small chips have 45 drivers each. A 50 Ω load was connected on the output of each driver in the simulation.

Figure 23 shows the calculated noise on the power supply and the output waveform of a driver on each chip when all the drivers switch simultaneously on the MCM with the thin film power planes. Port 6, where a large chip is connected, suffers the largest

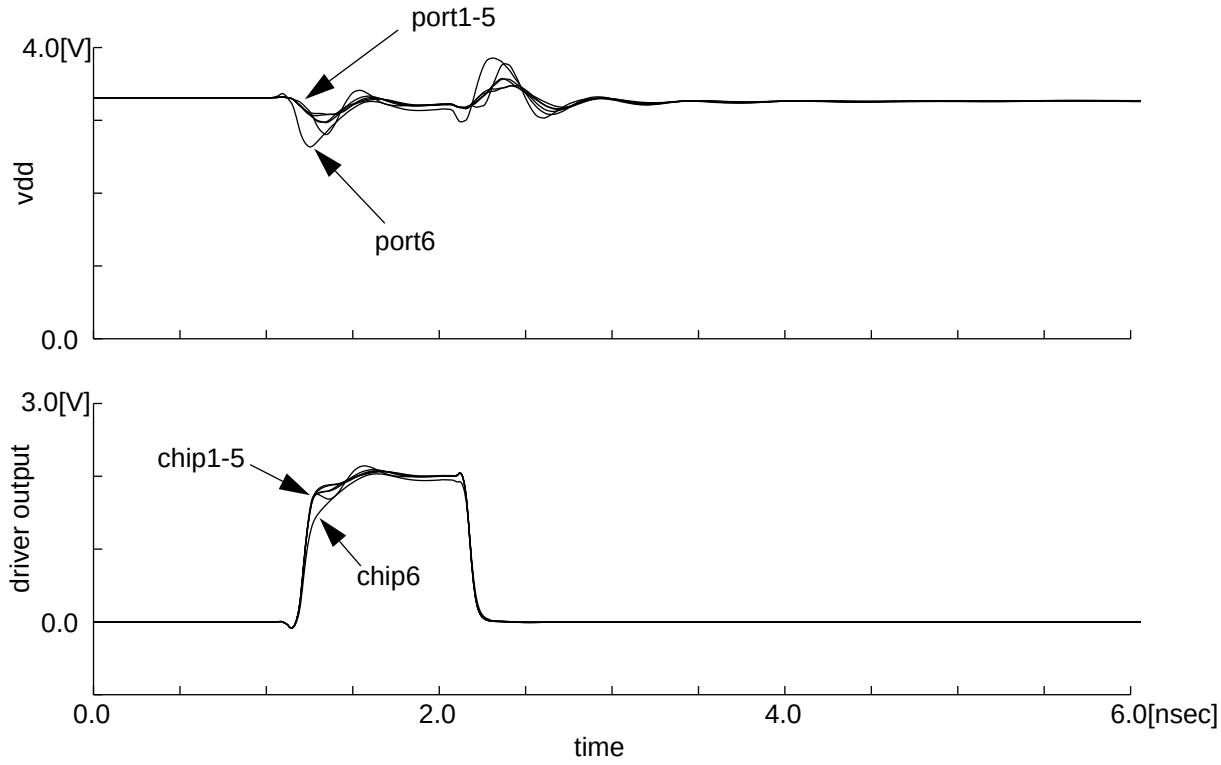


Figure 23. VDD noise and driver outputs of 19-chip MCM with thin film power planes.

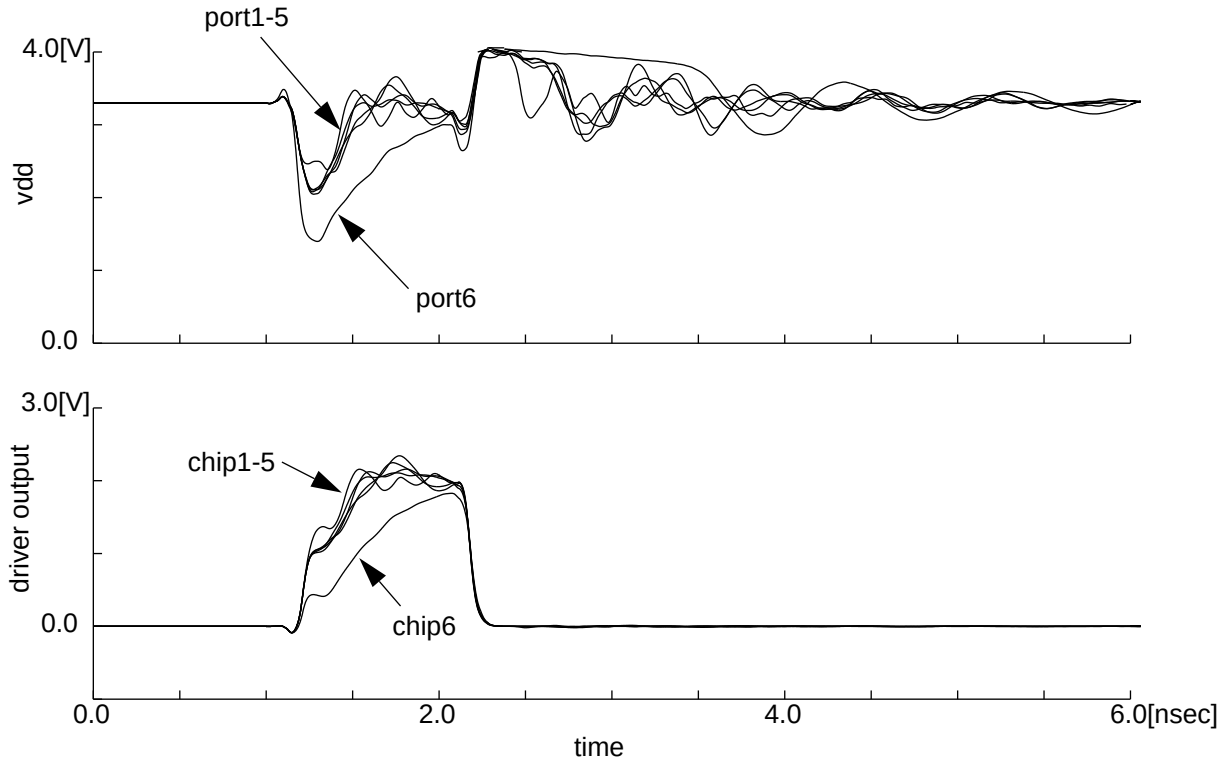


Figure 24. VDD noise and driver outputs of 19-chip MCM with thick film plane pair only.

noise. The VDD spike also causes the distortion on the output waveform. Figure 24 shows the same simulation for the case where the MCM has only the thick film plane pair. The VDD spike is unacceptably large and the output signals do not carry the correct logic levels.

Since these VDD spikes in the thin and thick film planes are due the impedance associated with the planes, adding more capacitors on the module does not reduce the noise. The only way to reduce the noise is to introduce an on-chip capacitor before the power connections of the chips see the planes. The effect of the on-chip bypass capacitor is shown in Figure 25 and Figure 26 where a 25 pF on-chip bypass capacitor is connected on each CMOS driver. For both thin and thick film cases, the spikes on VDD are filtered effectively by the on-chip bypass capacitors. However, the noise is still excessive for the thick film case. It was found that for the simulations with the on-chip bypass capacitors, a non-distributed model (inductor/resistor mesh only without capacitor) can simulate the noise quite accurately because the fast edges on the VDD spikes have already been filtered by the on-chip bypass capacitors before they arrive at the planes.

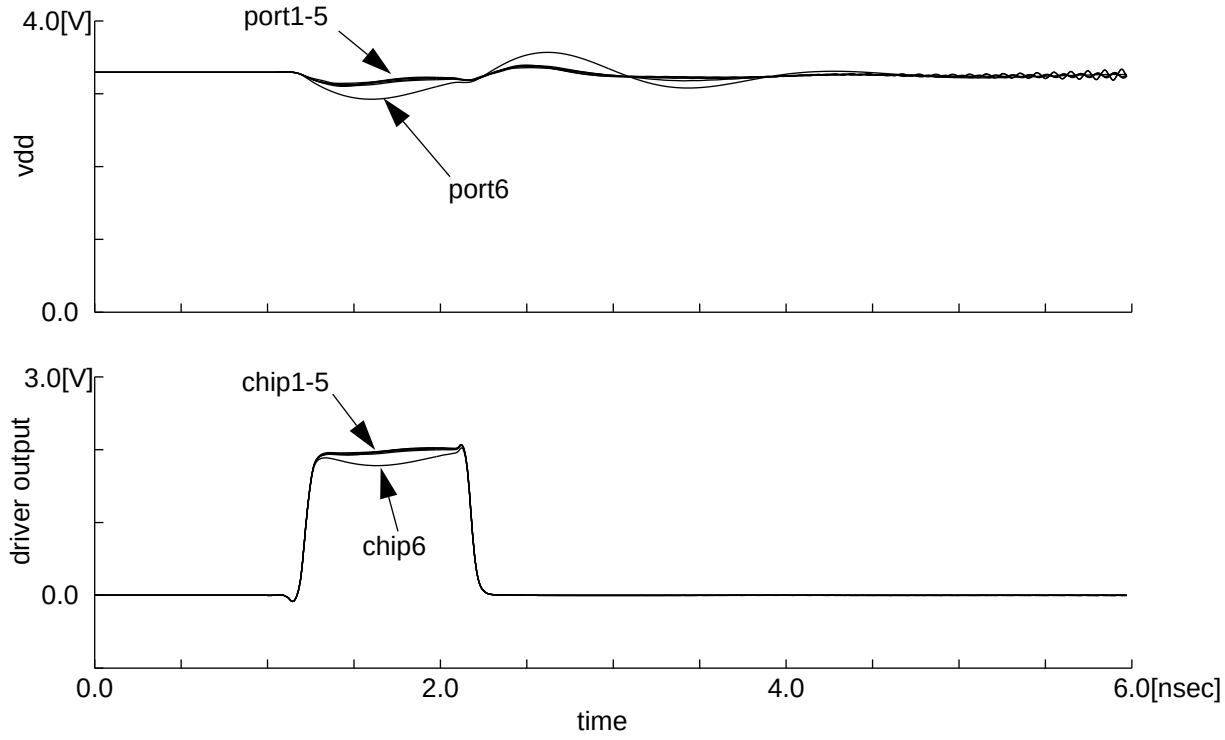


Figure 25. VDD noise and driver outputs of 19-chip MCM with thin film power planes and with on-chip bypass capacitors.

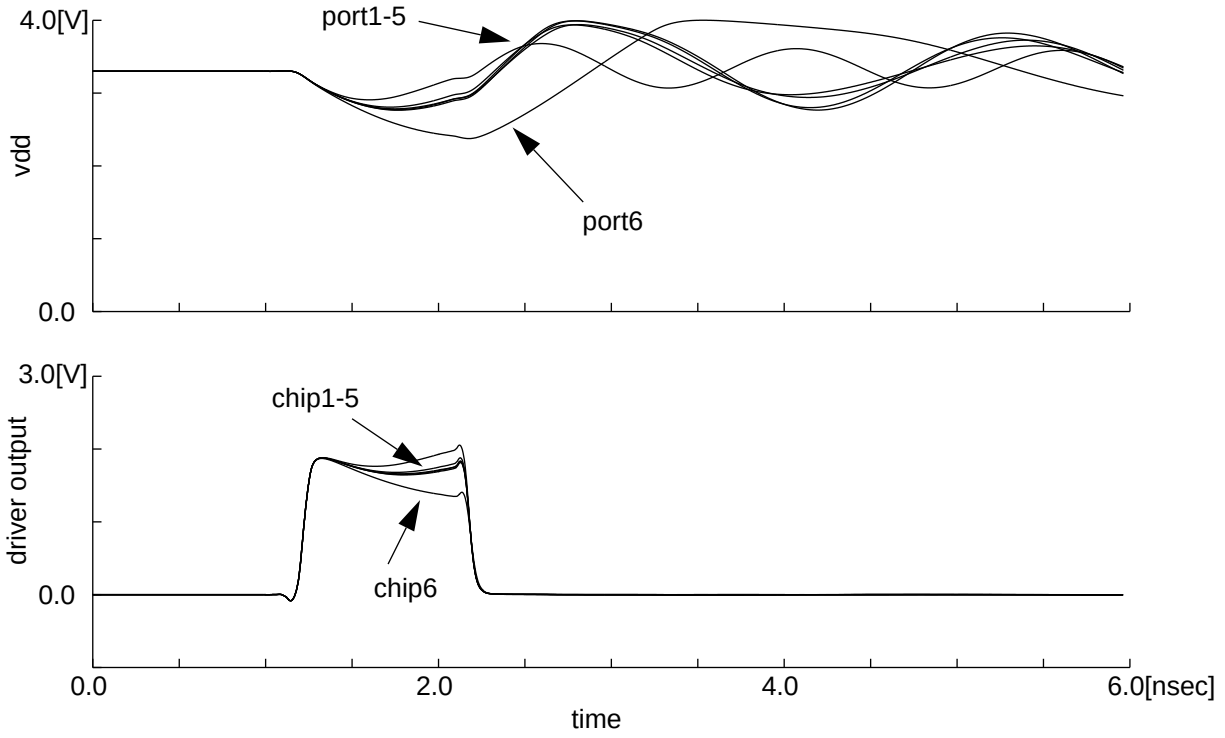


Figure 26. VDD noise and driver outputs of 19-chip MCM with thick film plane pair only, but with on-chip bypass capacitors.

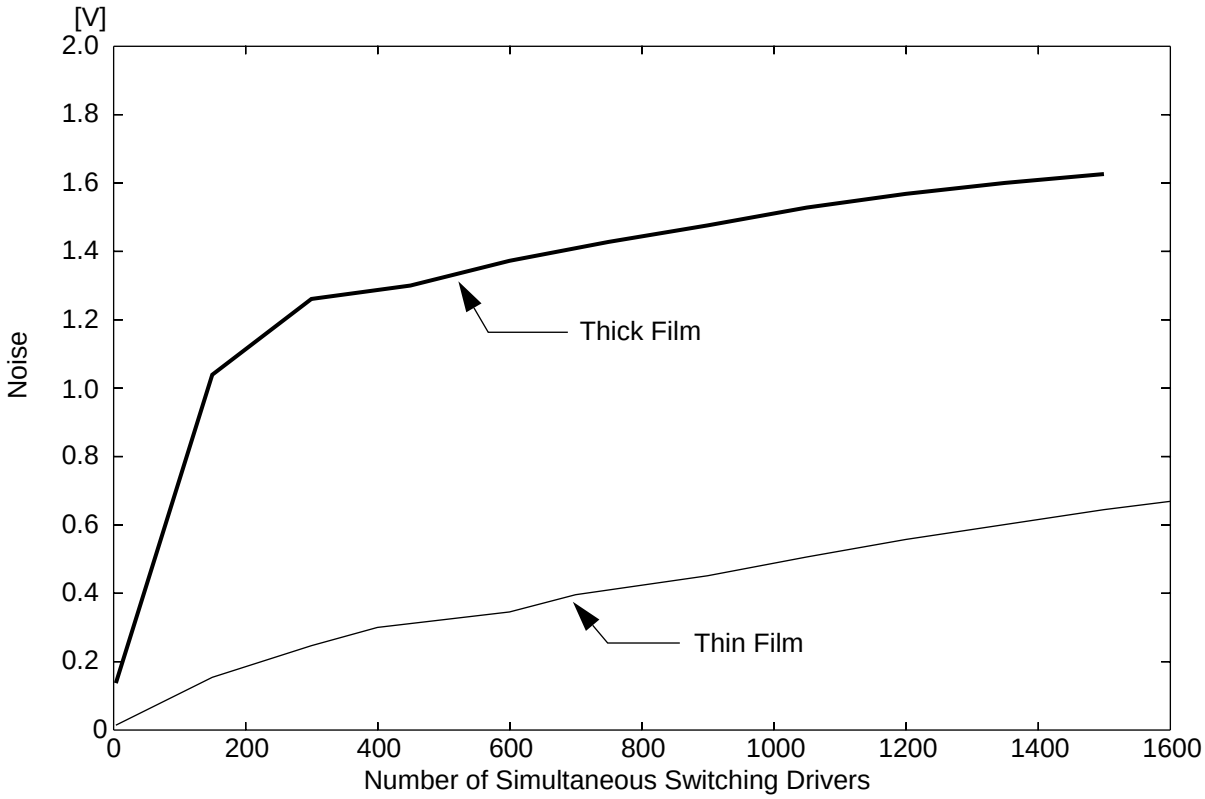


Figure 27. Noise on VDD vs. number of simultaneous switching drivers.

Figure 27 shows the power supply noise with respect to the number of simultaneously switching drivers on the MCM when the on-chip capacitors are used with the thin and thick film planes. The curve for the thick film saturates at near 300 drivers because of the negative feed back effect of the driver reported in [Sent91]. Figure 27 clearly shows that the thick film substrate imposes a severe limitation on the number of simultaneous switching drivers on the MCM compared to the thin film substrate.

7 Conclusions

It is possible with existing tools to build accurate models of planar power distribution systems. We have proved the accuracy of the models with the frequency domain measurements of the thick and thin film planes which are commonly used in MCM substrates. These models can be used in time domain simulations in combination with the existing SPICE models of active circuits using SSPICE, which is a modified SPICE with an s-parameter circuit model. This time domain simulation methodology can in turn be used to predict the simultaneous switching noise in large MCM's and the effects of the on-chip and off-chip bypass capacitors.

Acknowledgment

The authors would like to thank Dan Miller of Computer Peripherals Lab, HP Laboratories for the design and fabrication of the thick film test substrate.

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