Defect Analysis of Roll-to-Roll SAIL Manufactured Flexible Display Backplanes

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HP Laboratories
HPL-2011-35

Keyword(s):

SAIL, flexible displays, roll-to-roll

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External Posting Date: March 21, 2011 [Fulltext] Approved for External Publication
Internal Posting Date: March 21, 2011 [Fulltext]
To be presented at Device Research Conference, Jun. 20, 2011.

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Abstract
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1. Introduction
HP and Powerfilm have together been developing methods for fabrication of electronics on flexible substrates using roll-to-roll (R2R) processes for over 10 years. We have created the world's first R2R active matrix display using the Self-Aligned Imprint Lithography (SAIL) process [1]. SAIL has been used to fabricate both electrophoretic and OLED displays and amorphous silicon and metal oxide based backplanes have been demonstrated with the process [2-4]. We are currently developing small quantities of wrist-worn solar powered displays for the Army Research Laboratory. The production of these qqVGA displays is the first step in scaling the SAIL process from the lab to volume manufacturing. To achieve necessary yields we have developed tools for inspection and electrical test of flexible substrates that are not bonded to a carrier as opposed to other efforts which utilize a bond - debond method for fabricating flexible backplanes on rigid carriers using conventional flat panel tools [5]. The leading sources of defectivity fall into two categories: electrical defects in the thin films of the TFT (thin film transistor) and defects affecting the imprint lithography process.

Figure 1: 160X120 pixel e-Ink based display with500µm pixel pitch being developed for the Army

2. Self Aligned Imprint Lithography
The SAIL process was developed not only to make flexible displays but to enable low cost. We started with the single assumption that we would use R2R processes exclusively. The high level process flow for SAIL is shown on Figure 2. Unlike a conventional panel based process all of the deposition steps for the complete thin film transistor (TFT) stack are completed before any of the patterning steps. The multiple patterns required to create the backplane are encoded in the different heights of a 3D masking structure that is molded on top of the thin film stack once before any of the etching steps. By alternately etching the masking structure and the thin film stack the multiple patterns required for the backplane are transferred to the device layers. Because the mask distorts with the substrate perfect alignment is maintained regardless of process induced distortion.

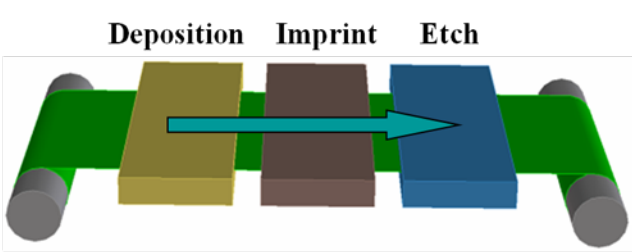


Figure 2: Schematic flow for SAIL

Figure 3 is an SEM image showing the 4 discrete heights in the mask used to produce bottom gate a-Si TFTs. Imprint lithography is ideally suited for R2R implementation because of its high resolution, compatibility with flexible substrates, high throughput and ability to reproduce complex 3-D structures. We have imprinted 40nm lines on 50µ thick polyimide and have developed materials that can maintain fidelity for thousands of impressions at throughputs of greater than 5m/min. Figure 4 shows transfer curves for 180 °C amorphous silicon TFTs produced with the R2R SAIL process. The curves are normalized by the W/L ratio of the devices to illustrate the scaling for channel lengths from 100μm to 1μm. At channel lengths below around 5μm the normalized on-current begins to drop due to the larger relative effect of resistance in the contacts. It is significant to note that while the on-current scales inversely with channel length, the speed of the TFT increases inversely with the square of channel length.

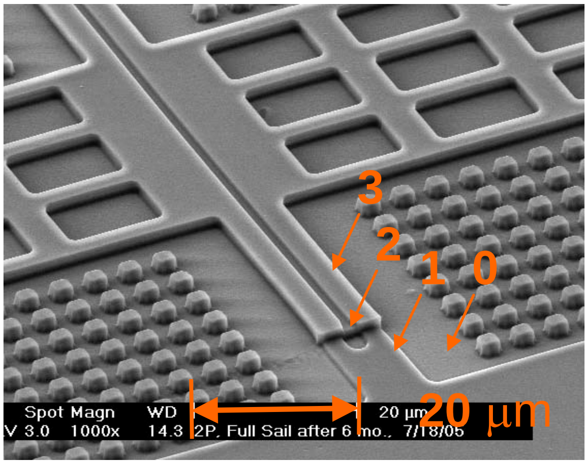


Figure 3: **4 level imprinted mask for active matrix backplane**

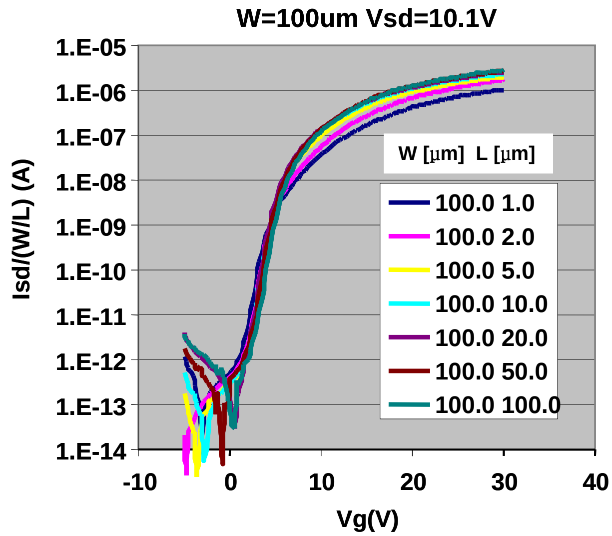


Figure 4: Transfer curves normalized to the W/L ratio for R2R fabricated SAIL amorphous silicon TFTs

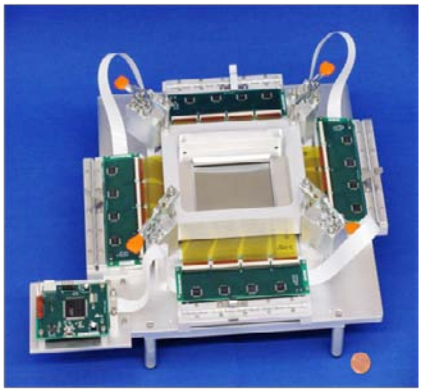
3. Fabrication

Our backplanes are fabricated on 50 μm thick 1/3 m wide polyimide films. The web is wrapped on 6" diameter cores and moved from one machine to another during processing, each machine having its own unwind and rewind station. All equipment has been built in-house or externally to our specifications. The full TFT stack is deposited using vacuum deposition equipment at PowerFilm Inc. The imprint polymer is coated and embossed on a coater/imprinter at HP Labs. The subsequent etch process which transfers the imprint mask into the TFT geometries are performed by in a R2R tank etch and RIE (Reactive Ion Etch) at HP Labs. The backplane arrays are then singulated, tested, and some simple defects such as shorts are repaired before laminating them with an E Ink frontplane.

4. Inspection and Electrical Test

We developed an electrical tester which uses bumped flex circuit contacts to connect to contact pads all sides of the backplane (Figure 5). The flex circuits are aligned to the backplane contacts through the use of alignment pins. Accurate alignment holes are cut in the substrate outside of the array near to the contact pads using a laser wafer dicer. A pressure ring applies even pressure around the array to ensure contact on all pads. Fixtures are included to facilitate loading and unloading the backplane under test without damage and to apply contact pressure repeatably. Compact electronics were built to obtain rapid test results. The system measures each data line and gate line for opens or shorts to common in less than 10 seconds.

It is necessary to perform R2R optical inspection both to evaluate the quality of the incoming substrate prior to processing and secondly to be able to study the evolution of defects during SAIL processing. Cutting samples from the web and imaging them with conventional inspection tools is not an option for two reasons. First, splices or holes in the web can interfere with further processing and second, once a sample is removed from the web the affects of the subsequent process steps cannot be studied. Figure 6 is a photograph of a R2R inspection tool that we have developed for inspection of the web at intermediate points in the process. The web is imaged by a microscope on the crown of a precision roller. The microscope can be scanned in the cross web direction.



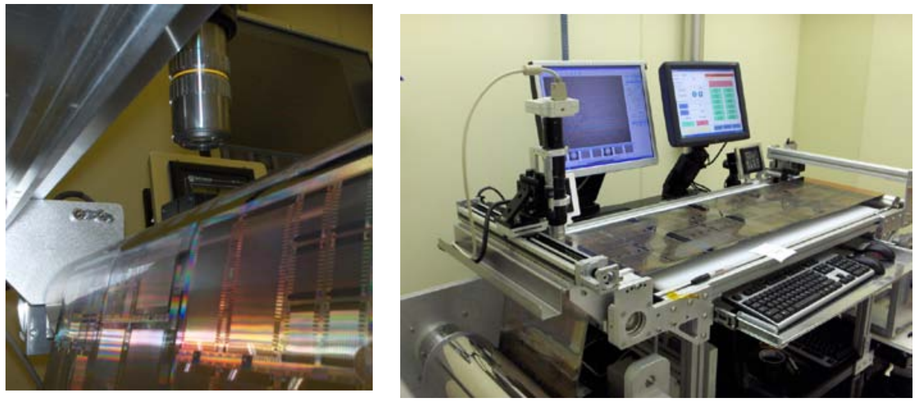


Figure 5: Flexible backplane electrical tester **Figure 6: R2R optical inspection system**

5. Defects

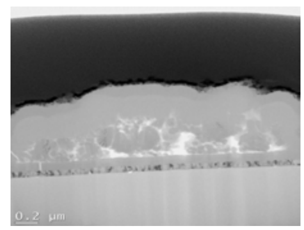


Figure 7: TEM of TFT stack with particle defect

Currently two of the most common defect types in the SAIL process are shunts and surface particles. A shunt is a low resistance path between the top and bottom metal in the TFT stack. In the SAIL process the TFT stack is used for all of the components of the pixel circuit including data lines, gate lines, and the hold capacitor in addition to the TFT. A shunt in any of these components can result at minimum in the loss of a pixel or possibly a row or column loss. Shunts can be caused by asperities in the substrate, irregularities in the sputter or CVD processes, or voids resulting from mechanical damage. Figure 7 is a TEM showing embedded particles in TFT stack that can lead to electrical failure.

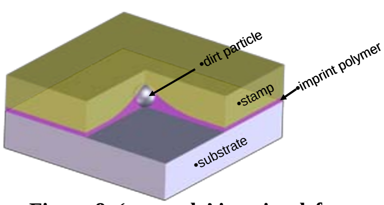


Figure 8: 'tent-pole' imprint defect

A second common defect occurs during the imprint process when the elastomeric imprint stamp is impinged onto the liquid photopolymer. This class of defects are generally referred to as 'tenting defects' because they produce a locally raised surface that deflects the imprint stamp (like a tent pole) creating an excess of photopolymer as shown on Figure 8. like a tent the area covered depends on the height of the pole so a relatively small particle can disrupt the pattern over a much larger area. In the SAIL process device layers are mapped to different thicknesses of the photopolymer masking structure so a significant change to the thickness of the masking layer (~0.7µm) can result in an incorrect mapping of the device layers. Typically this results in a short. Sources of tenting defects may be particles on top of the TFT stack, asperities within the TFT stack, or irregularities on the surface of the substrate. If the tenting is formed by a particle that remains on the web then the particle can acerbate the problem by masking subsequent etch processes or in some cases become adhered to the backside of the web as it is wound up then tear loose from its original location resulting in local delamination of the stack. Figure 9 shows the evolution of tenting defect through the SAIL process

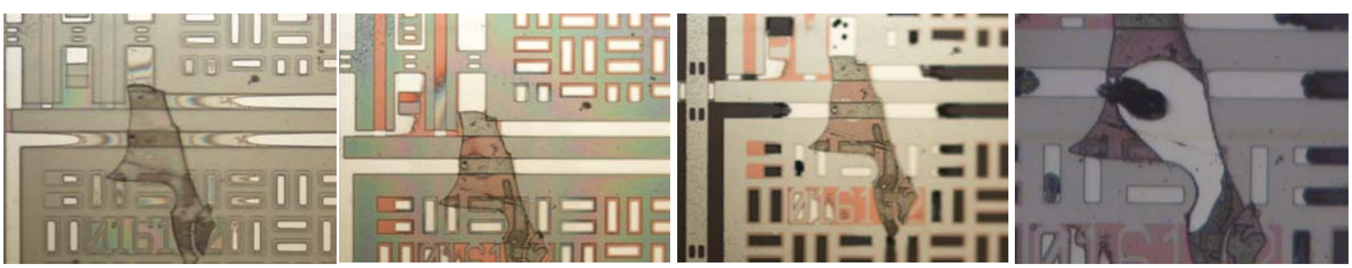


Figure 8: 'tent-pole' imprint defect results in tenting, micromasking and delamination. The evolution of the defect through the SAIL process starts at the left following the imprint, through the successive etch processes and finally adhesion and tearout on the right.

6. Acknowledgements

The authors gratefully acknowledge the support of their collaborators and sponsors including: the Army Research Laboratory (contract W911NF-08-2-0063), E Ink Corporation, and the ASU Flexible Display Center.

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