Design of efficient, virtual non-blocking optical switches

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optical switching, switch design

Large optical switches are made by connecting smaller switch arrays together, usually as three stage networks. This letter shows how three stage efficiency can be further improved, by allowing a negligible amount of blocking to exist. A simple design algorithm is also developed, which removes the need for long simulations.

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Abstract: Large optical switches are made by connecting smaller switch arrays together, usually as three stage networks. T his letter shows how three stage efficiency can be further improved, by allowing a negligible amount of blocking to exist. A simple design algorithm is also developed, which removes the need for long simulations.

Introduction: There is widespread interest these days in an all-optical core network layer for high speed data transmission. Such a layer could provide a world-wide backbone for an all-IP network, or for SDH and SONET based networking. This would enable high speed communication, operating in the 10s of Terrahertz range [1]. A major component in this network is the optical cross-connect switch. Efficient three stage (Clos) switches can be designed [2] which are completely non-blocking. However, extra savings in terms of the number of switch elements can be achieved by an internal routing algorithm which, although not completely non-blocking, will experience blocking so infrequently that the effect can be ignored (virtual non-blocking).

A 3 stage switch has the topology of Fig 1. The p outputs of the top input array are each connected to a separate stage 2 array, etc. For this design to be strictly non-blocking, the Clos condition $p \geq 2n-1$ [2] must be satisfied, where p and n are defined in Fig. 1. However, by allowing an extremely small amount of blocking, the number of stage 2 switches can be reduced, improving efficiency and reducing network cost. A major outcome was the development of a mathematical model, which removed the necessity for extremely long simulation runs at network deployment.

Simulation: A test case was run, with n = 16, q = 16. Random traffic was introduced on a random basis, using a discretised truncated Poisson model. The hold time for a call was chosen from a truncated gaussian distribution, such that the switch was loaded to about 95% capacity. A new call was always routed through the available stage 2 array nearest the top of the stage 2 stack of arrays (referred to as switch packing).

The simulation was monitored with varying values of p (with p = 31 necessary for Clos non-blocking). Starting with p = 22, the blocking probability $P_b(p)$ was calculated, allowing for about 50 blocking events to occur. Then p was increased (noting each P_b) until $P_b(p) < 10^{-5}$.

Theory: When $P_b(p) < 10^{-5}$, the simulation run time will be very long, and so a theory was developed for these cases of interest. When $Pb(p) \approx 10^{-5}$ or lower, it was found that when a switch packing blockage occurred, the bottom stage 2 array had only one connection path through it. This is because the packing strategy tries to use the top stage 2 array first for a new call, then the next array down, and so on. If the number of stage 2 arrays is increased by one, a blockage will still imply that the bottom array has only one non-zero entry. So the blocking probability $P_b(i+1)$ of i+1 stage 2 arrays can be related to the blocking probability $P_b(i)$ by a recurrence relation:

$$P_b(i+1) = P_b(i)[P(c)P(f|1)] \qquad (1)$$

where $P_b(i)$ is the switch blocking probability of i stage 2 arrays, P(c) is the blocking probability of the bottom stage 2 array that already has one call in progress, and P(f|1) is the conditional probability that the bottom stage 2 array will have one call in progress. P(c) can be found by a combinatorial calculation, and P(f|1) by an iteration of (1). For example, the simulation found $P_b(23) = 1.9e\text{-}4$ and $P_b(24) = 4.0e\text{-}6$. Also, a calculation gave P(c) = 0.121. Then (1) gives P(f|1) = 0.174. With P(c) and P(f|1) established, repeated use of (1) predicts the results shown in Table 1.

These values would be difficult to find by simulation, because of the very long run times involved. A six day simulation for v = 25 was run as a check. It gave $P_b(25) =$ 8.72e-8, which is close to the iterative result. Table 1 shows that virtual non-blocking can be achieved with 25 stage 2 arrays, whereas 31 arrays would be needed to satisfy the Clos condition. Assuming a rate of 1 call connection per day, there would be about 31,000 years between blocked calls. For this slight blockage, the design has reduced the number of stage 2 arrays by 19%.

Conclusion: The design consists of two parts. First, simulation runs are performed for a varying number of stage 2 arrays, until the blocking probability reduces to say 10^{-5}. With modern PCs, this part can be performed in a few minutes. It has been observed that when this level of blocking exists, the bottom stage 2 array is lightly loaded, and normally is handling just one call. The next part uses a simple iterative equation to predict blocking probability, using parameters gained from the simulation and combinatorial calculation.

The iterative results show a region of virtual non-blocking for the switch, which uses fewer arrays than the classic Clos result. The network designer can then choose the minimum switch size that will satisfy a realistic blocking probability specification.

References

1. Dettmer, R. 'Photons and petabits', IEE Review, July 2000, pp. 16-18.

2. Clos, C., 'A study of non-blocking switching networks', Bell System Technical Journal, March 1953, pp. 406-424.

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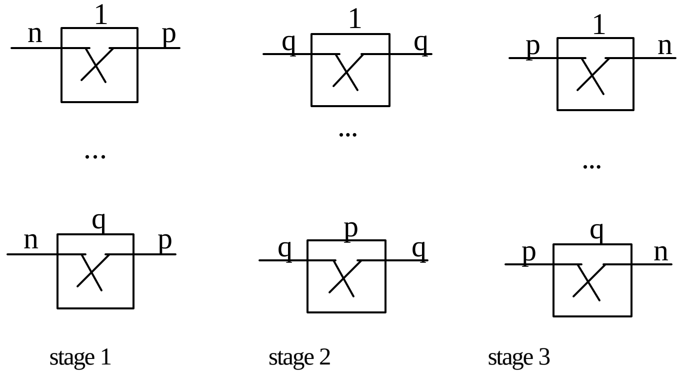

Fig. 1. The structure of an efficient three stage Clos switch

$v =$	25	26	27
$P_b(v) =$	8.4e-8	1.8e-9	3.8e-11

Table 1. Blocking probabilities for the example, as the number of second stage arrays is increased.