Interfacial Gate Resistance in Schottky-Barrier-Gate Field-Effect Transistors

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Abstract

We discuss in depth a previously overlooked component in the gate resistance R_g of Schottky-Barrier-Gate FETs, in particular 0.1-μm gate-length AlInAs/GaInAs MODFETs. The high-frequency noise and power gain of these FETs depends critically on R_g. This has been the motivation for the development of T-gates which keep the gate finger metallization resistance R_{ga} (proportional to the gate width W_g) low, even for very short gate length L_g. R_{ga} increases with frequency due to the skin effect, but our 3D numerical modeling shows conclusively that this effect is negligible. We show that the always "larger-than-expected" R_g, is instead caused by a component R_{gi} which scales *inversely* with W_g. We interpret R_{gi} as a metal-semiconductor *interfacial* gate resistance. The dominance of R_{gi} profoundly affects device optimization and model scaling. For GaAs and InP based SBGFETs there appears to exist a smallest practically achievable normalized interfacial gate resistance r_{gi} on the order of 10^{-7} Ωcm^2.

1. Introduction: Evidence of a Residual Gate Resistance Component

The gate resistance R_g has long been recognized as a parasitic parameter that degrades the noise figure and limits the power gain of Schottky-Barrier-Gate (SBG) FETs (MESFETs and MODFETs). The gate metallization resistance clearly contributes to R_g [1,2]. It does so in a distributed way, which reduces the effect to a third of the end-to-end gate finger resistance:

$$R_{ga} = \frac{r_{ga} W_g}{3 N_f^2}.$$

(1) To distinguish this well-known resistance from the additional component which is the

topic of this paper, we have introduced the subscript *a* to indicate *a*ccess resistance along the gate finger. r_{ga} is the normalized end-to-end gate metallization resistance given by

$$r_{ga} = \frac{r}{A_{gx}},$$

(2)

where ρ is the gate metal bulk resistivity, and A_{gx} is the gate cross-sectional area. W_g is the total gate width, and N_f is the number of parallel fingers that make up the gate. As the gate length L_g is shrunk to deep sub-micron dimensions it is customary to limit the increase in r_{ga} by using a T-shaped cross section, and to increase the number of parallel gate fingers [3]. Skin effect will introduce frequency dependence in the AC gate metallization access resistance [4]:

$$r_{ga}^{(ac)}(f) = r_{ga}\sqrt{1+\frac{f}{f_{se}}},$$

(3)

where the characteristic frequency for onset of significant skin effect is

$$f_{se} = b\,\frac{r_{ga}}{m_o}.$$

(4)

$\mu_o = 4\pi\cdot 10^{-7}$ Vs/Am is the vacuum permeability, and β is a geometric factor, approximately equal to 3.5 for a square cross-section. For a typical r_{ga}=150 Ω/mm, f_{se} is 420 GHz. Although β can be reduced by the presence of a ground plane [5], the skin effect certainly appears to be negligible. f_{se} gets even larger for larger r_{ga}. In Section 2 we show numerically that the skin effect is indeed negligible, and that eqns. (3)-(4) are accurate and appropriate for a SBGFET gate.

Another resistive component on the input side of the FET is the charging resistance R_i (or R_{gs}) for the gate-source capacitance. This parameter is often hard to separate from R_g during extraction of the equivalent circuit [6]. However, R_i is between a sixth and a fifth of the zero-drain-bias channel resistance at the gate bias used [7]. Thus,

$$R_i \approx \tfrac{1}{5} R_o \left(\frac{L_g}{W_g} \right) \left(\frac{I_d^{(\max)}}{I_d} \right) = \frac{L_g v_{sat}}{5 m I_d},$$

(5)

where R_o and $I_d^{(max)}$ are the sheet resistance and saturated current for the full channel, I_d is the saturated current for the gate bias used, v_{sat} is the effective saturation velocity, and μ is the mobility. The factor 1/5 in eqn. (5) is the upper limit of the quantity $(R_{11}-R_{12})/(I_{11}-I_{12})^2$, where the R_{ij}- and I_{ij}-parameters determine the Y-parameters, and are derived from the linear MODFET wave equation in [8]. It accounts both for the distributed nature of R_i, and the change in sheet electron concentration along the channel. In reality, for velocity-saturated short-gate FETs, the factor can be expected to be even smaller than 1/6. Both eqns. (1) and (5) predict very small resistances, often much smaller than the values produced by equivalent circuit extraction methods. This is an indication of an additional component in the input resistance, the physics of which must be established in order to better understand FET operation, and to generate scalable CAD models.

Our first hint that such a component exists came not from model extraction, but from the prediction, based on well-established device physics [9], of power gain in our 0.1-μm gate-length AlInAs/GaInAs MODFETs [10]. Fig. 1 shows the predicted frequency dependence of Mason's unilateral gain G_u [11]. Measured $G_u(f)$ usually shows smooth behavior, from which f_{max} is typically estimated by extrapolation at -20 dB/decade. Not all of the gain curves in Fig. 1 exhibit such smooth behavior. The curve with the sharpest resonances includes only the two resistive components in eqns. (1) and (5). The only reasonable way we found to damp the resonances, for a more realistic prediction, was to introduce an additional component in R_g. As shown in Fig. 1, the increase of this component produces increasingly smooth $G_u(f)$. The most likely physical location of this component is at the metal-semiconductor interface, since all other physical contributions to R_g are accounted for. We thus introduce [10] an *interfacial gate resistance component*

$$R_{gi} = \frac{r_{gi}}{W_g L_g},$$

(6)

which scales as a contact resistance with r_{gi} as the *normalized interfacial gate resistance*. This is reminiscent of JFET behavior, where the effect is well understood in terms of a standard ohmic contact resistance. In our gate lithography [12], care has been taken to avoid the "necking" problem [13] that can occur for short gates with large height-to-width aspect ratio in the cross-section of the bottom stem part of the gate metallization mask. Fig. 5 in [12] shows our rectangular T-gate stem, which differs from the trapezoidal shape associated with necking [13]. In processes where necking does occur, an additional gate resistance term with the same $1/W_g$ scaling as in eqn. (6) would result if the top of the trapezoid gets sufficiently narrow. In severe cases, where the trapezoid becomes a triangle, disconnecting the top from the bottom, the result would be a large increase in the standard metallization access resistance R_{ga} which is proportional to W_g (eqn. (1)).

The rest of this paper deals with establishing r_{gi} for SBGFETs, not as a fudge factor, but as a legitimate, ultimately intrinsic, physically based parameter which must be dealt with appropriately in order to properly optimize the device and to accurately scale CAD models. We show how we measure R_g, and that it has a component which scales inversely with gate width; and discuss several significant consequences of the interfacial gate resistance for optimization and modeling. We leave the detailed analysis of the physical origin of r_{gi} to a separate article [14].

We end this introductory section by showing evidence in the literature that ours is not the only laboratory in the world where this 'new' gate resistance component appears. Table I shows published data on high-performance short-gate AlInAs/GaInAs MODFETs. It includes gate geometry, channel sheet resistance, relative current bias, gate metal access resistance, and the equivalent circuit (ec) values for R_i and R_g. It also includes R_{ga} and R_i calculated (calc) by eqns. (1) and (5), respectively. The last column lists the residual gate resistance $\Delta R_g = R_g^{(ec)}+R_i^{(ec)}-R_{ga}^{(calc)}-R_i^{(calc)}$. In all cases ΔR_g is larger than the theoretical estimate $R_{ga}^{(calc)}+R_i^{(calc)}$, in all cases but one [19] significantly so. As discussed above, normal skin effect is negligible. It has, however, been proposed that skin effect resulting from field concentration at the gate footprint can be a reason for excessive RF gate resistance [16]. This would involve a significant difference in potential between the top and bottom of the T-gate, at the far end of the gate. This is unlikely, and 3D numerical modeling in

Section 2 shows that the effect is indeed negligible. The most likely origin of ΔR_g is instead the metal-semiconductor interface. If one multiplies ΔR_g by gate area $L_g W_g$, i.e. normalizes it as if it scaled as an interfacial component, the values fall in the range $6 \cdot 10^{-8}$ - $2 \cdot 10^{-6}$ Ωcm^2 . This range is consistent with values we have seen during our process development, as we discuss below. The wide spread is not unreasonable considering how critical variations in surface conditions can be, a well-known empirical fact. Part of the spread is undoubtedly due to errors introduced by basing the estimate on a single gate width, as will become clear in Section 3.

2. 3D Modeling of the Skin Effect in a MODFET T-gate

The curve-fitting formula, eqns. (3)-(4), for the skin effect is based on numerical calculations for isolated strip conductors with rectangular cross-section [4]. It tends to overestimate the effect when the frequency is not very different from f_{se} and the cross-section aspect ratio is close to one, but not by much more than 10% [4]. The presence of a ground plane can in extreme cases increase the AC resistance by a factor of two because of current redistribution and concentration towards the side of the strip nearest the ground plane [5]. For a lossy ground plane, and sufficiently wide strip and high frequency, another factor of two is incurred [5]. A MODFET gate is different from the microstrip case in several respects. The gate dimensions and shape are very different from a typical microstrip. The ground plane is quite far removed, and has negligible effect on wave propagation along the gate finger. The nearby channel, however, does affect the transverse field lines. The 2DEG channel can for the present purpose be thought of as a lossy ground plane, but, in contrast to [5], it has limited extent. The nearby highly conductive source and drain contacts reduce the loss from the case of an infinite lossy ground plane [5]. The qualitative reason proposed for the 10X discrepancy between DC and RF gate resistance in [16] relies on field concentration at the gate footprint due to the proximity of the conductive channel, and the resulting increased skin effect. We find this unlikely to cause such a large R_g discrepancy. However, we are unable to prove this analytically, because of the geometrical complexity of the problem. In this section we instead analyze it numerically.

Fig. 2 shows the cross-section of a 0.1-μm T-gate MODFET similar to ours. The gate metal is assumed to have a relative dielectric constant of one. The choice of metal dielectric constant is not critical since the $4.1 \cdot 10^7$ S/m conductivity will swamp any parallel displacement current. Fig. 2 fully represents the geometry and physics of the electromagnetic problem of feeding a MODFET gate with an input signal. We use the HP-MDS/Momentum software to solve the 3D electromagnetic problem. The software treats the interior of metals in a simplified way that is valid for typical microstrip geometries. In our case, the method can be used for the drain and source contact metal, and for the 2DEG. However, for the gate, the aspect ratio and small bottom stem preclude relying on this standard treatment. Instead, we represent the gate as a square lattice of thin metal sheets as shown in Fig. 2, and described in the caption. The central result is contained in the 200-GHz current density distribution over the horizontal segments in Fig. 2. Note that the current density peaks at the corners, and that the center number is the lowest. These are the manifestations of the skin effect [4]. By comparing the $R \cdot I^2$ power distribution of the high-frequency case to the uniform DC case, one finds that the skin effect even at this presently unattainably high frequency, results in only a 12% increase in r_{ga}. This estimate is an upper limit. In Table II below, we have also included the lower limit. The range in estimates is due to fluctuation in the numerical solution along the gate finger. Fig. 2 is the cross-section with the largest skin effect. The discretization of the problem, resulting in some degree of numerical error, is one reason for these fluctuations. Another is that, for better convergence, the gate voltage is fed only to the innermost segment at the input end, resulting in small wave-like variations along the finger.

Fig. 3 illustrates the gradual (linear) reduction in gate current density as the open end is approached, and an essentially uniform displacement current is fed from the bottom of the gate to the 2DEG. This results in the factor 1/3 in eqn. (1). The center-feeding causes the $\approx$ 1-μm darker region with lower current density near the input side of the gate. This is the distance over which spreading of the input current from the center segment in Fig. 2 to the entire gate cross-section takes place. The uniform displacement current becomes a uniform lateral 2DEG current flowing nearly perpendicularly towards the nearby highly conductive source and drain contacts, for minimum-loss collection of the gate current. The

current flow pattern in Fig. 3 illustrates the poor local screening provided by the 2DEG, and shows that the source and drain metals act much more like a ground plane than the channel. Without this feature, of course, FET-width scaling for increased current and low-frequency gain would not be approximately linear.

Table II shows that the 2D numerical calculation in [4] for an isolated strip with our gate aspect ratio predicts a skin effect that agrees very well with our calculations for the full 3D representation of a MODFET. Since 200 GHz is close to f_{se}=330 GHz, the curve-fitting formula (eqns. (3)-(4)) overestimates the skin effect. To further compare our numerical approach with the two alternative methods, and to get into the frequency regime where eqns. (3)-(4) agree better with numerical calculations for isolated strips [4], we have included in Table II results for 800 GHz. Our numerically calculated values agree with the 2D numerical results in [4]. The curve-fitting approach is relatively more accurate as the frequency is increased above f_{se}.

Our 3D calculation of the skin effect includes the effect of field concentration at the gate footprint by the proximity of the 2DEG. Yet the results are very comparable to those for an isolated rectangular gate without a stem. The results show that the skin effect is much too small to explain the large experimentally observed gate resistances. Section 3 shows that not only is the magnitude of R_g inconsistent with skin effect, but so is its scaling with gate width.

3. Measurement and Scaling of the Gate Resistance

Computerized extraction of equivalent circuit elements, such as $R_g^{(ec)}$ and $R_i^{(ec)}$ in Table I, is necessary for generation of device models used in circuit simulators. The approach is not very suitable, however, when only one parameter (R_g) is of interest, but many FETs, with different widths and processing, are to be analyzed. We instead use a more direct "cold FET" (V_d=0 V) measurement method applicable to our symmetric 0.1-μm AlInAs/GaInAs MODFET process [9,10]. We bias the gate for full channel occupation without significant DC gate leakage. Compared to the $\approx$0.3-Ωmm source and drain resistances (R_s and R_d, respectively) the full channel resistance $R_{ch}=R_oL_g/W_g$ is negligible

(≈ 0.02 Ωmm). The equivalent circuit is shown in Fig. 4. We measure the two-port S-parameters, translate these to Y-parameters, and calculate the gate resistance from:

$$R_g = \frac{\mathrm{Re}(Y_{11})}{\mathrm{Im}^2(Y_{11})} - \frac{1}{4\,\mathrm{Re}(Y_{22})},$$

(7)

where the last term subtracts out the series contribution $R_s/2$ of the equal (and parallel) source and drain resistances. For longer gates, R_{ch} contributes to R_s and cannot be neglected [7]. Thus, we restrict the use of eqn. (7) to short symmetric gates, and the scaling study to a variation in gate *width*. Fig. 5 shows an example of the gate bias dependence of the three terms in eqn. (7) at 20 GHz. As the threshold voltage V_{th} (-0.86 V) is approached, $1/\mathrm{Re}(Y_{22})$ increases rapidly since R_{ch} ceases to be negligible compared to R_s. A similar increase occurs in the $\mathrm{Re}(Y_{11})/\mathrm{Im}^2(Y_{11})$ term since its numerator includes R_i (eqn. (5)) which is related to R_{ch}. In forward bias $\mathrm{Re}(Y_{11})/\mathrm{Im}^2(Y_{11})$ increases because of gate conduction. In the gate voltage range between threshold and Schottky turn-on, the right hand side of eqn. (7) is rather flat, and is a good measure of the gate resistance. For our normal depletion-mode FETs we use V_g=0 V. The frequency dependence of the three terms is shown in Fig. 6. For low frequencies, parallel gate conduction artificially increases the R_g estimate. At sufficiently high frequency, however, the gate conductance is negligible compared to the gate capacitance (as has been assumed in Fig. 4), and the right hand side of eqn. (7) is frequency independent and a good measure of R_g. We usually average over the flat region, and (consistent with the modeling in Section 2) have not seen any increase with frequency suggestive of skin effect, even for measurements up to 50 GHz.

Fig. 7 shows R_g, determined with the method just described, for a number of two-finger (N_f=2) FETs with 6 different total widths: W_g=22, 44, 60, 80, 100 and 150 μm. The error bars show the max-min spread. We fit the median values, by the least-squares method, to the expression for the total gate resistance $R_g=R_{ga}+R_{gi}$, allowing for a fixed layout/calibration related offset R_{gr}:

$$R_g(W_g) = R_{gr} + \frac{r_{ga} W_g}{3N_f^2} + \frac{r_{gi}}{W_g L_g}.$$

(8)

Fig. 7 has two fits, one assuming the separately measured DC value of r_{ga}, the other letting the fit determine r_{ga}. The parameter of primary interest, r_{gi}, is not critically dependent on which of the two r_{ga}'s is used. This is because R_{gi} dominates the total R_g for narrow gates. Even for the widest FET (W_g=2x75 μm) R_{gi} is large (5 Ω) compared to the realistic measurement-based R_{ga} (1 Ω), and certainly not negligible even compared to the exaggerated fit-based R_{ga} (7 Ω).

Gate recess and evaporation are the most critical steps in an SBGFET process. Delay between the two, or contamination during either, causes degradation of the FET characteristics. To some degree this always occurs in an actual fabrication environment. Thus in [10] we proposed a tunneling barrier of 1-2 monolayer of oxide or organic residue as the likely origin of r_{gi}. For our 0.1-μm AlInAs/GaInAs MODFETs, we have developed processes that keep r_{gi} at an acceptably low value. Fig. 8 shows the history of r_{gi} over the course of process development. Most of the data fall below $1 \cdot 10^{-6}$ Ωcm^2, but rarely below $3 \cdot 10^{-7}$ Ωcm^2. Three wafers exhibit interfacial gate resistance larger than $1 \cdot 10^{-6}$ Ωcm^2. In three cases r_{gi} is below $2 \cdot 10^{-7}$ Ωcm^2. $3 \cdot 10^{-7}$ Ωcm^2 seems then to be a reproducible lower limit for our material and process. An alternative process [20] which has SiO_2 instead of resist adjacent to the gate trough generally produces r_{gi} closer to, or below, this limit. We believe this process results in a more pristine metal-semiconductor interface, one that begins to approach a physically ideal Schottky barrier. We discuss this situation theoretically in [14]. We have also observed that some resists result in higher and more erratic gate resistance, possibly because they are less chemically inert to the recess etch.

There are alternative methods of determining R_g. Reference [21] uses a more general method, which does not require symmetry and short gates. That work confirms, for 0.2 μm power PHEMTs, the dominant inverse gate-width scaling of R_g that we showed in [10]. We fitted their $R_g(W_g)$ data to eqn. (8), and show the result in Fig. 9. As opposed to Fig. 7, the number of gate fingers N_f now varies. The least-squares method produces a remarkably good fit (a) with r_{gi}= $5.3 \cdot 10^{-7}$ Ωcm^2 and r_{ga}=885 Ω/mm. The interfacial gate

resistance falls in the typical range we observe (Fig. 8). r_{ga} is large, but close to the 615 Ω/mm DC estimate based on the gate cross section [22]. In fit (b) in Fig. 9, r_{ga} is fixed at the DC estimate. As in Fig. 7, this does not affect the result. Because of the many parallel fingers used, and the typical value for r_{gi}, the contribution of the large r_{ga} to the total R_g is not dominant, but still significant. This analysis of published data from another laboratory provides further evidence that the interfacial gate resistance is a common phenomenon. Because this fit uses multiple gate widths, the estimate for r_{gi} extracted from [21] is actually much more solid than the wide range resulting from single gate widths in Table I.

We have not introduced a separate equivalent circuit element for R_{gi}. R_{gi} is simply a 'new' term in the gate resistance, one that, however, scales very differently from the well-understood metallization access resistance R_{ga}, and therefore should be kept track of.

4. Consequences of the Interfacial Gate Resistance

The existence of the interfacial gate resistance r_{gi}, and its dominant contribution to the total gate resistance, has several important consequences. The first one is evident in Fig. 1. Resonances sometimes seen in Mason's unilateral gain, usually dismissed as being due to calibration problems, may very well be real, and due to a relative lack of resistive damping at the gate metal-semiconductor interface. We certainly have seen correlation between low r_{gi} and the existence of such resonances. The Y-parameters depend in a smoother way on r_{gi} than does G_u. Two particularly interesting examples, the transconductance magnitude $g_m=|Y_{21}|$ and delay $\tau=-\arg(Y_{21})/\omega$, are shown in Fig. 10, calculated at
50 GHz for our typical low-noise device. We vary r_{gi} in the experimentally observed regime (Fig. 8). The effect of R_s, R_d and R_{ga} are not included, so we are looking at what is often considered the intrinsic FET. Because the "semi-intrinsic" R_{gi} absorbs a fraction of the gate voltage, g_m is reduced. For the same reason the input capacitance $C_{11}=\mathrm{Im}(Y_{11})/\omega$ is reduced as shown in Fig. 11. Most dramatic, however, is the increase in τ shown in Fig. 10. The truly intrinsic τ (0.22ps) is quickly swamped by a component induced by r_{gi}. If one attempts to infer the extent of the high-field drain region from τ (and v_{sat}), and does not take r_{gi} into account, one could get a vastly exaggerated estimate ($v_{sat}\tau$). A less dramatic,

but still interesting, consequence of r_{gi} is the increase in output capacitance $C_{22}=\mathrm{Im}(Y_{22})/\omega$ evident in Fig. 11, despite constant intrinsic drain-source capacitance.

The interfacial gate resistance, and its characteristic scaling, also affect the optimization of the device. The ultimate invariant measure of FET small-signal AC performance is often considered to be Mason's unilateral gain G_u [11]. Because of the potential resonant behavior of G_u and its deviation from a −20-dB/decade frequency dependence, we optimize the *actual* f_{max}. This can be found easily with a root finding algorithm, and is a particularly canonical choice since it is equal to the *actual* f_{mag}, the frequency where $G_{ma}=1$ [23,24,9] (Fig. 1). We use the small-signal model described in [9], with the same FET parameters used in Figs. 1, 10 and 11, and listed in Table III. We fix the gate-channel spacing to a small value that still results in acceptable gate leakage. The first step is to determine the optimum gate length. Fig. 12 shows the dependence of the predicted f_{max} on this basic parameter. We vary the interfacial gate resistance from 0 to $1\cdot10^{-6}$ $\Omega\mathrm{cm}^2$. In Fig. 12 we have also included the current-gain cutoff frequency f_T, which does not depend on r_{gi}. Had the optimization been based on f_T, the optimum L_g would have been 0.02 μm. The optimum occurs because of the non-negligible effect of the output conductance g_d on f_T, which is significant for non-zero R_s+R_d [25] when the gate is short [26,9]. The power gain cutoff frequency depends strongly on r_{gi}, and the optimum gate length increases with r_{gi}. For our practical lower limit $3\cdot10^{-7}$ $\Omega\mathrm{cm}^2$ the optimum L_g is 0.11 μm, and we will assume this value in the following steps. In this first step we looked at the basic performance, not affected by distributed effects along the gate finger or end capacitances. Thus we picked a very small W_g, and zero end feedback capacitance C_{gdx}. These preliminary choices are abandoned in Fig. 13 where we look for optimum gate width. Because of distributed effects due to r_{ga} for wider FET fingers, and the increased importance of C_{gdx} for narrower fingers, f_{max} has a maximum, in our case at 35 μm. For narrow fingers, C_{gdx} also degrades f_T. For reference we have included the $C_{gdx}=0$ case. With the optimized gate geometry, we now look at the sensitivity to a variation in the two gate resistance components. Fig. 14 shows a strong degrading effect by the interfacial gate resistance in a range we observe experimentally. In contrast, the dependence on the gate metallization access resistance shown in Fig. 15 is rather weak. There may thus be occasion to redirect process

development efforts aimed solely at achieving a large gate cross-section toward achieving a better metal-semiconductor interface.

Fig. 16 shows the predicted frequency dependence of the minimum noise figure for the optimized FET. The calculations use a Fukui-like equation [9] based on Pospieszalski's [27] and Pucel's noise models [28]. The central parameter is the noise temperature T_d of the output conductance g_d. To be physically based, and not just a fitting parameter, T_d should be close to the actual electron temperature in the high-field drain region which determines g_d. The literature on non-stationary electron transport in FETs is consistent with temperatures from 2200 to 4600 K [9]. We assume T_d=3100 K for the calculated curves in Fig. 16. We also plot our own noise data [9], and data reviewed in [29] for 0.10-0.15 μm gate AlInAs/GaInAs MODFETs. It is interesting that the wide spread in measured noise figure can be explained by the observed wide range in r_{gi} (Fig. 8). To explain the spread through variations in T_d rather than r_{gi}, we would have to assume a totally unphysical range of 3000-30000 K.

In addition to these interesting consequences relating to device physics, there is a very important practical one, which relates to the device model we use in circuit simulation. It is likely to be important also for other device models and circuit simulators. When the large-signal measurement-based device model [30] is extracted for the FET under test, the first step is to determine the parasitic resistances from S-parameter data in cold-FET configuration. Once these have been calculated, and the S-parameters of the FET have been measured in the entire active biasing regime, the non-linear voltage-controlled charge and current functions of the three intrinsic nodes can be determined [30]. The result, an accurate large-signal non-quasi-static table-based model of the device, can then be used for reliable circuit design. However, a problem may arise if a FET of different width is used in the circuit. The simulator assumes the proportional gate width scaling of eqn. (1), and determines the constant of proportionality $r_{ga}/(3N_f^2)$ from the measured gate resistance and geometry of the FET on which the extraction was done. Since the gate resistance is dominated by a term which scales *inversely* with W_g, it is clear that this can lead to large scaling errors, and inaccurate circuit modeling. Fortunately, in the HP EEsof Root FET Model, there is a way around this problem: *by replacing in the Model Variable Table, the*

total extracted R_g with a separately measured or calculated R_{ga} (eqn. (1)), *an internal time constant model parameter 'taug' will approximately, and automatically, take care of the remaining dominant W_g^{-1}-term R_{gi}*. The model topology for the intrinsic device does not explicitly include R_i-type resistive elements [30]. However, the "all-encompassing" gate delay parameter *'taug'*, which is determined by the extraction algorithm, accounts approximately for resulting internal delays such R_iC_{gs}. By replacing R_g with R_{ga}, we have then essentially set $R_i=R_{gi}$. This is obviously not correct physically, but it does lead to correct W_g scaling, and thus much more accurate and reliable circuit simulation. The different gate length scaling of R_i and R_{gi} (eqns. (5) and (6)) is not an issue since the gate length must be considered fixed for the particular process and model.

5. Conclusions and Preview of a Theoretical Analysis

We have presented experimental evidence for the existence of an interfacial component R_{gi} in the gate resistance of our 0.1-μm AlInAs/GaInAs MODFETs, and for Schottky-barrier-gate FETs in general. The component is typically dominant, and scales inversely to the well-known metallization resistance R_{ga}. R_{gi} has probably gone undetected so long because it is negligible for longer gates, and an excessive R_g can be buried in R_i, or be dismissed as being due to skin effect. Theoretical considerations and experimental observations, however, show that neither of these is a legitimate way of accounting for a significant fraction of the input series resistance of short-gate FETs. Letting R_i account for R_{gi} becomes increasingly unphysical the shorter the gate length L_g becomes, since R_i is proportional to L_g, while R_{gi} is inversely so. We have shown how we measure the gate resistance, and confirmed the scaling of what we can only interpret as an interfacial component. The cases of longer gates that we have examined are consistent with an inverse L_g scaling, but, because of the increase in channel resistance R_oL_g/W_g for longer gates, the interfacial gate resistance is actually better studied on short gates, where it also has the most noticeable detrimental effect. We reviewed physical and practical consequences, which are important for a fuller understanding of high-speed SBGFETs, and more reliable circuit simulation.

Most models for Schottky-barrier formation involve a dipole layer between the positive metal background and negative surface or interface charge, separated by a distance of atomic layer dimension. The most widely used, and analytically tractable, model of this nature is that by Cowley and Sze [31]. They assumed a 4-5 A interfacial layer with vacuum electronic properties to explain the Schottky barrier height of a variety of metals on Si, GaP, GaAs and CdS. We have investigated the tunneling resistance presented by such an interfacial barrier to the charging and discharging of the surface states. The predictions are consistent with the experimentally determined minimum interfacial gate resistance. These theoretical results will be discussed in detail in [14], where we also investigate the frequency dependence of the phenomenon up to 1 THz. We find that the minimum r_{gi} is not expected to be capacitively bypassed at presently attainable frequencies. Thus, while Cowley-Sze's "interfacial layer of the order of atomic dimensions" is more or less "transparent to electrons" [31], it presents a resistance that cannot be ignored at microwave and millimeter-wave frequencies.

6. Acknowledgments

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FIGURE CAPTIONS

Fig. 1. Calculated unilateral and maximum stable/available gain versus frequency for a 0.15-μm AlInAs/GaInAs MODFET with gate resistance as a parameter. R_g increases in the direction of the arrows.

Fig. 2. Symmetric cross-section of a 0.1-μm T-gate MODFET geometry for one-port HP-MDS/Momentum simulation. The width of the gate finger, i.e. the dimension into the page, is 25 μm. The stimulating gate voltage is fed to the center of the input end of the gate finger. The return current is collected laterally through the 2DEG by the source and drain contact metal (Fig. 3). The drain, source and 2DEG are modeled as solid metals. The 2DEG channel is represented by thin metal with its conductivity adjusted to yield the 200 Ω/square full channel sheet resistance. The gate is made up of two perpendicular sets of thin metal sheets. The horizontal sheet conducts laterally and along the gate finger. The vertical sheets are "vias" that connect adjacent horizontal sheets, and conduct only in the vertical direction. Thus, these do not contribute to the conductance of interest along the gate finger. The conductance of each sheet is adjusted to account for the conductance of the actual bulk gate metal in the 0.1 μm separation between the sheets. Thus, an edge sheet (dotted lines) has half the conductance of an interior sheet. This has been accounted for in the 200 GHz current density (framed numbers) associated with a horizontal segment.

Fig. 3. Top view visual output of HP MDS/Momentum simulation of the current distribution in the MODFET in Fig. 2. The gate finger shading illustrates the current density in the top layer of the T-gate. Lighter color indicates larger density. The arrows indicate lateral current density in the 2DEG, and in the source and drain contacts.

Fig. 4. Equivalent circuit for a short symmetric cold FET: V_d=0 V, $n_s(V_g)=n_{so}$

Fig. 5. A measurement of the three terms in eqn. (7) versus V_g at V_d=0 V and f=20 GHz. L_g=0.1 μm, W_g=2x30 μm.

Fig. 6. Frequency dependence of the three terms in Fig. 5 at $V_g = V_d$ =0 V.

Fig. 7. Gate resistance of two-finger 0.1-μm AlInAs/GaInAs MODFETs versus total gate width. (a) Full fit → r_{ga}= 560 Ω/mm, r_{gi}= $9.2 \cdot 10^{-7}$ Ωcm^2 . (b) Fit with r_{ga}(DC)= 82 Ω/mm → r_{gi}= $8.1 \cdot 10^{-7}$ Ωcm^2 .

Fig. 8. History of the interfacial gate resistance for our 0.1-μm AlInAs/GaInAs MOD-FETs. r_{gi}= $2 \cdot 10^{-7}$ Ωcm^2 has been high-lighted with a bold line.

Fig. 9. Gate resistance and number of gate fingers for multi-finger 0.2-μm PHEMTs versus total gate width [21]. (a) Full fit → r_{ga}= 885 Ω/mm, r_{gi}= $5.3 \cdot 10^{-7}$ Ωcm^2 . (b) Fit with r_{ga}(DC est.)= 614 Ω/mm → r_{gi}= $5.9 \cdot 10^{-7}$ Ωcm^2 . R_{ga} and R_{gr} are the gate metallization access resistance and the residual fixed resistance, respectively, for fit (a).

Fig. 10. Effect of the interfacial gate resistance on the microwave transconductance.

Fig. 11. Effect of the interfacial gate resistance on the input and output capacitance.

Fig. 12. Calculated current and power gain cutoff frequencies for optimization of the gate length. The interfacial gate resistance is varied in its experimentally observed typical range.

Fig. 13. Calculated current and power gain cutoff frequencies for optimization of the gate width. The interfacial gate resistance is our lowest practical, and the gate length optimum associated with this. The case of no end feedback capacitance is shown for comparison.

Fig. 14. Calculated sensitivity of current and power gain cutoff frequencies to a variation in interfacial gate resistance for the optimized device.

Fig. 15. Calculated sensitivity of current and power gain cutoff frequencies to a variation in gate metallization access resistance for the optimized device.

Fig. 16. Calculated minimum noise figure versus frequency for the theoretically optimized device. The interfacial gate resistance is varied in steps of $5 \cdot 10^{-7}$ Ωcm^2 in a range observed experimentally. Measured room temperature noise figure for our own FET [9] (solid circle), and for other discrete 0.10-0.15 μm AlInAs/GaInAs MOD-FETs [29] (open circles) have been included.

TABLES

Table I: Examples of indication in InGaAs/AlInAs MODFET literature of a residual gate resistance: $DR_g = R_g^{(ec)}+R_i^{(ec)}-R_{ga}^{(calc)}-R_i^{(calc)}$; ec=equivalent circuit, calc= calculated with eqns. (1) and (5).

Ref.	L_g (μm)	W_g (μm)	N_f	R_o (ohm)	$I_d/I_d^{(max)}$	r_{ga} (ohm/mm)	$R_i^{(ec)}$ (ohm)	$R_g^{(ec)}$ (ohm)	$R_i^{(calc)}$ (ohm)	$R_{ga}^{(calc)}$ (ohm)	ΔR_g (ohm)
[15]	.08	50	2?	208	.30	300	1.0	7.0	0.2	1.3	6.5
[16]	.18	125	8	208	.12	86	6.0	0.6	0.5	0.1	6.0
[17]	.10	50	2?	210	.14	88?	11.8	0.34	0.6	0.4	11.1
[18]	.15	100	2	242	.16	150	5.6	7.09	0.45	1.3	11.0
[19]	.10	40	4	210?	.13	190	0.4	1.92	0.81	0.16	1.4

When not enough information was available from the references (indicated by '?') we assumed v_{sat} $=2.7\cdot10^7$ cm/s, n_{so} $=3\cdot10^{12}$ cm^{-2} (full channel electron sheet concentration), $N_f=2$, $\rho=2.2\cdot10^{-6}$ Ωcm (Au), and/or $A_{gx}=(0.5\ \mu m)^2$. Because of the small $R_{ga}^{(calc)}+R_i^{(calc)}$, these uncertainties should not affect ΔR_g much.

Table II: MODFET T-Gate Skin Effect $r_{ga}^{(ac)}(f)/r_{ga}$ at Two Large Frequencies Calculated with Three Methods

f(GHz)	HP-MDS/Momentum, Full MODFET 3D Geometry	2D Numerical, Isolated Strip [4]	Eqns. (3)-(4), Isolated Strip
200	1.05-1.12	1.10	1.27
800	1.67-1.73	1.70	1.85

Table III: Fixed parameters based on measurements and reverse modeling [7,20]

Variable Definition	Variable	Value
Channel sheet resistance (cf. eqn. (5))	$R_oI_d^{(max)}/I_d$	400 Ω
Effective saturation velocity	v_{sat}	$2.8\cdot10^7$ cm/s
Gate-channel spacing	d_{gc}	235 A
Normalized output conductance [9]	$g_d^{(sq)}=g_dL_g/W_g$	15 μS
Intrinsic transconductance delay	τ	0.22 ps
Source resistance	R_s	0.34 Ωmm
Drain resistance	R_d	0.31 Ωmm
Gate metallization access resistance	r_{ga}	46 Ω/mm
Source and drain side fringe capacitance	C_f	114 fF/mm
Intrinsic drain-source capacitance	C_{ds}	288 fF/mm
Layout dependent feedback capacitance (W_g indep.)	C_{gdx}	0.55 fF

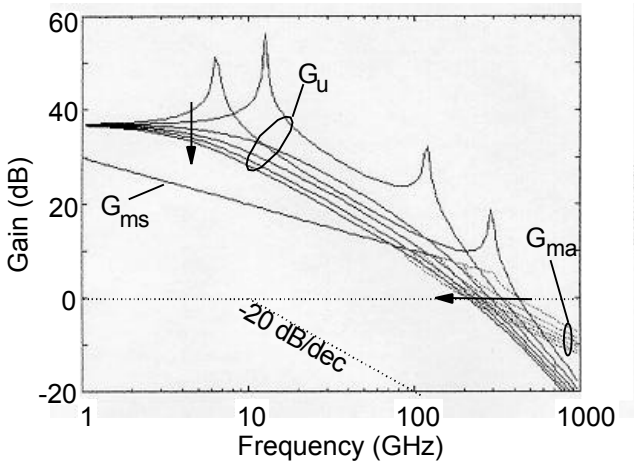


Fig.1

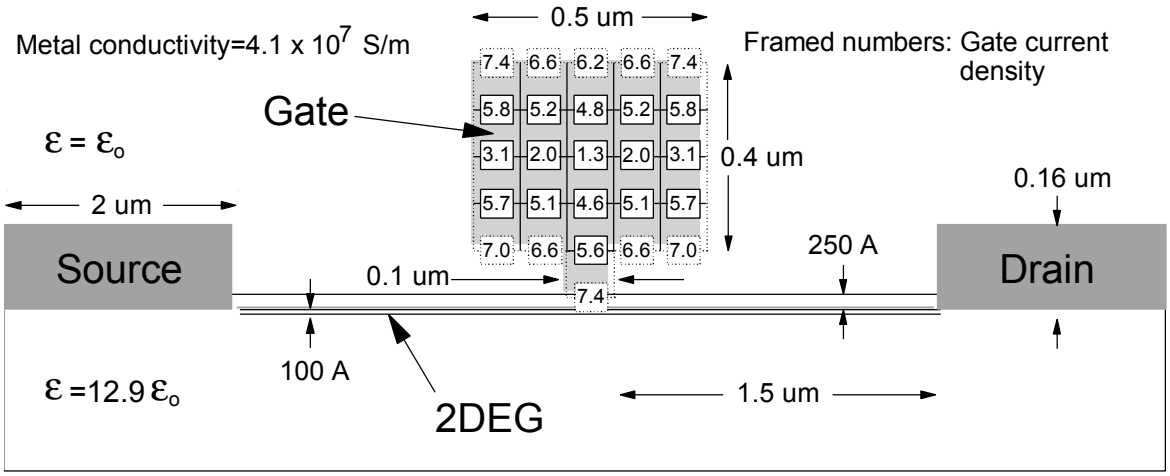
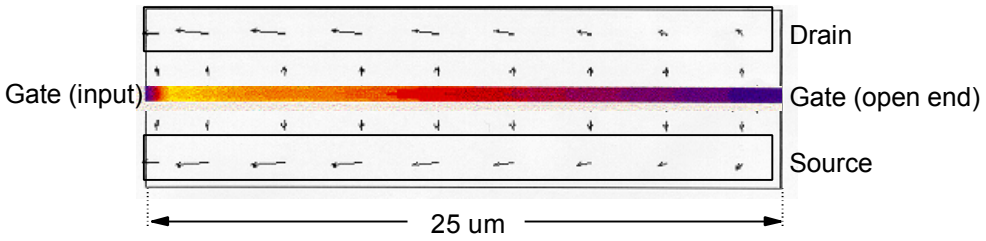


Fig. 2



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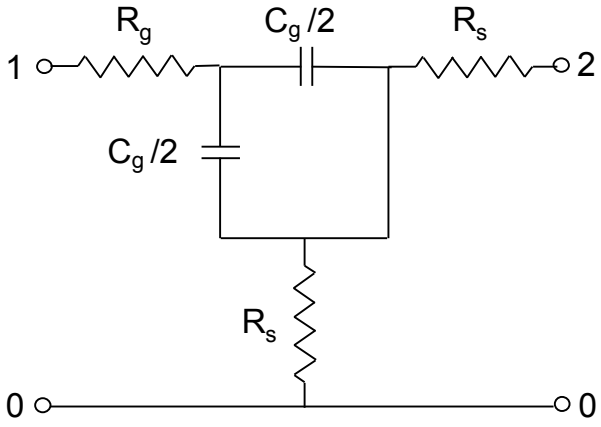


Fig. 4

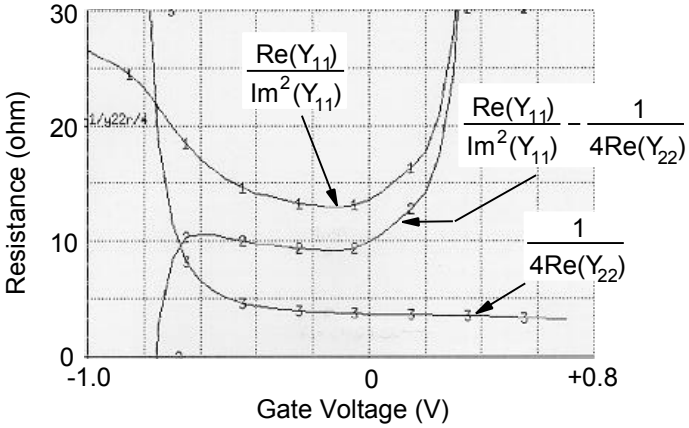


Fig. 5

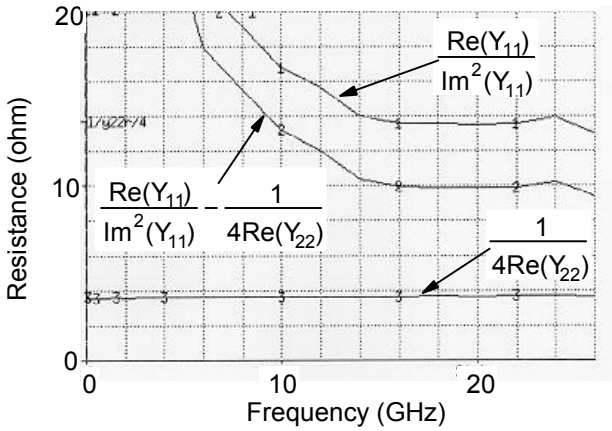


Fig. 6

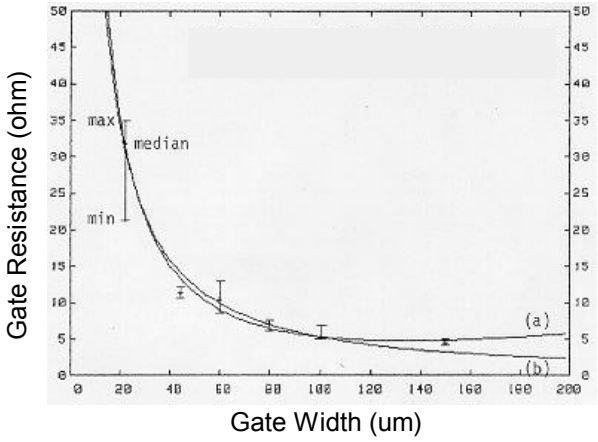


Fig. 7

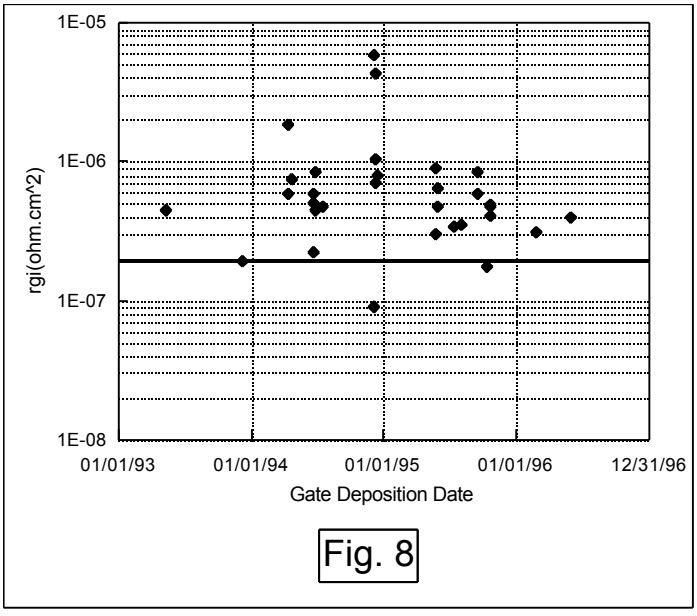


Fig. 8

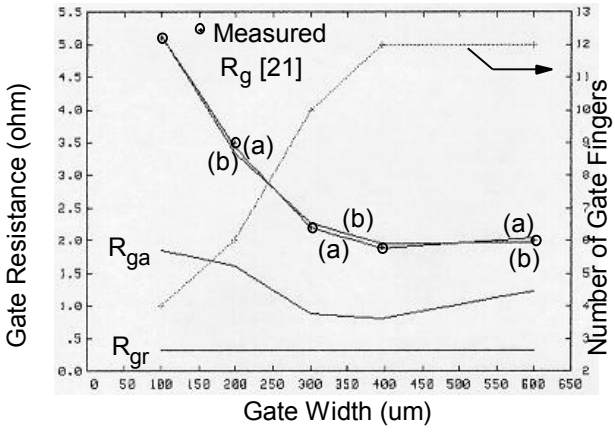


Fig. 9

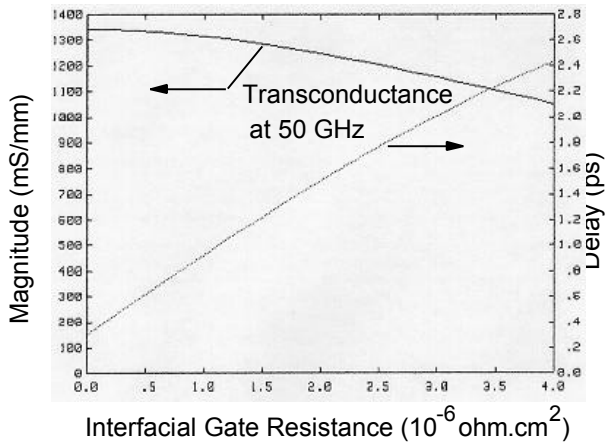


Fig. 10

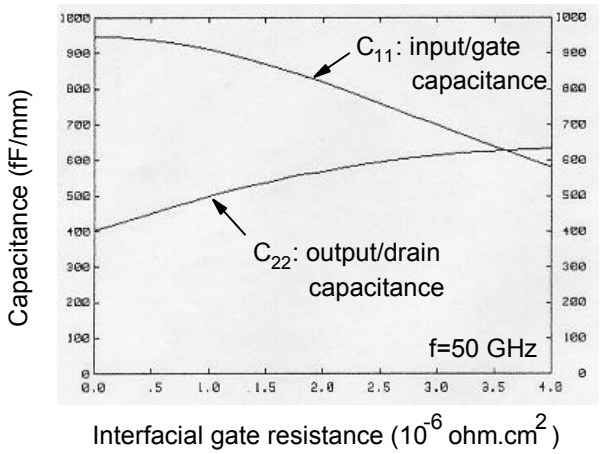
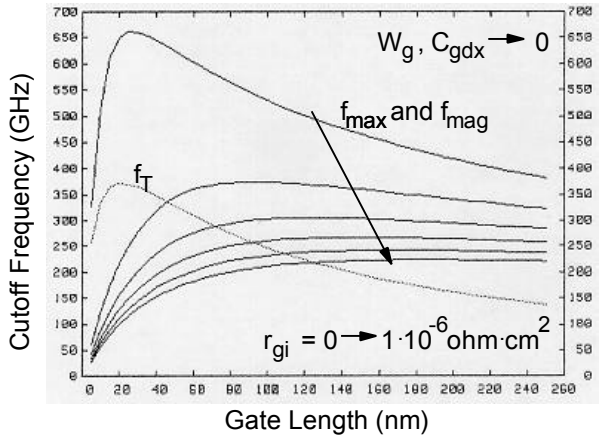


Fig. 11



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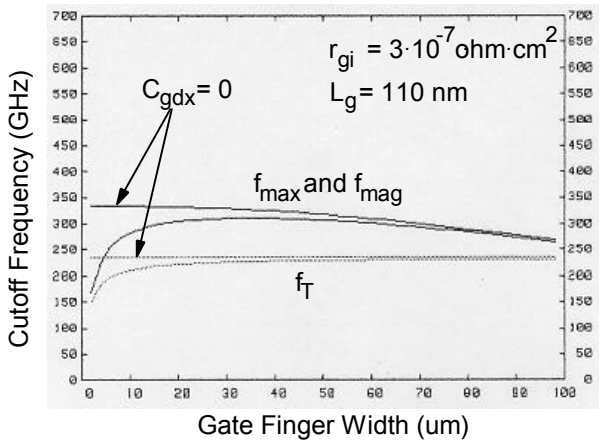
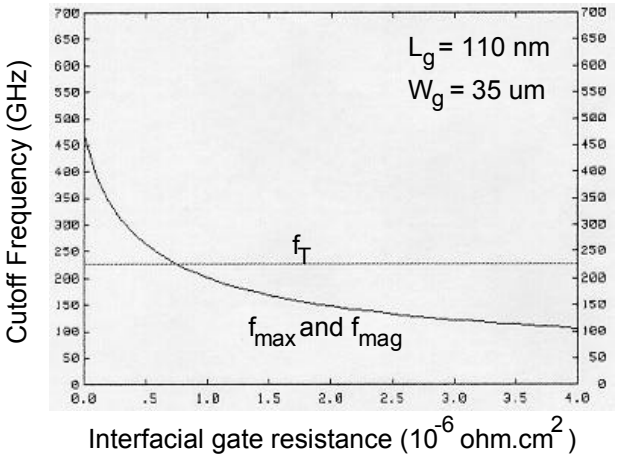


Fig. 13



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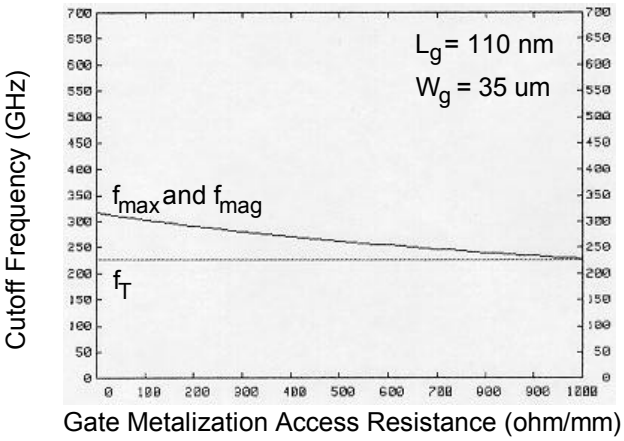

Fig. 15

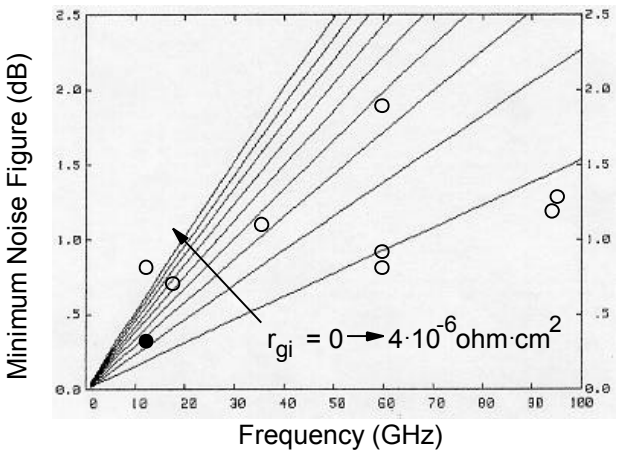
Minimum Noise Figure (dB)
2.5
2.0
1.5
1.0
.5
0.0
0
10
20
30
40
50
60
70
80
90
100
r_{gi} = 0 → 4·10^{-6}ohm·cm^2
Frequency (GHz)

Fig. 16