An IC for Linearizing RF Power Amplifiers Using Envelope Elimination and Restoration

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This paper presents a monolithic CMOS implementation of an envelope elimination and restoration linearization system that improves the linearity of efficient RF power amplifiers. The linearization IC, which occupies 4.3 mm^2 when implemented in a 0.8-μm CMOS technology, consists of a limiter, envelope detectors, and a delta-modulated switching power supply. This circuit was used to linearize AMPS (Advanced Mobile Phone System) cellular power amplifiers transmitting NADC (North American Digital Cellular) wave-forms. Measurements show that the linearized outputs meet the spectral mask and phase distortion requirements of NADC. The linearization system can improve the overall efficiency from 36% to 49%, while increasing the maximum linear output power from 26.5dBm to 29.5dBm.

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I. INTRODUCTION

Efficient radio-frequency (RF) power amplifiers (PAs) are highly desirable in battery-operated systems such as cellular telephones because PAs typically dominate the power consumption of these portable systems. RF PAs are most efficient when operating as compressed, nonlinear amplifiers [1]-[2]. However, these nonlinear PAs can only amplify constant-envelope RF signals without introducing significant distortion. Cellular systems such as the Advanced Mobile Phone System (AMPS) and Global System for Mobile communications (GSM) employ modulation schemes that generate constant amplitude RF outputs in order to use efficient but nonlinear PAs. With the growing emphasis in channel capacity, several modern wireless communication systems use non-constant envelope RF signals so as to increase spectral efficiency. For example, the North American Digital Cellular (NADC) standard employs $\pi/4$ QPSK modulation. This modulation format has a 3:1 envelope variation [3]. Unfortunately, the amplification of non-constant envelope RF signals requires linear PAs, which are inherently less power efficient.

The traditional approach to linear RF power amplification is to back-off the output power of a PA until its distortion is reduced to an acceptable level. This *power back-off* approach to linear amplification suffers from significant reduction in both output power and efficiency. Numerous alternative approaches to linear RF power amplification have been proposed [1], [4]-[9]. This work investigates the use of an envelope elimination and restoration (EER) system [4]-[5] as an alternative to *power back-off*, to simultaneously achieve efficiency and linearity in RF PAs. In particular, this paper presents the design of a delta-modulated switching power supply, a limiter, and envelope detectors that together form a feedback system to linearize efficient but nonlinear PAs. The prototype linearization system, designed in a standard 0.8-μm CMOS technology, has been tested with a CMOS PA [10], and two commercially available gallium arsenide (GaAs) PAs.

Compared to the power back-off approach, EER linearization provides: 1) higher linear RF output power, 2) higher peak efficiency, and 3) higher efficiency across a wider range of output power. High efficiency across a range of output powers is important for radio systems that utilize power control. In radio systems with power control, the power amplifiers often run at less than the maximum power output level, and efficiency at these reduced power levels is important.

Compared to previous discrete implementations of EER systems [11]-[12], which are intended for use in high-power base stations, this design is amenable to integration in a low-cost CMOS technology and makes linearization affordable for hand-sets.

Section II describes the architecture of linearization system. It presents the trade-off between efficiency and linearity in RF power amplifiers as well as introduces the envelope elimination and restoration linearization technique. Section III explains the design and implementation of the linearization IC, consisting of a switching power supply, an RF envelope detector and RF limiter.

The performance of the linearization IC when applied to three different RF PAs are summarized in Section IV.

II. ARCHITECTURE

A. RF POWER AMPLIFERS

Fig. 1 shows the typical output stage of an RF PA, which consists of an output transistor, an RF choke, and an impedance matching network. The behavior of this amplifier is determined by its conduction angle, input signal overdrive, and output load impedance. A comprehensive review of the classical definitions of RF power amplifier is given in [1]-[2]. Fig. 2 shows how the classical definitions [2] of a MOS power amplifier relate to its conduction angle and input signal overdrive. It illustrates that a given PA can potentially be in any one of the classical operating modes depending on its conduction angle and input signal overdrive. For a small RF input signal V_{in}, the amplifier in Fig. 1 can operate in class A, AB, B, or C depending on its conduction angle, which is determined primarily by its DC gate bias. The PA efficiency can be improved by reducing its conduction angle (moving the design into class C operation) but at the expense of lower output power. An alternative approach to increase PA efficiency that does not compromise output power is to increase its gate overdrive until the output transistor operates as an on-off switch [13]. This nonlinear but efficient switched-mode operation is commonly referred to as *saturated class A, saturated class C, class D, class E, or class F* amplifier depending on its conduction angle and load impedance [2]. In this paper, no attempt is made to differentiate the various *switched-mode* PAs.

The trade-off between efficiency and linearity for the simplified PA output stage in Fig. 1 is determined by its gate overdrive. Assuming that the output transistor is biased for class A operation, for a small RF input V_{in}, the output drain voltage V_D is a linearly amplified version of the input. The power dissipated in the output transistor is given by $P_D = I_D \times V_D$. Reducing power P_D by increasing the gate overdrive will improve the overall efficiency of the amplifier. When the output transistor operates as an on-off switch, the output drain voltage and current are distorted square waves. If there is no overlap between the drain current and voltage, the product $P_D = I_D \times V_D = 0$. When no power is wasted in the output transistor, all of the power from the supply is delivered to the load and maximum efficiency is achieved. Obviously, any realizable RF PA will suffer from losses due to overlapping on-times of the drain current and voltage as well as parasitic on-resistance of the output transistor. Nonetheless, a *switched-mode* PA can be highly efficient but will also be highly nonlinear.

In a switched-mode PA, the output power

$$P_{OUT} \propto V_{DD}^{2}. \quad (1)$$

That is, the output power or the envelope of the RF output signal can be controlled by varying the supply voltage. This characteristic of switched-mode PAs is ideally suited for linearization using envelope elimination and restoration.

B. ENVELOPE ELIMINATION AND RESTORATION

Fig. 3(a) shows the block diagram of the EER linearization scheme as first proposed by Khan [4]. As the name "envelope elimination and restoration" implies, the envelope of the RF input is first *eliminated* by a limiter to generate a constant-amplitude phase signal. At the same time, the magnitude information is extracted by an envelope detector. The magnitude and phase information are amplified separately and then recombined to *restore* the desired RF output. A way to recombine the magnitude and phase components is to use an efficient switched-mode RF PA. As described by (1), the envelope of the RF output of a switched-mode PA is directly proportional to its supply voltage. The envelope and phase components can therefore be recombined if the phase signal (RF) is applied at the gate of the transistor and the magnitude signal (low frequency) directly modulates the supply. The key advantage of this EER approach is that the RF PA always operates as an efficient switched-mode amplifier. That is, the EER system can linearize the switched-mode RF PA without compromising its efficiency.

Fig. 3(b) shows the prototype implementation of a closed loop EER system. Similar to Fig 3(a), the RF input is decomposed into its polar components—a low-frequency (LF) envelope (magnitude) and a radio-frequency (RF) phase—by an envelope detector and limiter, respectively. In this design, a switching power supply amplifies the LF magnitude, while an efficient constant-amplitude RF PA amplifies the constant-amplitude RF phase. The recombination process in Fig. 3(b) involves directly modulating the supply voltage of a switched-mode PA using the LF output of the switching power supply. A feedback path from the RF output of the PA to the input of the switching power supply guarantees amplitude tracking between the RF input and RF output wave-forms. This feedback loop reduces the non-linearities introduced 1) by the mismatch between the phase and magnitude paths and 2) by the switched-mode amplifier when it deviates from the ideal behavior predicted by (1). Two separate envelope detectors in Fig. 3(b) provide first order cancellation of non-idealities introduced by the envelope detectors.

In an EER system, the phase and magnitude paths are amplified separately. The delay in the RF phase path can be substantially shorter than that of the low-frequency magnitude path. Mismatch in the delay of these two paths is a source of distortion [15]. According to Raab [15], the intermodulation distortion introduced by delay mismatch for two equal input tones is given by

$$IMD \approx 2\pi B_{RF}^{2}\,\Delta\tau^{2} \tag{2}$$

where B_{RF} is the bandwidth of the RF signal and $\Delta\tau$ is the delay mismatch. The result given by (2) matches well with behavioral simulations of two-tone tests for third-order intermodulation in the range of -60dBc to -20dBc. For two tones that are 300 kHz apart, the third-order intermodulation is less than -40dBc when the delay mismatch is less than 130ns.

The dominant source of delay in the magnitude path in Fig. 3(b) is the lowpass filter of the switching power supply. Instead of using an explicit delay in the phase path to match that of the envelope path [12], this design employs feedback to reduce the delay of the magnitude signal. In a closed-loop system, the delay introduced by the lowpass filter in the forward path is reduced by the loop gain. This delay reduction is analogous to how the delay of the dominant pole of an operational amplifier is reduced by its feedback.

Two techniques allow the phase path of this design to operate in an open-loop configuration. First, a limiter is used to form the input to the switched-mode PA. A switched-mode PA will generate unacceptably large phase distortion if its RF input has a non-constant envelope [14]. The limiter removes envelope fluctuations, and thus any phase distortion that might be introduced by the PA. Secondly, the modulated power supply is applied only to the drain of the output transistor of the RF PA. A changing voltage at this point has only a minor effect on the phase of the output wave-form. Therefore, unlike the design in [14], phase feedback is not required in this design. These design choices significantly simplify the architecture of the system. However, special care must be exercised in the design of the limiter to reduce AM to PM distortion.

III. IMPLEMENTATION

Several implementations of the envelope elimination and restoration system have been proposed to provide efficient, linear RF power amplification [11]-[12]. This work focuses on a monolithic implementation in a low-cost CMOS technology. The linearization IC consists of a switching power supply, envelope detector, and limiter.

A. SWITCHING POWER SUPPLY

Several previously reported implementations of EER use pulse-width modulation (PWM) in the switching power supply. Unfortunately, PWM is an inherently nonlinear process that generates harmonic distortion [2],[16]-[17]. This design uses delta modulation to provide improved linearity over a wider signal bandwidth [18].

Fig. 4 shows the block diagram and schematic of a switching power supply based on delta modulation. The purpose of this switching power supply is to provide linear amplification of the

envelope information in Fig. 3(b). The block diagram in Fig. 4(a) is conceptually similar to a traditional switching power supply. It is a closed-loop system that employs a modulation scheme to generate a two-level signal. This two-level signal is efficiently amplified by a class-D driver, and then lowpass filtered to reconstruct the desired output. Pulse-width modulation is widely used in switching power supplies that only need to provide a DC or low-frequency output. In low-frequency (or DC) applications, the non-linearity of pulse-width modulation is not relevant. However, in applications that require switching power supplies with large bandwidths and low distortion, a more efficient modulation scheme such as delta modulation is preferred. For the same over-sampling ratio (or switching frequency), a system based on delta modulation can provide wider signal bandwidth and lower distortion than a pulse width modulated system [18]. Finally, as shown in Fig. 4(b), the circuit complexity of a system based on delta modulation is comparable to that of pulse-width modulation.

The delta modulation loop in Fig. 4(a) comprises a subtractor, a compensation zero that ensures stability, a comparator, and an external passive second-order low-pass filter. In the complete linearized amplifier system, the feedback loop encloses the RF power amplifier. In this case, the amplitude feedback for the delta modulator comes from an envelope detector placed at the output of the RF power amplifier.

If the compensation network and the high-frequency gain blocks are ignored, this system can be reduced to a block diagram with subtractor, comparator, and lowpass filter. That is, the block diagram is essentially a delta modulation loop with a low-pass filter instead of an integrator. Since the delta modulation system is relatively insensitive to timing jitter, the sampling clock can potentially be derived directly from a divided-down version of the incoming RF signal. The lowpass filter in Fig. 4 is a second-order Butterworth filter. In order to ensure loop stability, a compensation zero of ($1.3–z^{-1}$) is implemented in discrete time.

Fig. 4(b) shows the switched-capacitor circuits used to implement the subtraction and compensation functions. The switches are NMOS transistors driven by 10MHz voltage-boosted clocks [19]. The capacitors consist of parasitic capacitance between metal 1, 2, and 3 because explicit high-density capacitors are not available in this digital technology. The operational amplifiers are fully differential folded cascode amplifiers with capacitive common-mode feedback [20] and gain boosting [21]. The output buffer is a large CMOS inverter.

The comparator consists of a preamplifier and a regenerative latch. The simplified schematic of the preamplifier is shown in Fig. 5. It consists of a differential pair with NMOS active loads. The transconductance of the cross-coupled NMOS transistors are chosen to be smaller than that of the diode-connected devices to ensure a positive impedance [22]. During the sample-mode, the differential pair is in unity gain feedback and the input voltages are stored on capacitors C1 and C2. During the amplification phase, the voltages stored in C1 and C2 are amplified to the output.

In order to increase the speed of the voltage regeneration, an additional cross-coupled pair of transistors Mx and My are turned on by a delayed clock to change the preamplifier into a regenerative latch. A second regenerative latch similar to the design in [23] is used to ensure full CMOS output swings. With input offset cancellation, this comparator can operate at 20MHz with an input offset of less than +/-0.5mV.

The switching power supply in Fig. 4 is essentially an audio frequency power amplifier. Fig. 6 shows the output spectrum of the power supply for a 20kHz, 0.8-V peak sinusoidal signal. Distortion of -55dBc and efficiency of 80% are achieved. When operating from a 3-V supply, the switching power supply can provide an output voltage that ranges from 0.1V to 2.65V, an output current of 0.75A, a signal bandwidth of 100kHz, a static power dissipation of 10mW, and an overall efficiency of 80%. The die area when implemented in a 0.8–μm CMOS technology is 3.9 mm^2. High efficiency in the switching power supply is desirable because its loss limits the overall power added efficiency (PAE) for the linearized system.

B. ENVELOPE DETECTOR

The main obstacle in designing an RF envelope detector in a CMOS technology is the lack of an ideal diode that can operate at the RF frequency. As shown in Fig. 7, the CMOS envelope detector consists of NMOS transistor M1 operating as a diode, capacitor C1, and current source I1. It is capable of extracting a 100kHz envelope from a 800-900 MHz RF input. Unfortunately, the gate to source voltage of transistor M1 is rather large and introduces distortion. A first order cancellation of the DC voltage and distortion of transistor M1 is provided by a pseudo-replica circuit consisting of transistor M2 and current source I2. Amplifier A1 keeps the voltages at nodes X and Y equal by driving the gate of transistor M2 to be equal to the envelope of the RF input signal at the gate of M1. A key feature of this envelope detector is that the pseudo-replica circuit only needs to operate at the envelope frequency, not at RF.

The envelope detector occupies 0.03 mm^2 of die area and dissipates 1.5mW of static power. The measured performance of this envelope detector in Fig. 8 shows that the 30kHz envelope of the RF signal can be extracted from an AM modulated RF input at 835MHz. As shown in the block diagram of the EER system in Fig. 3(b), two envelope detectors are used. The matching of these two detectors provide first-order cancellation of their non-idealities. The RF inputs to the envelope detectors are AC coupled through on-chip capacitors. This guarantees zero DC offset between the input and feedback signals at their respective envelope detectors.

C. LIMITER

Designing a 800 MHz RF limiter in a 0.8–μm CMOS technology poses a challenge because of the lack of gain at radio frequency, where the gain of a differential-pair is only slightly greater

than unity. Since the RF input signal of a PA is typically 0 dBm or larger, this design avoids the need for large RF signal gain in the limiter by either attenuating or amplifying the input signal to maintain a constant envelope. Limiting is performed with a variable gain amplifier in a feedback system to keep a constant envelope as illustrated in Fig. 9. The circuit consists of a variable gain amplifier (VGA), an envelope detector, and an error amplifier. The envelope of the VGA output is detected and compared with a DC reference signal generated on-chip by a replica circuit. The error amplifier adjusts the gain of the VGA to provide a constant envelope RF output. Because NADC signals only have an envelope variation of 3:1 [3], the requirements on this limiter are significantly relaxed compared to a limiter that must operate with 100% envelope modulation generated by two equal tones.

As discussed in Section II, the VGA in Fig. 9 must have low AM to PM distortion. Fig. 10 shows a VGA design that uses a multiplier-like structure with two differential pairs to ensure a constant DC bias point at the drains of the differential pairs. This topology is chosen instead of a simple differential pair because a VGA built as a simple differential pair with adjustable tail current can introduce substantial AM to PM distortion [24]. In Fig. 10, the RF input signal is applied to the first differential pair, whose tail current is controlled by a low-frequency control signal. A change in the tail current I_{b1} of the first differential pair is offset by an opposite change in I_{b2} of the second differential pair. The sum of the output currents I_{o1} and I_{o2} is always equal to the sum of the two tail currents I_{b1} and I_{b2}. The sum of I_{b1} and I_{b2} are in turn held constant by current source I_x.

The limiter, which consists of a single-ended to differential converter, a variable gain amplifier, an envelope detector, and an operational amplifier, occupies 0.34 mm^2 of die area and dissipates 37mW of static power. The RF output buffer of the limiter, on the other hand, dissipates 70mW of static power. The measured performance of the limiter (Fig. 11) shows that the envelope of a 835MHz carrier with 3:1 envelope variation is successfully removed. Measurement using a digitizing oscilloscope shows that the output has less than 1.5^o of phase modulation for a 3:1 envelope variation.

IV. EXPERIMENTAL RESULTS

The die micrograph of the linearization IC is shown in Fig. 12. All circuits are designed to operate from a supply as low as 2.7 V. However, the output buffer, which is a CMOS inverter, can operate with a supply of up to 6-V. The two on-chip inductors are used in the limiter to provide 50-ohm input and output impedance matching. The IC uses two separate on-chip supply independent bias generators for the RF circuitry (limiter and envelope detector) and the switching power supply to avoid cross-talk via the bias network. The sampling edges of the switched capacitor circuits are placed in the quiet time between transitions of the output buffer. Over 27

bond wires are used to provide a low-impedance ground/substrate contact. The linearization IC occupies 1.2mm x 4.2mm when fabricated in a 0.8-μm digital CMOS technology. The total static power dissipated in the linearization circuits is 120mW for a 3-V supply.

The linearization IC was applied to three different RF power amplifiers: a 3.3-V GaAs PA (PA3.3), a 4.8-V GaAs PA (PA4.8), and a 3-V CMOS PA.

Fig. 13 shows the PAEs of the two AMPS GaAs PAs that are linearized using the EER prototype system to meet the NADC specifications. When operating from a 3.3-V supply, the peak PAE of PA3.3 in AMPS operation is 42%. This PA can meet the linearity specification of NADC if its output power is backed off by 4 dB, which results in a PAE of 16% and an output power of 25.6dBm. On the other hand, when coupled to the linearization circuitry, PA3.3 has a peak PAE of 36% (including losses in the switching power supply and linearization circuitry) and an output power of 29dBm. In the case of PA4.8, a 5-V supply is used for the output buffer of the switching power supply to meet the part's 4.8V requirement. The peak efficiency of the linearized system with PA4.8 is 49% at 29.5dBm, which is only slightly lower than the PAE of 58% during non-linear (AMPS) operation. This result is far better than the 36% at 26.5dBm obtained when power back-off is used with this amplifier to achieve sufficient linearity. The linearization IC can also linearize a switched-mode CMOS power amplifier for NADC applications. This CMOS PA [10], which is intended for AMPS application, can provide 1 W of power with an overall efficiency of 42%. The linearized prototype system with this CMOS PA can meet the NADC requirements with an overall peak output power of 28dBm and peak PAE of 33%.

One of the critical linearity specifications for NADC PAs is the transmitted spectral mask. Fig. 14 shows the output spectrum of the switched-mode CMOS power amplifier with and without the linearization circuit. The spectral mask test was performed using a $(2^{15}-1)$ symbol pseudo-random NADC input signal generated by an HP8657D synthesizer. Without linearization, the PA is unsuitable for NADC applications because of the large out-of-channel emission. The linearization scheme reduces the adjacent channel power by more than 10 dB. Using the linearization circuit, the adjacent channel power of -30dBc, and alternate channel power of -48dBc meets the NADC requirements of -26dBc and -45dBc [3]. Similar results were obtained for the GaAs amplifiers discussed previously.

Fig. 15 shows the constellation of the CMOS PA with and without linearization as measured by an HP89441A vector signal analyzer. Without linearization, large error is evident in the $\pi/4$-QPSK constellation. The linearization system shows significant reduction in both magnitude and phase error. For peak output power of 28dBm, the linearized system has a measured error vector magnitude of 3.4 % rms, magnitude error of 2.5 % rms, and a phase error of 1.3 ^{o} rms.

V. CONCLUSION

The experimental results show that a monolithic implementation of an envelope elimination and restoration system can provide linear RF power with high efficiency. When applied to CMOS and GaAs switched-mode PAs, the prototype systems can provide greater than 28dBm of linear output power with 33% to 49% overall efficiency. In each case, the performance with the linearization circuit is significantly better than the amplifiers can achieve on their own.

This CMOS linearization IC consists of an efficient switching power supply, an envelope detector, and a limiter. The switching power supply uses delta modulation to achieve high efficiency over a wide signal bandwidth. The envelope detector employs a pseudo-replica circuit to reduce the distortion introduced by the gate to-source voltage of an NMOS transistor. Limiting is performed using a variable gain amplifier to avoid requiring large signal gain at RF. This design is amenable to integration in a low-cost CMOS technology and makes linearization affordable for hand-sets.

An additional benefit of the EER approach is that the overall efficiency remains high over a wide range of output power. This is important in hand-sets that must implement power control, as in advanced NADC or CDMA cell phones. Amplifiers in these applications may spend much of their time at lower output power levels, and increased efficiency at lower power levels will substantially increase battery life.

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FIGURE CAPTIONS

Fig. 1 Simplified output stage of an RF power amplifier.

Fig. 2 Classical definitions of RF PAs.

Fig. 3 (a) Conceptual block diagram of envelope elimination and restoration system. (b) current implementation.

Fig. 4 (a) Block diagram and (b) schematic of switching power supply

Fig. 5 Simplified schematic of comparator preamplifier.

Fig. 6 Measured spectrum of switching power supply output.

Fig. 7 Envelope detector.

Fig. 8 Measured performance of envelope detector.

Fig. 9 Block diagram of limiter.

Fig. 10 Simplified schematic of variable gain amplifier.

Fig. 11 Measured performance of limiter.

Fig. 12 Die photograph.

Fig. 13 Measured efficiency of (a) 3.3-V GaAs PA (b) 4.8-V GaAs PA.

Fig. 14 Measured spectral mask of CMOS PA.

Fig. 15 Measured $\pi/4$ QPSK constellation of CMOS PA.

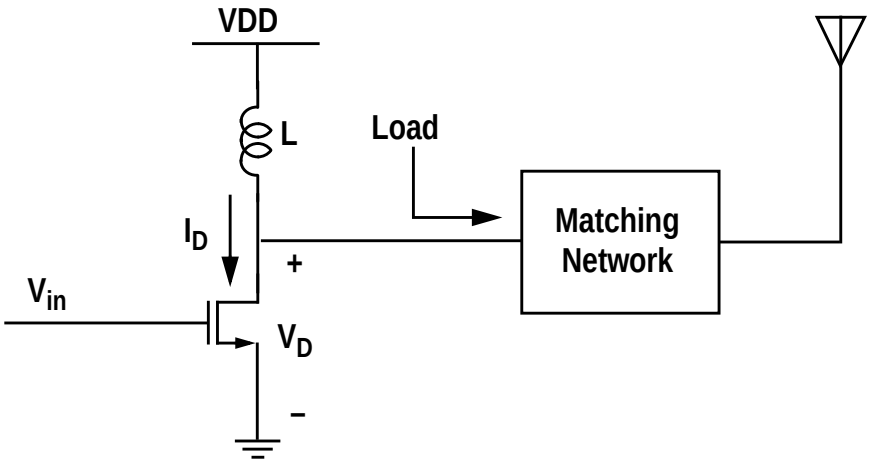

Figure 1: Simplified output stage of an RF power amplifier.
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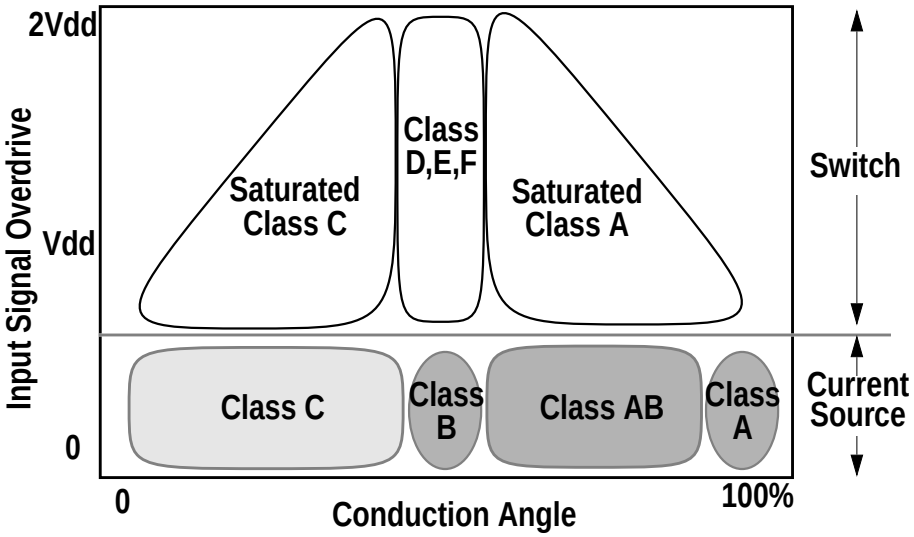

Figure 2: Classical definitions of RF power amplifiers.
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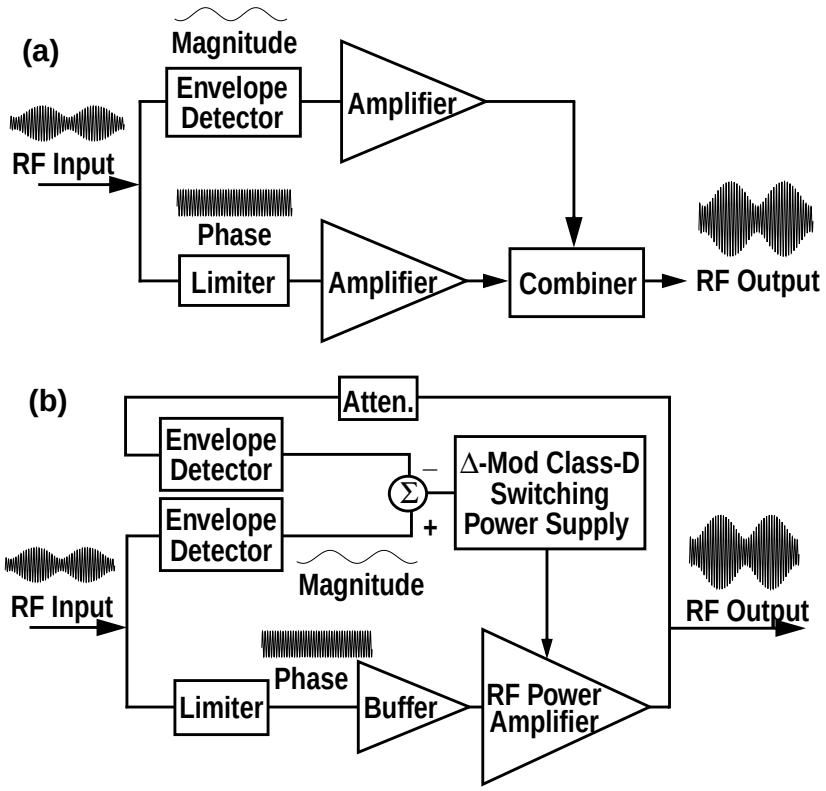

Figure 3: (a) Conceptual block diagram of envelope elimination and restoration (b) Current implementation

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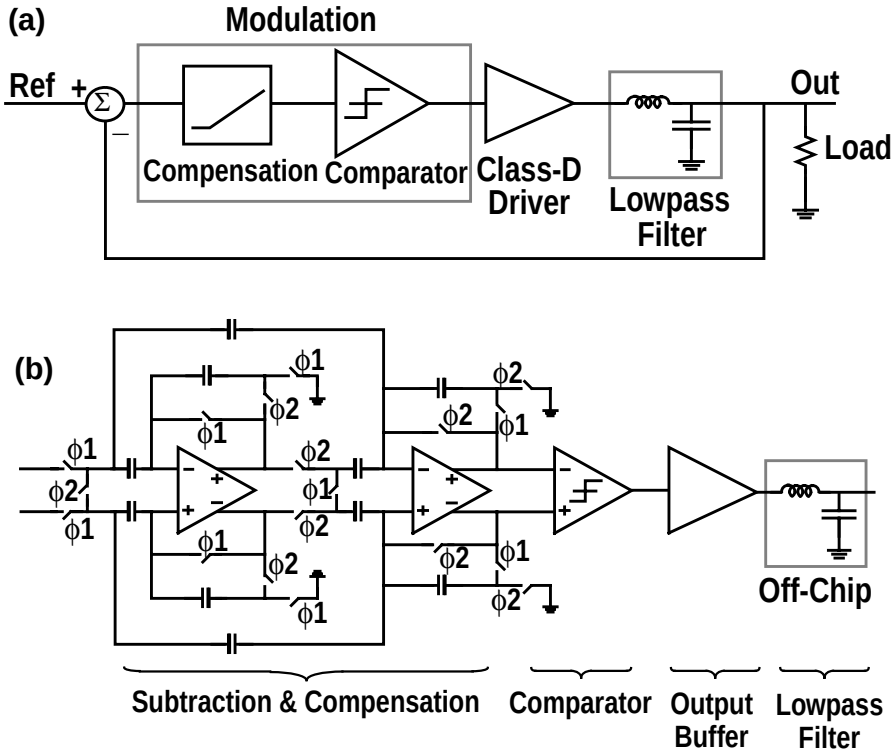

Figure 4: (a) Block diagram and (b) schematic of switching power supply.

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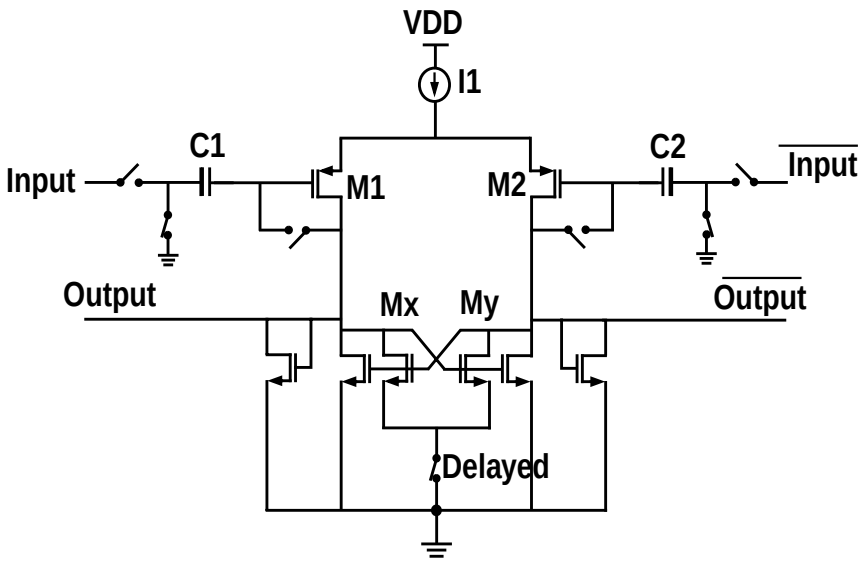

Figure 5: Schematic of comparator preamplifier.
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Supply Voltage	3.0V
Output Voltage	0.1 to 2.65V
Output Current	0.75 A
Bandwidth	100 kHz
Harmonic Distortion	–55 dBc
Efficiency	80%
Die Area	3.9 sq mm

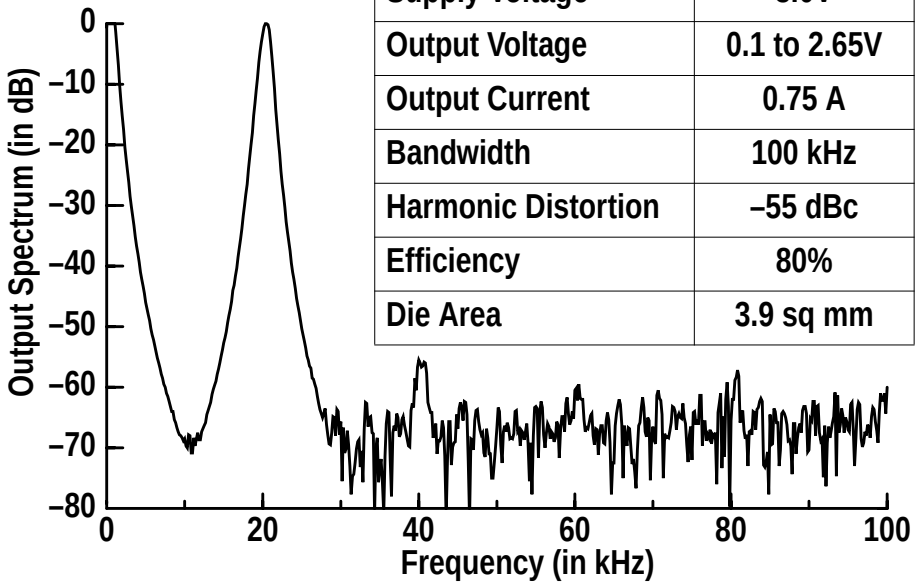

Figure 6: Measured spectrum of switching power supply output.
Su and McFarland

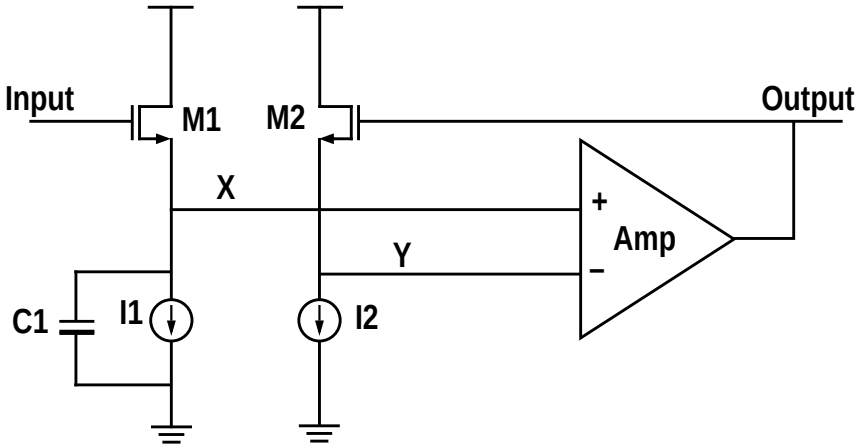

Figure 7: Envelope detector.
Su and McFarland

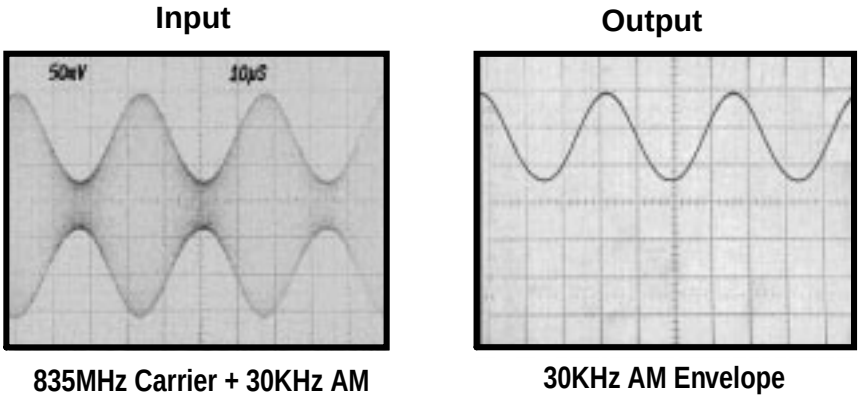

Figure 8: Measured performance of envelope detector.
Su and McFarland

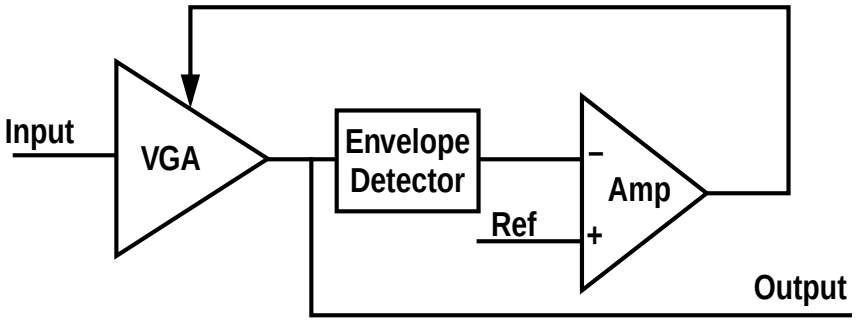

Figure 9: Block diagram of limiter.
Su and McFarland

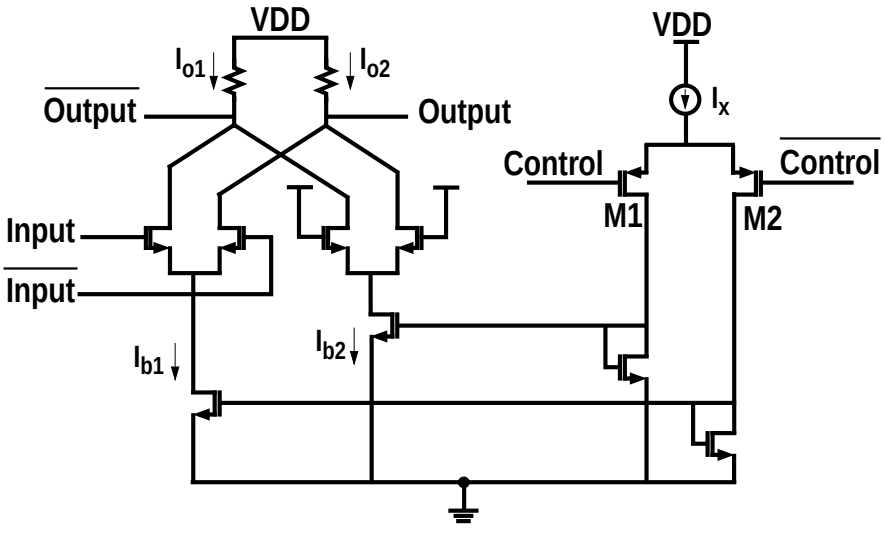

Figure 10: Simplified schematic of variable gain amplifier.
Su and McFarland

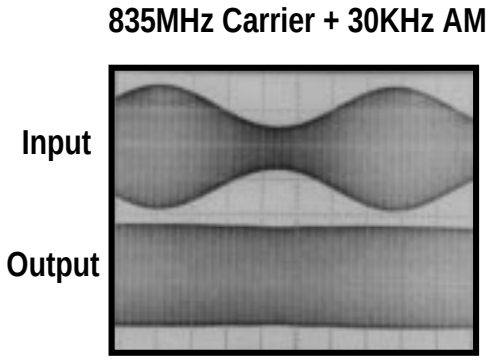

Figure 11: Measured performance of limiter.
Su and McFarland

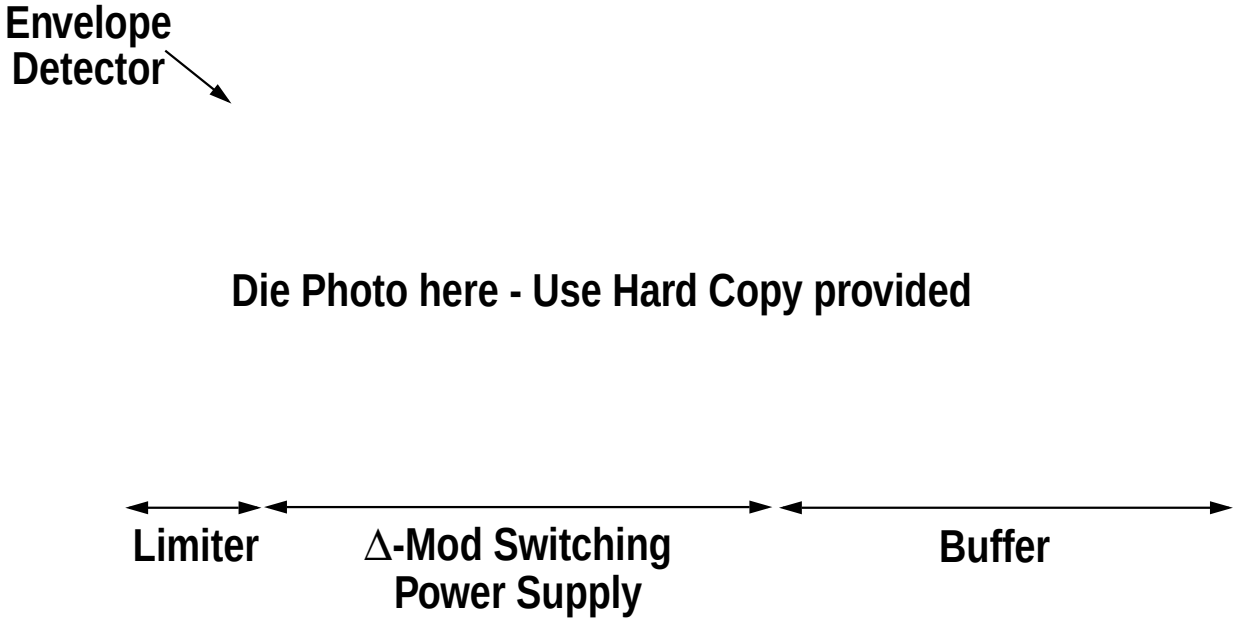

Figure 12: Die photograph.
Su and McFarland

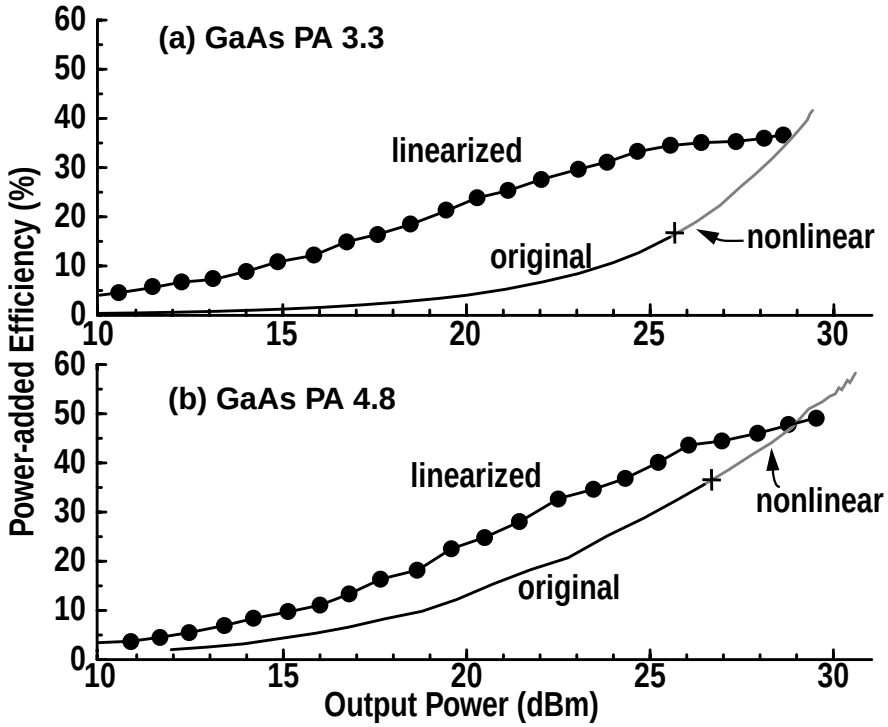

Figure 13: Measured efficiency of (a) 3.3-V Ga PA (b) 4.8-V GaAs PA.
Su and McFarland

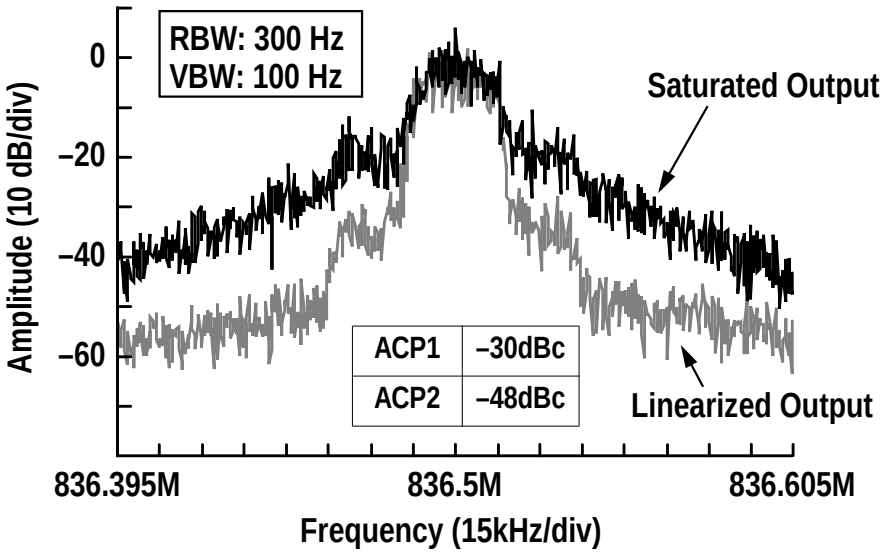

Figure 14: Measured spectral mask of CMOS PA.
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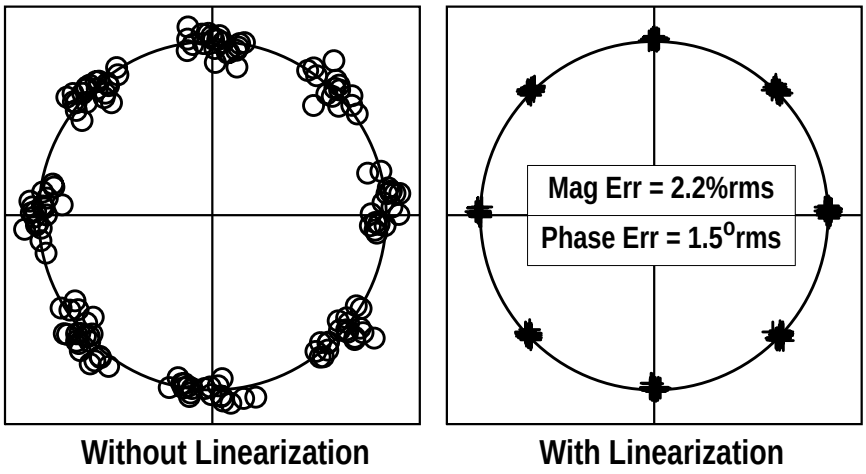

Figure 15: Measured $\pi/4$ constellation of CMOS PA.
Su and McFarland