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A 12 psec GaAs Double Heterostructure Step Recovery Diode

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We have fabricated a P^+-i-N^+ Double Heterostructure Step Recovery Diode (DHSRD) on $Al_{0.3}Ga_{0.7}As$/ $Al_xGa_{1-x}As$/$Al_{0.3}Ga_{0.7}As$ with > 14V amplitude and a (10 to 90%) transition time of ≤ 12 psec at a forward bias of 40mA. This is the fastest transition time reported for a DHSRD. The fast transition is due to the linearly graded bandgap $Al_xGa_{1-x}As$ undoped charge storage layer with grading from x=0 to x=0.15. The linear grading provides a quasi- electric field which confines the injected holes closer to the P^+ exit region and also provides a drift field to accelerate hole removal during the reverse recovery process.

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1 Introduction

Step recovery diodes (SRD's) are used primarily in generating extremely fast rise time pulses for use in frequency comb generation, harmonic frequency multipliers and samplers. In most applications, the SRD is used as a charge controlled switch. When forward biased, charge is injected into the diode making it a low impedance. When the stored charge is removed, the diode continues to have a low impedance until all the charge is removed at which point, the diode rapidly switches from the low to a high impedance. This property of the SRD to store charge and change its impedance level rapidly is used for the generation of extremely fast transition time waveforms. Moll *et al.* [1] proposed that the most ideal structure for a step recovery diode is an abrupt p^+-i-n^+ junction device. At forward bias, holes and electrons are injected into the intrinsic layer from the p^+ and n^+ contacts, respectively. The injected electrons and holes remain stored in the volume of the intrinsic region due to it's long minority carrier lifetime. This stored charge results in a large forward bias diffusion capacitance, C_{FWD}. When the stored charge from the i-layer is removed during reverse bias, the diode capacitance is a small capacitance C_{REV} of the depleted i-layer. The SRD is designed to have the fastest transition from C_{FWD} to C_{REV}. In this sense, the SRD is a practical realization of an ideal nonlinear capacitor.

The operation of the SRD as a pulse sharpener is illustrated in the circuit depicted in Figure 1. A forward current I_f is applied through the diode resulting in a stored charge $Q_s = I_f\,\tau$, where τ is the minority carrier lifetime. A step input voltage with a rise time shorter than τ is applied across the diode so as to reverse bias the diode. Initially, the large amount of stored electrons and holes will prevent the electric field from being developed across intrinsic layer keeping the voltage across the diode small. This stored charge provides for the large reverse current which keeps the diode voltage small. If the minority carrier lifetime is long enough, the current through the SRD will switch from I_f to a large peak reverse value of $I_r = V/R_{||}$, following the shape of the input signal. Ideally, once all the stored charge is removed from the intrinsic region, the current flowing through the diode transitions to a small space-charge limited reverse current. The speed with which the diode transitions from the peak reverse current I_r to the small space-charge limited current depends on the device structure and the external circuit that interacts with it. It is therefore possible to steepen a voltage edge so long as the input rise time is short compared to the minority carrier lifetime in the intrinsic layer.

In a SRD, the minority carriers injected into the intrinsic layer can be as high $1 \times 10^{18}\text{cm}^{-3}$ similar to a laser diode. Ideally, for SRD's fabricated on GaAs/AlGaAs, the minority carrier lifetime is limited by radiative recombination in the intrinsic region. The radiative lifetime in GaAs is around 3 nsec for the above injected carrier concentration [2,3]. For a double hetrostructure AlGaAs/GaAs/AlGaAs step recovery diode (DHSRD), this lifetime number may be increased slightly by photon reabsorption [4] in the GaAs active layer. However, fabricated devices with mesa structure do not approach this ideal lifetime number due to surface and heterointerface recombination.

The reverse recovery transition time of the SRD can be divided into several regimes. The first part of the step recovery is a "slow tail" portion due to the sweep out of the injected carriers by diffusion from their concentration gradients. This portion of the transition time is approximately given by the diffusion transit time $T_D = w^2/4D_a$ where w is the i-layer thickness and D_a is the ambipolar diffusion coefficient. For undoped GaAs D_a is dominated by the hole diffusion coefficient and is ≈ 9.4 cm^2/sec. After this time T_D, there is enough charge separation that an electric field starts to form in the intrinsic layer. This electric field will in turn assist in the sweep-out process of the confined carriers. This portion of the transition waveform will be limited by the saturated drift velocity in GaAs and is on the order of 10 psec/μm. Once all the injected charge is removed, the final portion of the transition time is due to the depletion of the background doping in the i-layer. This portion of the transition time is called the "round off" portion.

In a regular homojunction p^+-i-n^+ device, there is a substantial amount of minority carrier injection into the highly doped p^+ and n^+ regions with increased forward bias. This increases the effective charge storage layer width which results in an increase of the transition time with increased forward bias. While in the DHSRD, the double heterostructure confine the injected minority carriers only in the charge storage layer making it insensitive to transition time variations with the amount of charge storage or forward bias..

Previously, both SRD's and DHSRD's suffered from the initial "slow' diffusion tail during the reverse recovery process. This limited the transition time of Silicon SRD's to around 35 psec and 23 psec for DHSRD's [5]. In this work, we show that this "slow"diffusion tail portion of the transition time can be minimized substantially. Calculations using SEDAN3 [6] show that improved reverse recovery is obtained for both p-type and graded bandgap charge storage layers. In a p-type charge storage layer, the slow diffusion tail is minimized

due to the enhanced ambipolar diffusion. The fast transition for the current DHSRD is due to the linearly graded bandgap $Al_xGa_{1-x}As$ charge storage region with grading from $x = 0$ to $x = 0.15$. The linear grading results in a quasi-electric field which confines the injected holes closer to the P^+ exit region and also provide a drift field to accelerate hole removal during the reverse recovery process.

2 Material Structure and Device Fabrication

The DHSRD were grown in a Varian Modular GEN II MBE system equipped with a rotating 2 inch Indium-free substrate holder. The growth temperature T_s was measured using an optical pyrometer. The DHSRD were grown on a n^+ Si-doped $< 100 >$ oriented GaAs substrate. The growth temperature was $T_s = 620°C$ with a As_4/Ga beam flux ratio of 10:1 as measured by an ion gauge. The device structure is comprised of 0.8 μm of n^+ Si-doped GaAs ($5.0 \times 10^{18}cm^{-3}$), 0.2 μm of N^+ Si-doped $Al_{0.3}Ga_{0.7}As$ ($5.0 \times 10^{18}cm^{-3}$), 0.4 μm of undoped $Al_xGa_{1-x}As$ linearly graded from $x = 0.15$ to $x = 0.0$, 0.2 μm of P^+ Be-doped $Al_{0.3}Ga_{0.7}As$ ($5.0 \times 10^{19}cm^{-3}$), 0.3 μm of p^+ Be-doped GaAs ($1.0 \times 10^{20}cm^{-3}$). 12 , 10 and 8 μm radius $AuZn(5\%)$ p-type contacts were evaporated using standard photolithography and subsequent liftoff. A first mesa was wet etched using $NH_4OH : H_2O_2 : H_2O$ stopping about 1000 $\AA$ above the undoped charge storage layer. A second set of dots were patterned using photoresist which covered and extended beyond the top p-contacts by 3 μm. A second mesa was then etched through the charge storage layer stopping at the top of the bottom N^+ AlGaAs. The first mesa reduces the amount of current flow towards the exposed $Al_xGa_{1-x}As$ surface formed by the second mesa etch. In this way the surface recombination current may be minimized. The device structure schematic is shown in Fig. 2(a). 3 μm thick polyimide was used to planarize the device and top Ti/Au contacts were deposited. The top contact area was less than 2000 μm^2 keeping the parasitic capacitance to be less than 18 fF. The wafer was lapped down to less than 275 μm and $NiCr/Au/Ge/Au$ n-type ohmic contacts were used as backside contacts finishing the device. The diodes were then separated into 400 $\times$ 400 μm^2 squares and mounted into a 50 Ω suspended stripline package. DC blocking capacitors were incorporated into the transmission lines and precision grade 2.4mm connectors were used.

3 Devices and Characterization

The IV characteristics of the $10\mu m$ radius diode is shown in Fig. 2(b). The diode had an ideality factor $n < 2$ over 4 decades of current. This indicates that the forward current is dominated by recombination. A near linear dependance of forward current versus diode radius was found indicating the dominance of recombination at the diode periphery. The series resistance of the diode was less than 1.5Ω. The zero bias capacitance of the diode was around 156 fF and the capacitance at -10V was measured to be around 149 fF. The forward bias capacitance at 1.4V was measured to be around 3.5pF. The reverse breakdown of the diodes was around $17V$.

In Fig. 3 is shown the input step and the corresponding output transition obtained from a $10\mu m$ radius DHSRD. The input step was from a PPSL pulse generator with a (10 to 90 %) transition time of around 70 psec and a peak voltage of around 15 V. A forward bias current of around 40 mA was applied to the DHSRD using a bias tee. From Fig. 3 we can obtain the minority carrier lifetime as a function of forward bias current through the DHSRD. The amount of reverse current switched by the diode is approximately 600 mA assuming that the generator and load impedance to be around 50 Ω. The stored charge removed during the reverse recovery process is approximately 21 pC. Therefore, the DHSRD has a minority carrier lifetime of around ≤ 0.53 nsec at the forward bias of 40 mA. This lifetime is limited by surface recombination at the exposed diode perimeter and also nonradiative recombination in the $Al_xGa_{1-x}As$ charge storage region. The recombination in the $Al_xGa_{1-x}As$ storage region can be minimized by higher epitaxial growth temperatures. There is a tradeoff between minority carrier lifetime and power dissipation. Smaller values of τ results in higher current densities for the same level of charge storage and therefore higher power consumption. Also the amount of steepening available depends on the amount of stored charge available in the intrinsic layer. Thus longer lifetimes will allow for steepening pulses with slower edges and or higher amplitude step transitions.

In Fig. 4 is shown a blowup of the DHSRD transition time. The resulting step was steepened to a (10 to 90 %) transition time of < 13.6 psec with an amplitude of around 14.2 V as measured on a HP54124 50 GHz oscilloscope. This corresponds to a deconvolved rise time of around 11.7 psec assuming the sampling scope rise time of around 7 psec. This rise time is the averaged rise time measured which includes the low pass effects of any extraneous jitter. The effect of jitter can be removed from the measurement by measuring the mean (10 to

90 %) rise time using the histogram mode of the sampling scope. The resultant mean rise time was measured to be 12.2 psec. This corresponds to a deconvolved rise time of 10 psec. In estimating these rise times, the rise times of the package and 2.4mm coaxial attenuators were not accounted for.

In order to show the effectiveness of the linear grading we also fabricated a P^+-i-N^+ $Al_{0.3}Ga_{0.7}As$/ GaAs/$Al_{0.3}Ga_{0.7}As$ DHSRD with an ungraded GaAs (undoped) charge storage region with the same growth condition as the previous structure. For this structure, the minority carrier lifetime was increased by a factor of four. However, the transition time measured for the same $10\mu m$ design under the same drive conditions was around 27 psec.

4 Conclusions

In summary, we have developed a double heterostructure step recovery diode with (10 to 90 %) transition times of < 10 psec and amplitudes in excess of 14.2V. From these results, we feel that it would be possible to fabricate DHSRD's with transition times of ≤ 5 psec and amplitudes in excess of 8V.

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5 References

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Figures

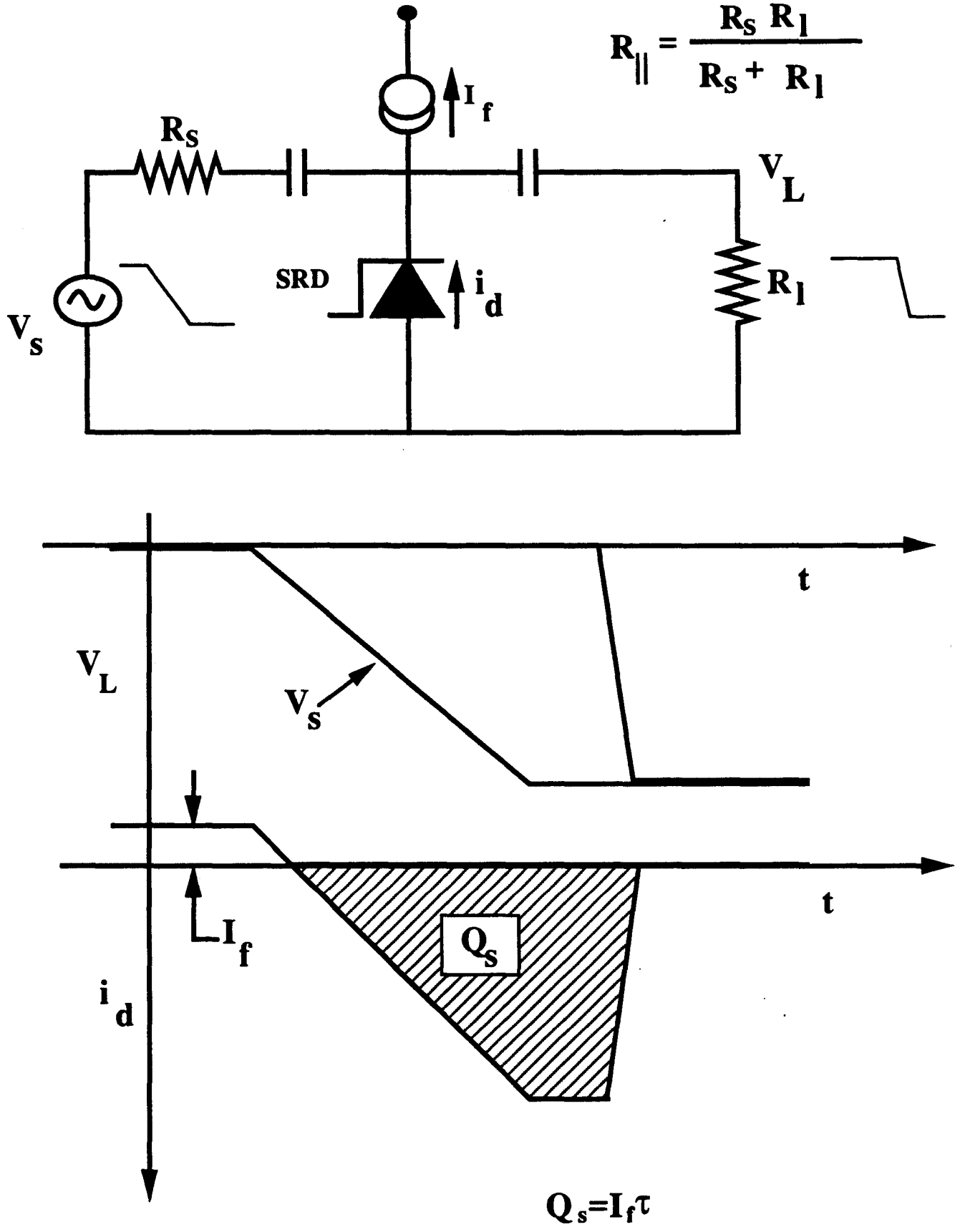
Figure 1. SRD Step Generator and Waveforms.

Figure 2(a). DHSRD device structure.

Figure 2(b). I-V characteristic of 10 μm radius DHSRD.

Figure 3. Step Recovery of DHSRD and input drive waveforms.

Figure 4. 13.6 psec transition time measured on HP54124 50 GHz sampling oscilloscope.


$R_{\parallel} = \frac{R_S R_l}{R_S + R_l}$
I_f
R_S
V_L
SRD
i_d
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t
I_f
Q_s
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$Q_s = I_f \tau$

Figure 1

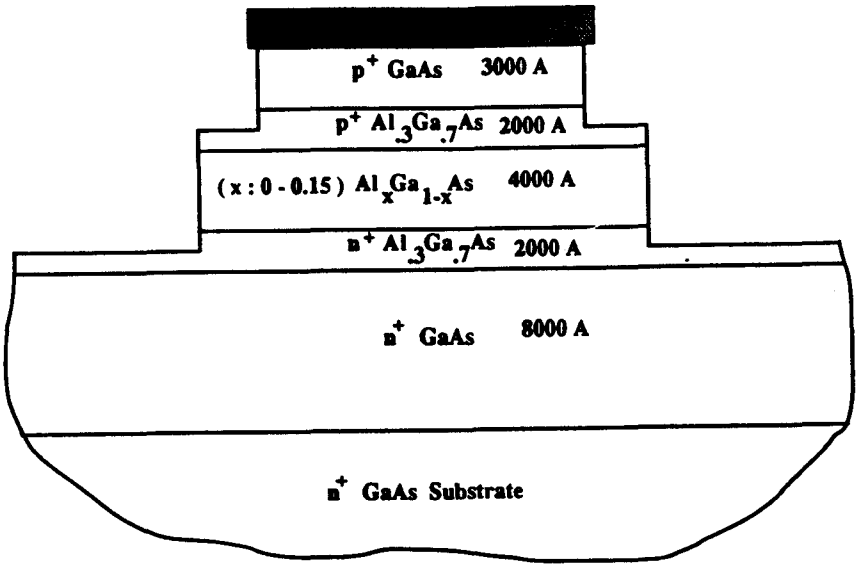

Figure 2 (a)

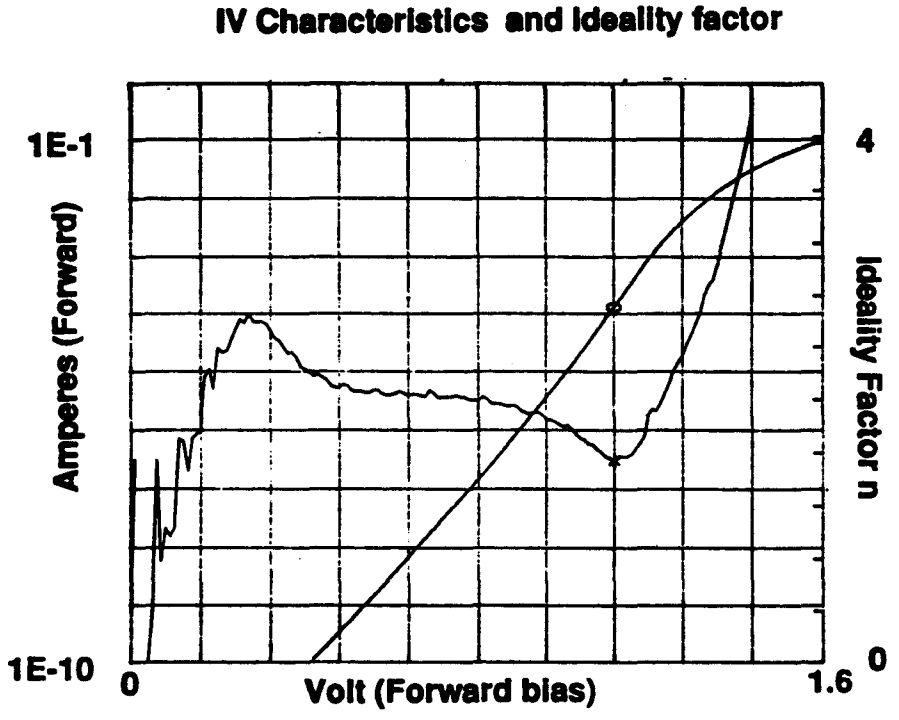

Figure 2 (b)

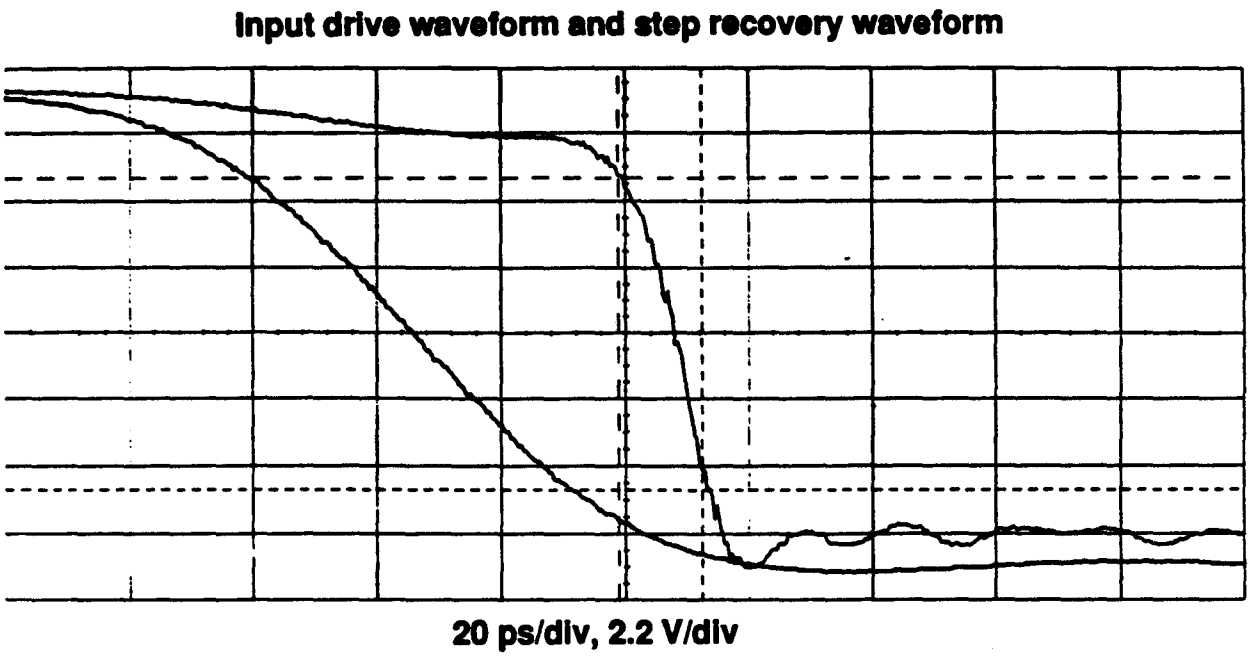

Figure 3

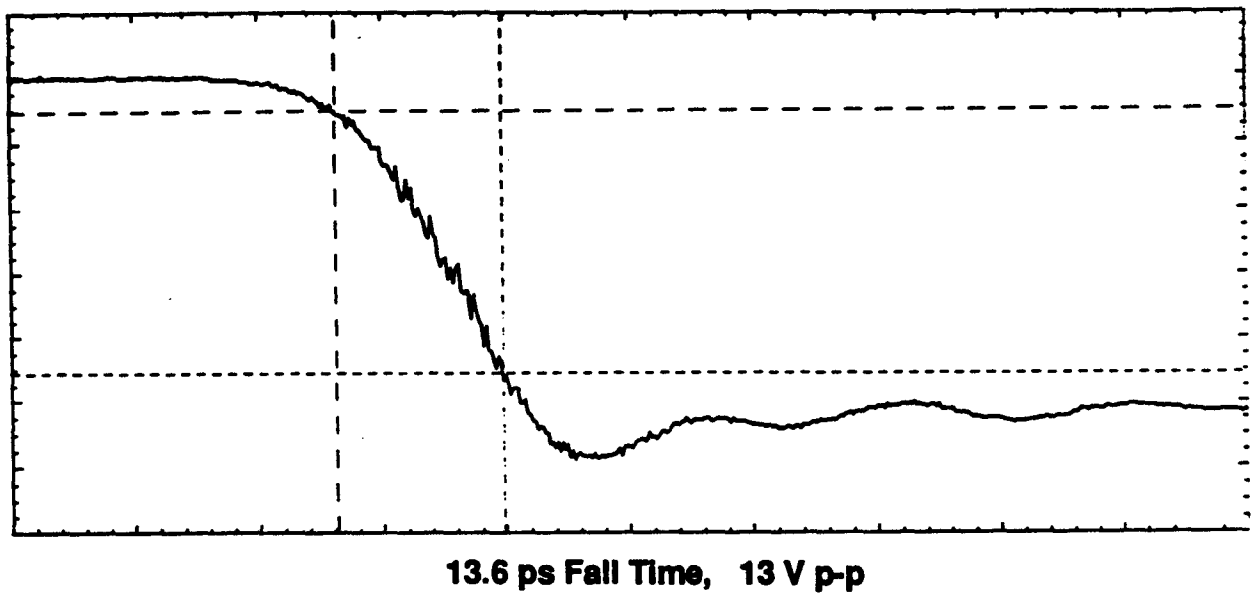

Figure 4