High Current Density in µc-Si PECVD Diodes for Low Temperature Applications

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ABSTRACT

The development of microcrystalline diodes grown at low temperature by PECVD techniques is reported. Current densities near 200 A/cm^2 at + 2 V, and rectification ratios on the order of 10^5 at +/- 1V and 10^7 at +/- 2V were obtained. The reverse currents were in the nano-ampere range. Correlations between deposition conditions and film quality are presented. The effects of mesa formation and subsequent treatments designed to reduce process damage are discussed: annealing conditions yield an increase in forward current, and a decrease in reverse current. Fabrication conditions are compatible with applications requiring low temperature processes (e. g., multi-layer structures, molecular layers, or plastic substrates and coatings).

INTRODUCTION

Low temperature processes are desirable for emerging technologies. The high temperatures required for LPCVD deposition of polysilicon (600 ^{o}C) or amorphous (525 ^{o}C) Si (and to some extent, hot-wire processes) are incompatible with emerging applications incorporating organics, metals and layered circuit structures, which require low temperature processing. PECVD presents a viable alternative. Cross point array architecture for magnetic and moletronic memory applications are currently under development [1, 2]. In the simplest configuration, with the memory element sandwiched between two conductors, the sense amplifiers have high precision requirements needing sophisticated and costly CMOS structures. Incorporation of a series diode within the memory cell relaxes the constraints on the sense electronics, improves performance, cost structure and achievable density. The diode must be formed at low temperature and on amorphous underlayers, requiring the use of amorphous (α) or microcrystalline (μc) Si devices.

The diode requirements include ~1000 A/cm^2 forward current density (J_F), ~10^5 rectification ratio (RR), and GΩ resistance at low forward voltages [3]. J_F and RR in α-Si or μc-Si p-i-n diodes are not often reported (as applications are usually for solar cells); the highest values in the recent literature are 0.1 A/cm^2 at 700 mV [4] and 0.1 A/cm^2 at 1.2 V [5] with no RR noted. We report an improvement in forward current densities in μc-Si p-i-n diodes to 180 A/cm^2 with rectification ratios greater than 10^6 at +/- 2 Volts.

EXPERIMENTAL DETAILS

Figure 1 shows the diode structure. The substrate was a 6" <100> Si wafer / 100 nm PECVD SiO_2 / 100 nm evaporated Cr (CHA system). All Si depositions were performed in an Applied Materials P5000 PECVD operated at 13.56 MHz. A brief sputter etch of Cr was performed to remove the CrO_x layer. The deposition chamber was cleaned and conditioned before each run, as well as between the n-type and intrinsic depositions. The wafer was transferred in vacuum to the deposition chamber, where n: α-Si / i: (α + μc)-Si / p: α-Si were deposited. Film thickness was determined by either reflectivity (Prometrix UV 1050) or profilometer (DEKTAK^3 ST) measurements.

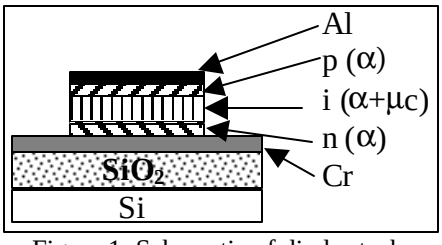

Figure 1: Schematic of diode stack

Diodes were defined by metal deposition and subsequent dry etch. A photolithographic lift-off process produced arrays of 101 elements each of diameters of 10 μm, 20 μm, 40 μm, 80 μm, 160 μm, 320 μm and 640 μm. 100 nm of Al was deposited in an SFI magnetron sputtering system after Ar clean (5 min.). After lift off, the aluminum features were used as an RIE etch mask (CHF_3 7.5 sccm; O2 0.4 sccm; 40 mT; 75 W). The unpatterned Cr bottom contact was the etch stop.

Two different, sequential anneals were performed subsequent to mesa definition, the first was in the P5000 system (P5000 anneal) with a H:N (1:10), gas flow and a the second in a tube furnace with H:Ar (5%:95%) for 10 hours ("forming gas" anneal FGA). Electrical characteristics of the diodes were measured after each process. The P5000 anneal consisted of a short hydrogen plasma scrub (180 sec.; 30 W; 200 ^oC; 340 sccm H_2) followed by an in-situ anneal (3600 s; 0 W; 180 ^oC; 340 sccm H_2; 3400 sccm N_2). The FGA (180^o C; 10 hours; 5% H_2 in Ar 10 sccm) was performed on the smaller devices (20 μm, 40 μm and 80 μm).

The Raman microscope used was a Renishaw Ramascope 2000, with a 35 mW (3.3 mW at the sample for 100% power) 514 nm Argon laser, 1200 line grating, backscattering geometry with a 5 μm spot size. Acquisition time was 10 seconds for 3 accumulations and a binning of 1 for most of the spectra. Penetration depth in α-Si (based on the data collected) was extrapolated to 825 nm.

Electrical characteristics of full diode structures, as well as individual n and p layers, were measured on a Signatone semi-automatic probe station connected to an Agilent 4155C Semiconductor Parameter Analyzer. It was programmed to use a two point I-V measurement over the arrays, sweeping voltage from –2 V to 2 V with integration time of no less than 640 μs .

MATERIALS RESULTS

Current density is optimized in microcrystalline Si p-i-n junctions [6]. Deposition parameters (gas flow, pressure, H dilution, temperature, spacing and power) were adjusted to optimize μc-Si content. Microcrystalline formation is reportedly obtained in the SiH_4 depletion region, which occurs when the film deposition rate saturates with increasing power. This region purportedly coincides with the onset of the mixed phase (α + μc) region [7].

Figure 2a shows this curve for intrinsic Si. Deposition conditions are [SiH_4]=15 sccm; [H_2] = 1500 sccm; T = 220 ^oC; spacing = 500 mils. There is a clear saturation region occurring at 0.91 W/cm^2. Figure 2b shows the μc-Si content as determined by Raman analysis, with the highest μc-Si content of 68% at 0.45 W/cm^2, monotonically decreasing with increasing deposition power. This is contrary to expectations, as the onset of the mixed phase region is expected at the onset of the saturation region at 0.91 W/cm^2, if the model of Collins et al. is valid under these deposition conditions [7]. Similar curves were obtained for the n- and p- type materials; the deposition conditions for each layer in the subsequent diode deposition were chosen at the power corresponding to the saturation condition (prior to Raman studies).

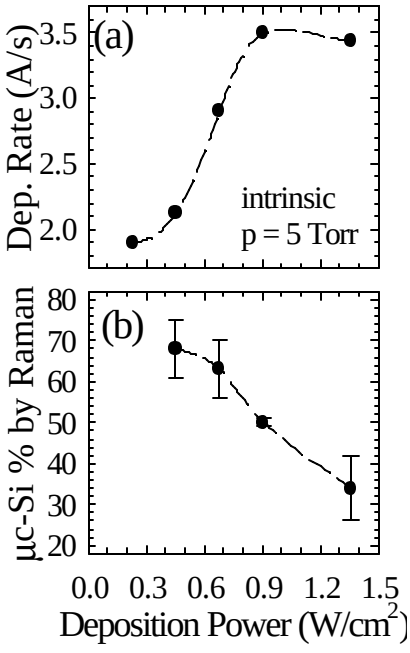

Figure 2: (a) Intrinsic Si deposition rate as a function of power. (b) μc-Si content as determined by Raman spectroscopy. Lines are guides.

Figure 3 shows the μc-Si content as determined by Raman spectroscopy as a function of silane dilution. Even though other deposition parameters changed in these experiments (power, gas flow), this data shows that microcrystalline content is primarily determined by dilution. This agrees qualitatively with the result of Collins and Ferlauto [7], however the scale of this result differs greatly: they find μc-Si formation at dilution ratios ($R=[H_2]/[SiH_4]$) of ~80 and thickness of 100 Å, whereas we require much higher dilution ratios even for 1600 Å thick samples. One explanation for the discrepancy is the difference in substrate: their depositions were on crystalline Si, whereas ours were on Cr or SiO_2.

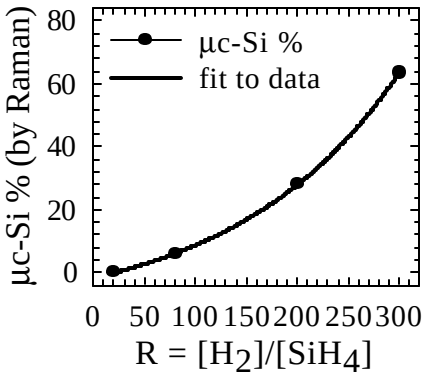

Figure 3: μc-Si content as determined by Raman spectroscopy as a function of silane dilution.

Table I: deposition parameters for diode stack.

layer	PH_3 (sccm)	B_2H_6 (sccm)	SiH_4 (sccm)	H_2 (sccm)	R	Power (W)	T (^oC)	Spacing (mils)	Pressure (Torr)
n	2	-	5	1000	200	240	220	500	5
i	-	-	5/5	1500/1000	300/200	240/40	220	500	5
p	-	2	5	1500	300	240	220	500	5

Combining the result of Figure 3, showing μc-Si content is primarily dependent on dilution level, with the result of Figure 2b, showing decreasing μc-Si content with increasing power, we conclude the optimal deposition condition for i: μc-Si is high dilution and low power.

Table I shows the deposition conditions for the n-, i- and p- layers for the sample whose diode characteristics are reported in the following sections. The i-layer is a mixed phase region, deposited in the manner of Wang et al. [8].

ELECTRICAL RESULTS

Measurements were made at 295 ^oK in semi-darkness (blanking display screens decreased the reverse current by 50x) after each process step: mesa definition, P5000 anneal, FGA. Measurements were made with a common ground to the wafer edge and a probe to the p-layer and differed little from data taken with two close probes; sheet resistance of the lower contact is not a dominant factor.

Figure 4 displays curves for diodes of (a) 40 μm and (b) 20 μm diameters. Reverse current decreases and forward current increases after each step. Post anneal, forward current increased 1000x while the reverse current

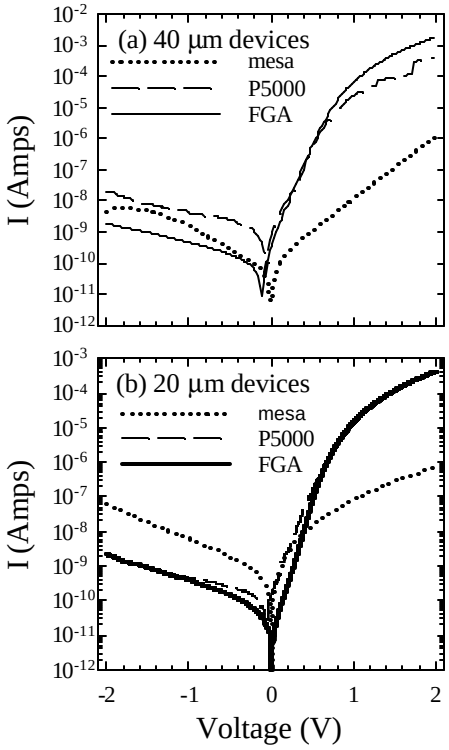

Figure 4: I-V characteristics of patterned mesa (dotted); after P5000 anneal (dashed) and after FGA (solid) for (a) 40 μm device (b) 20 μm device.

decreased nearly 100x to the nA range in 20 μm devices and over 10x in the 40 μm devices, relative to the patterned mesa results.

P-n junction diodes showed poor rectification, this is expected and attributed to high defect densities in the doped α -Si layers [9]. It is believed that an undoped layer will have fewer defects than a doped layer, therefore the addition of an i-layer between the p and n regions should diminish tunneling currents and improve diode characteristics. However, our FTIR data [10] shows that the doped α-Si materials have very low concentration of di-hydride bonds, indicating a lower defect density than the intrinsic α-Si material [11].

Figure 5 shows average current density (100 devices per point with distribution bars) plotted versus device area at 1 V and 2 V for the patterned mesas and after subsequent anneals. At 2 V the unannealed devices show flat or decreasing current density (J_F) from 10 μm to 40 μm and then increasing J_F with larger device size. The P5000 anneal increases J_F markedly in the smaller devices, with less effect on the larger devices, such that the curve J_F now decreases with increasing size, and the larger devices no longer have higher J_F than the smaller devices. This would be consistent with the hydrogen plasma acting on the exposed perimeters of the diodes, renewing the surface and passivating edge damage. For smaller devices, with large perimeter to area ratio, leakage current becomes more important (the 160 μm devices are anomalous, possibly due to local defects). The FGA anneal does not significantly further improve the forward current density, but it does improve the uniformity. We expect the upper region (>1V) of the I-V curve to be dominated by series resistance, e. g. probes, leads, materials and interfaces within the stack [12, 13]. Since J_F does not remain constant, and therefore resistance does not scale with area, the roll over of J_F at high V must be due to a characteristic external to the diode (e.g., point contact or lead line). If it were due to a resistance contribution from either a material layer or metal / semiconductor contact, it would scale with device area. This factor plus the presence of a thick α i-layer below the μc layer would lower the entire curve. The v-shaped nature of the initial curve, indicates there are multiple influences which require further study. Reducing the diameter by 2.5 μm to account for RIE undercut increases J_F in the 20 μm devices to over 180 A/cm^2.

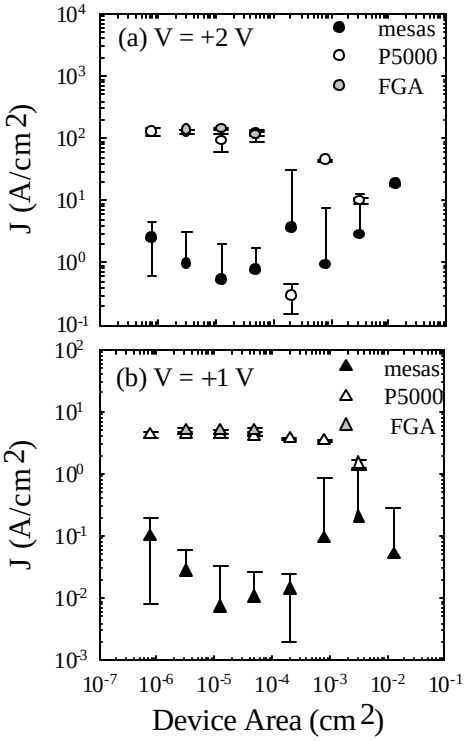

Figure 5: Current density vs. device area for forward bias of (a) +2 V; (b) +1 V.

Around 1 V, where the diode is expected to be fully on, the curves of the annealed devices are more regular. The as-patterned devices still display the same competing trends (flat to negative slope through the smaller devices and positive slope through the larger devices). Annealing improves all devices here with the largest gains in the smaller devices. The curve flattens and J becomes independent of area for all but the largest devices. Further study will be required to fit the rollover of the P5000-anneal curve to extract a value for R_{series} in Eq. 3.

The reverse current is plotted in Figure 6. While the anneals improve uniformity and lower current density, the situation is more complicated. The negative slope of the curves among the smaller devices is greater than -½, suggesting that defects, rather than perimeter leakage,

dominate the reverse current. The overall v-shaped dependence of the curves indicates two competing effects.

Forward current density is given by

$$J_F(V_A) = J_0[\exp(qV_A/nk_BT) - 1] \quad (1)$$

where q is the electron charge, V_A is the applied voltage, n is the ideality factor, k_B is Boltzmann's constant and T is the temperature (degrees Kelvin) [14]. In forward bias $qV >> k_BT$ and Eq. 1 is more commonly expressed as

$$J_F(V_A) = J_0\exp(qV_A/nk_BT) \quad (2)$$

Or

$$J_F(V_A) = J_0[\exp(q[V_A - R_{series}\,JA]/nk_BT)] \quad (3)$$

V_A in Eq. 1 is the applied voltage to the diode. In the test system

$$V_A = V_d + IR_{series} = V_d + JAR_{series} \quad (4)$$

voltage is applied to both the diode V_d and across the resistance in the system R_{series}. R_{series} includes resistance associated with probing the device (contact to the metal, surface oxide, tip debris), connections/lead lines, plus that of the diode materials themselves and the interfaces between them.

In Figure 7, the normalized forward current density is plotted versus voltage in the manner of Phillips [12] to facilitate extraction of the slope (fit yields: a = 1.74; b=15.88). On the normalized curve the slope corresponds to:

$$b = q/nk_BT \quad (5)$$

Solving for n yields an ideality factor of 2.48. While for an ideal crystal silicon diode n equals 1, amorphous material produces values >2. Kroon et. al [15] theorize that values larger than 2 are obtained when the splitting of the quasi-Fermi levels is smaller than the applied voltage and occurs when recombination is spread out over a wide region. The devices under study have a thick i-layer and we believe areas of uniform defect density, which would be in keeping with this argument.

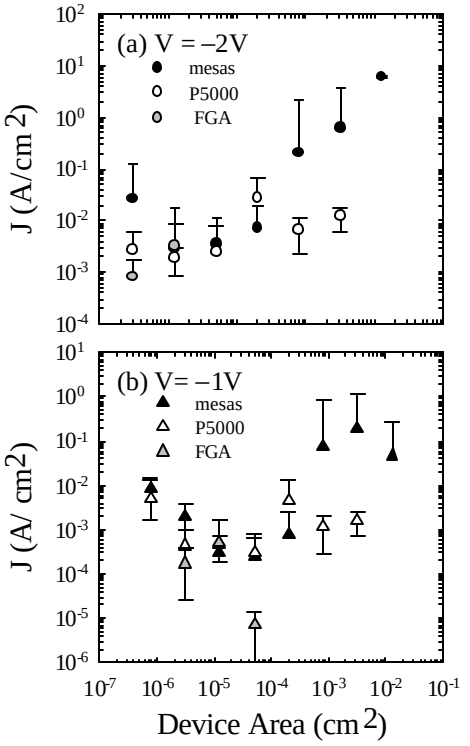

Figure 6: Current density vs. area for (a) –2 V and (b) –1 V bias.

SUMMARY AND FUTURE WORK

Although leakage is not dominating, device characteristics may be improved by passivation of exposed sidewalls to reduce perimeter leakage current, especially in smaller diodes (large perimeter relative to area). Passivation may be achieved with a silicon nitride covering or by etching only through the p-layer.

Anneals that improve device performance also usually improve device contact (e. g. forming gas anneal

at 400-500 ^{o}C or RTA). With these low temperature devices, however, the p-contact is not annealed in the manner of bulk silicon devices. Efforts will be made to decrease contact resistance at both the metal/silicon and probe/metal interfaces. In addition we will fit the diode curves to extract a resistance. Optimum anneal time as well as gas composition will be evaluated to determine which parameter has greatest effect: carrier gas or time at temperature. Kroon et al. theorizes that structures, when grown in the sequence n-i-p as in the devices of this study, have an incomplete defect equilibrium at the p-i interface. Anneals may be acting on this. FGA-type anneals will also be performed directly without an intermediate hydrogen plasma.

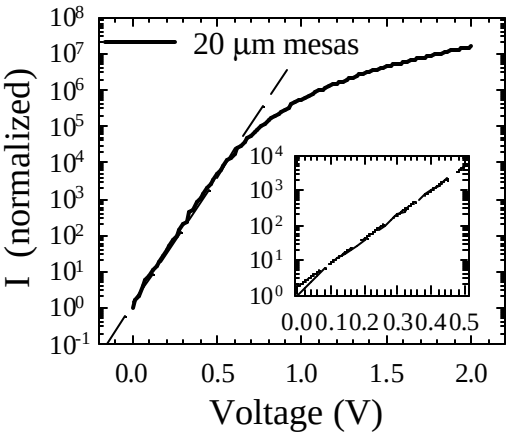

Figure 7: Normalized current for 20 μm device vs. voltage (solid). inset: slope in low V linear region (solid) and fit (dashed): y = a exp (bx)

Data indicates that device performance is defect limited. Forward current density could be improved by nucleating the μc-i-layer sooner, thereby decreasing the thickness and resistance of the underlying α–i-layer. Initial efforts show promise and steps will be taken to improve performance. Among them are: passivation, improved contact and improved μc-Si nucleation.

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