Self-Assembled TiSi_x Nanostructures formed by Chemical Vapor Deposition

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Outline

- Motivation
- Ti deposition
- Island formation during deposition
- Island modification during annealing
- Nanowire growth
- Nanowire alignment





Moore's (Second) Law and Self Assembly

- The **cost** of IC fabrication facilities continues to increase
- Much of cost relates to **lithography** of very small features
- Using **self-assembly** to form the smallest features can potentially reduce the escalating cost
- Coarser lithography can be used to position the fine features formed by self-assembly
- Features formed **thermodynamically** will have large numbers of defects
- Coupling self-assembly with a defect tolerant computer architecture is attractive





Deposition from TiCl₄





Lower Temperatures (T<700°C)













Islands after Deposition

Large (7%) lattice mismatch \rightarrow island formation





Atomic-Force Micrographs









Annealing of CVD TiSix Islands



During annealing

Amount of Ti on surface remains the same Island density decreases Islands take characteristic shapes





Islands after Annealing TiSi₂ on Si(001)



3×10¹⁴ Ti/cm²



 1.5×10^{14} Ti/cm² (1 µm × 1 µm images)



3×10¹⁵ Ti/cm²

After annealing

Island size depends only weakly on the amount of Ti Island density increases with increasing amount of Ti





Island Density after Annealing







Plan-View TEM: TiSi₂/Si(001) Three Island Types



Most numerous islands Flat-top Square or rectangular Mostly recessed into surrounding surface (C49 TiSi₂)

Transmission electron micrograph courtesy of D. P. Basile and M. Wong of Agilent Technologies





Cross-Section TEMs: TiSi₂/Si(001) Embedded Islands







Islands mainly recessed into the surrounding Si surface The period of the structure at the TiSi₂/Si interface corresponds to the difference in lattice constant.



Transmission electron micrographs courtesy of D. P. Basile and M. Wong of Agilent Technologies



Ti-Catalyzed Si Nanowires

Possible interconnections for molecular electronics

Forming wires

1) Form nuclei

Expose to vapor TiCl₄ at 600-700°C

TiSi_x islands form on Si(001)

by strain energy from lattice mismatch

2) Form nanowires

Expose to vapor SiH₄ or SiH₂Cl₂ at 600-700°C





Ti-Catalyzed Si Nanowires



Shallow-angle scanning electron micrograph



High-resolution transmission electron micrograph

Micrographs courtesy of Tor Hesjedal Stanford University





<u>Single-Crystal Si Wire</u> with TiSi_x at Tip

TiSi_x

Si



EDS analysis courtesy of Tor Hesjedal, Stanford University, and David Basile, Agilent Technologies











Surface-Reaction-Rate-Limited Growth

Initial Stage of Wire Growth



Subsequent Stage of Wire Growth







Higher Temperature

Uncatalyzed growth rate significant

Surface-Reaction-Rate Limited SiH₂Cl₂ at 920°C



Mass-Transport Limited SiH₄ at 920°C







Positioning Islands and Nanowires

Oxide-Patterned Si Substrate



Si TiSi₂ islands







/Si wires





Aligning Nanowires Using an Ion Beam

Sparse array: after deposition



Sparse array: after alignment









Aligning Nanowires Using an Ion Beam

Shadowed wires



Dense array after shadowed alignment







Summary

Ti deposition

Rate decreases as temperature decreases

• Island formation during deposition

Size decreases as temperature decreases Density varies only weakly with temperature

Island modification during annealing Islands coarsen

Nanowire growth

Ti catalyzes SiH₄ and SiH₂Cl₂ decomposition Ti remains at tip of growing wire

• Nanowire alignment using an ion beam



