Advanced Device Concepts and Research: Self-Assembled Nanostructures

Presented by
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Quantum Science Research
Hewlett-Packard Laboratories

www.hpl.hp.com/research/qsr

MSE Colloquium
Stanford University
November 15, 2002

Outline

Limits of Device Scaling

Alternative Device Concepts

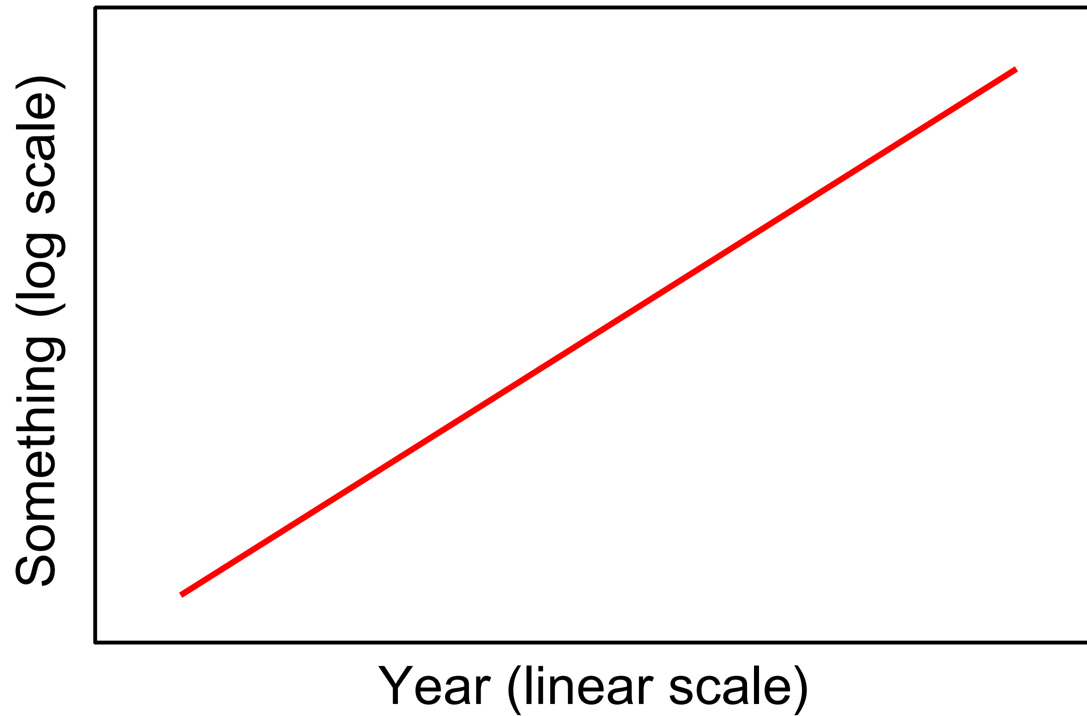
Self-Assembled Nanostructures

- Forming small structures
  - Putting them where we want them
- Zero- and one-dimensional structures
  - Catalyzed nanowire growth
  - Strain from lattice mismatch
- Nanowire transistor (speculation)

Enabling Concept

- Defect Tolerance

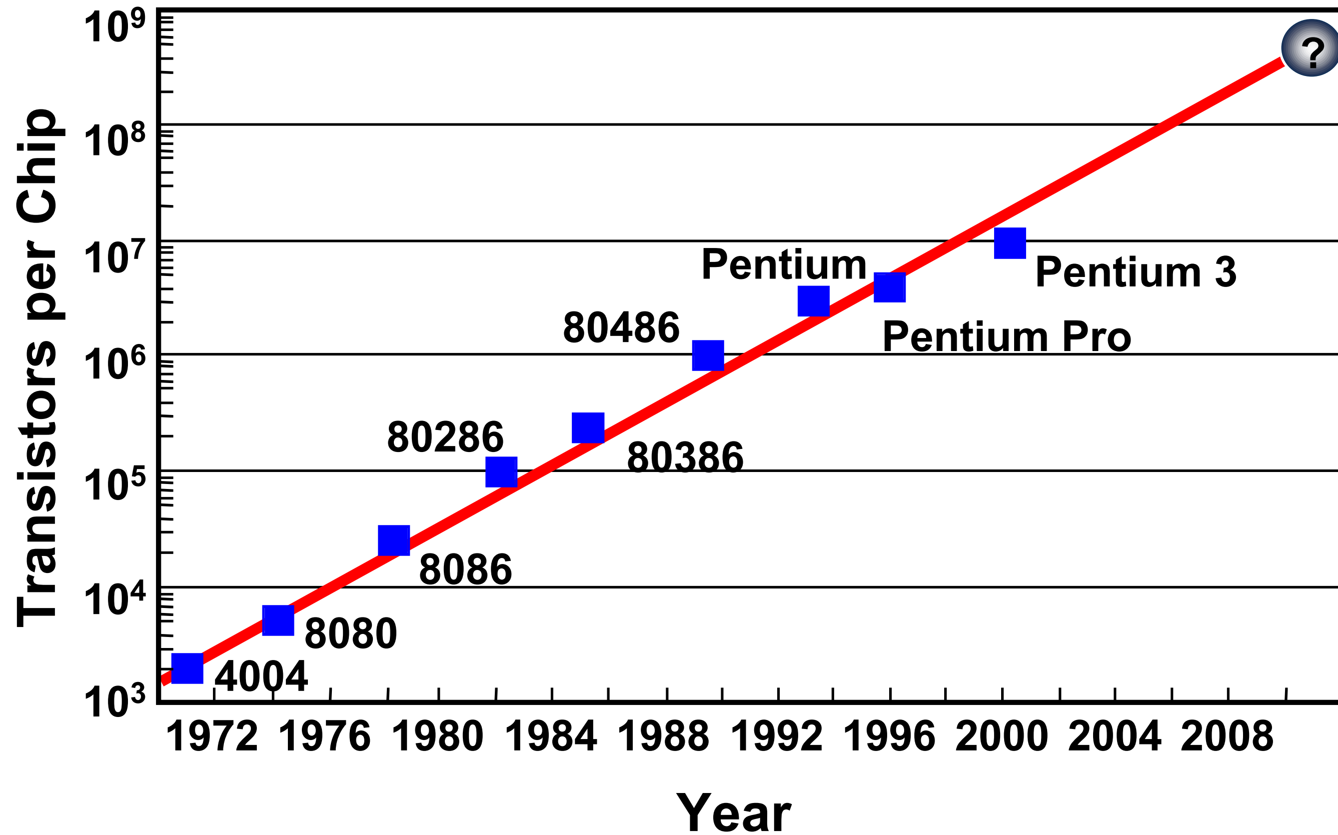
Moore's Law (General Case)



Even Dilbert uses Moore's Law

(Reference: Scott Adams “Dilbert,” July 15, 1997)

Moore's Law
Number of Transistors

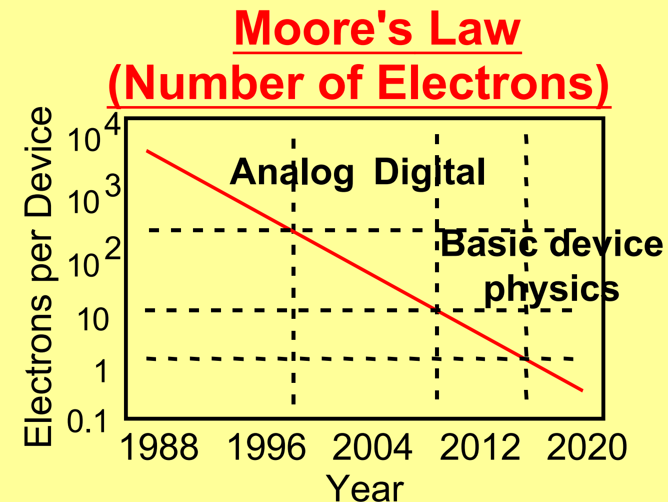


Critical Issues

Device size and density

- Physically small features
- Operation with small features
- Limited number of electrons
- Interconnections

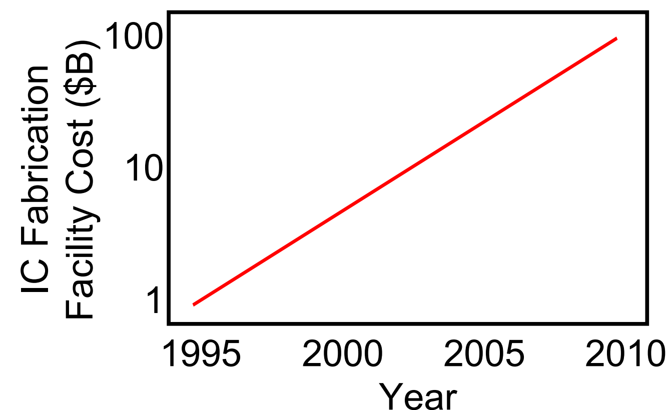
Moore's Law (Number of Electrons)



Cost

- Minimize expensive lithography
- Self (or directed) assembly
- Simpler architecture
- Defect-tolerant architecture

Moore's "Second Law" Cost of IC Fabrication Facility



Potential Devices

Single-electron devices
Quantum cellular automata
Molecular electronics
Quantum computing

Single-Electron Device

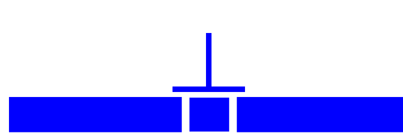
Minimum number of electrons

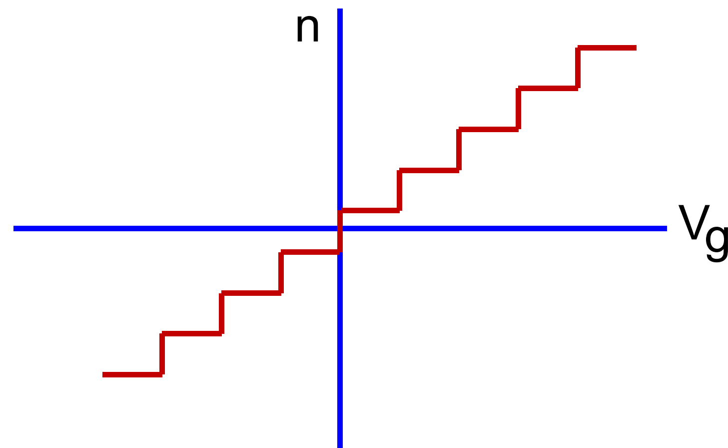
Coulomb blockade

- Energy to add single electron
  - $E = q^2/2C$
  - 1 aF ~ 80 meV ~ 3 kT at 300 K

Can control charging by gate electrode

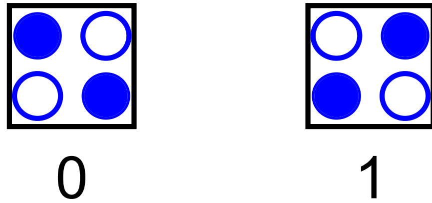
Sensitive to fractional background charge



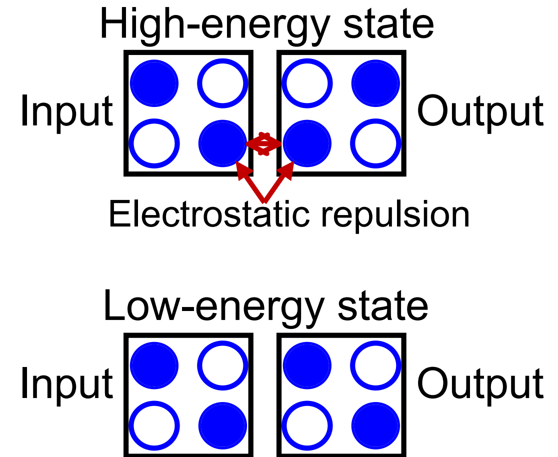


Quantum Cellular Automata

Cell with two possible polarizations

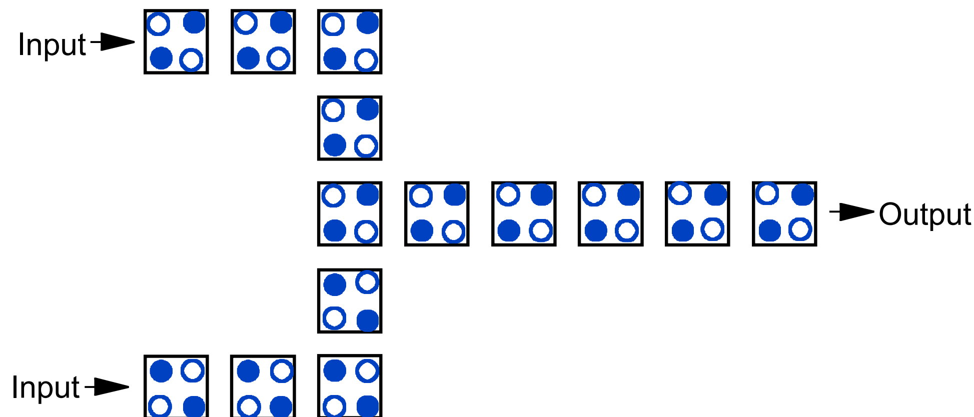


Two interacting cells



Electrostatic interaction between adjacent cells
Don't need wires to individual cells
Add energy to prevent "sticking"
Clocking…perhaps through substrate or overlayer

Logic



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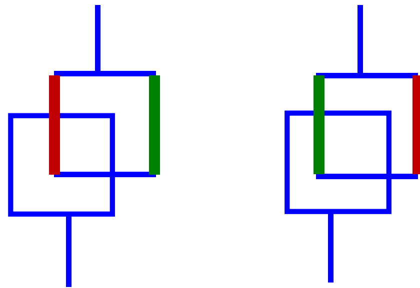
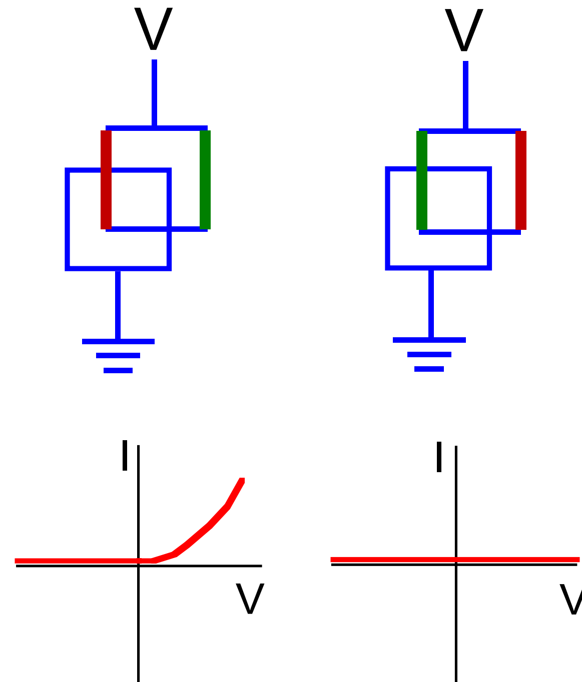
Molecular Electronics

Organic molecule with two states
of different electronic conductivity





Switch small group of molecules on nanowires
Eventually switch single molecule
Switching time?

C. P. Collier, *et al,* Science **289**,
1172 (18 August 2000)

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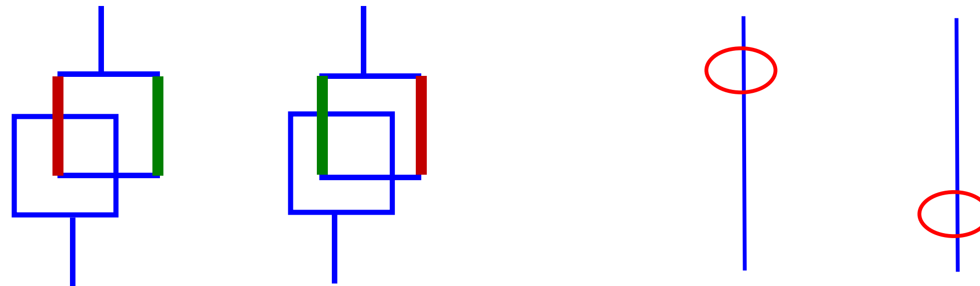
Molecular Electronics: Switching

Electronic reconfiguration of molecular structure
Charging of internal node within molecule
Possibly modify bonding of molecule to electrode



C P Collier, E W Wong, M Belohradsky, F M Raymo, J F Stoddart, P J Kuekes, R S Williams, and J R Heath, Science, vol. 285, p. 391, 16 July 1999

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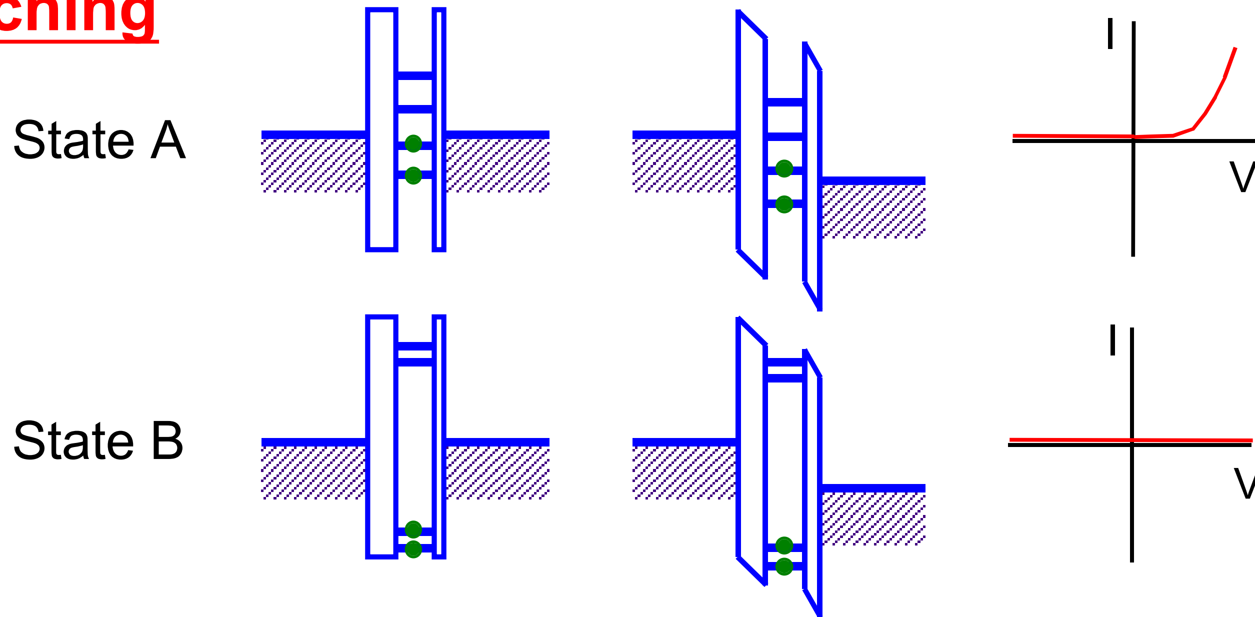
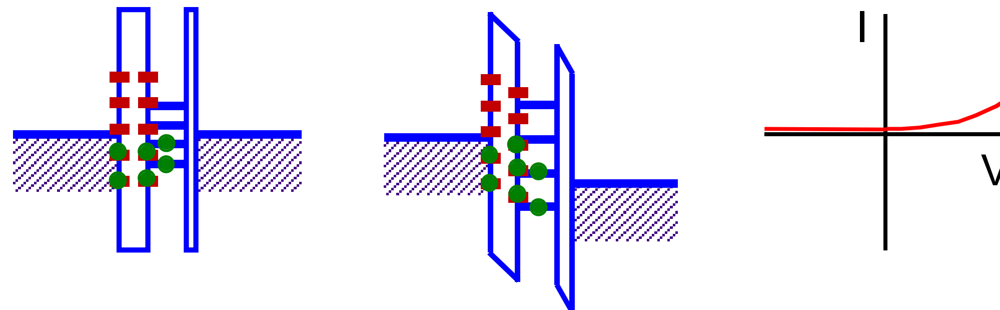
Molecular Electronics



Interfaces: Charge Trapping



Potential Devices

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Quantum cellular automata
Molecular electronics
Quantum computing
(Exciting, but speculative)

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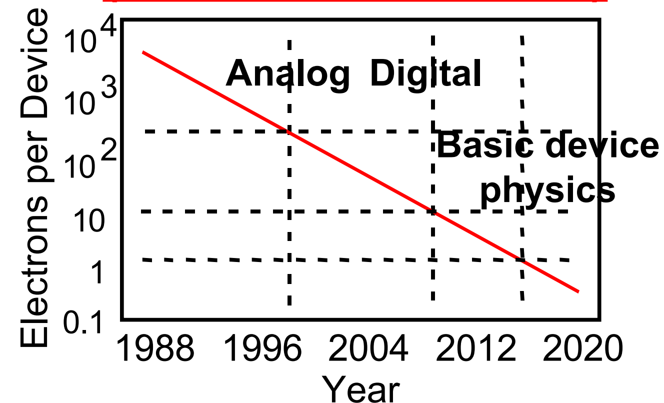

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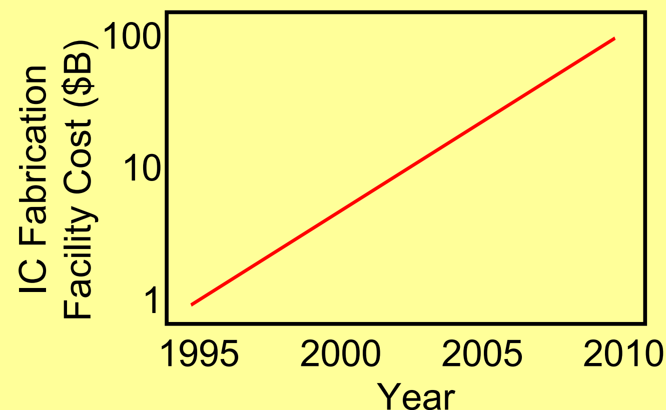


Advanced Lithography

Near-term

- Deep UV: I-line: 365 nm
- Excimer: 248, 193 nm
- Phase-shift masks
- Contrast enhancement

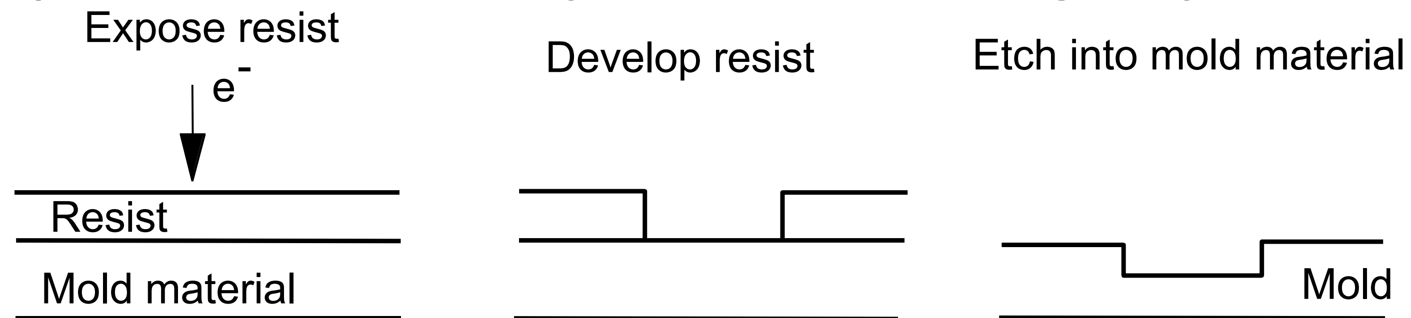
Future

- Electron beam: Serial
- Scanned probe: Serial
- x-ray: Parallel (masks?)
- Extreme ultraviolet 13 nm
  - Parallel
  - Reflective optics
- Nanoimprinting

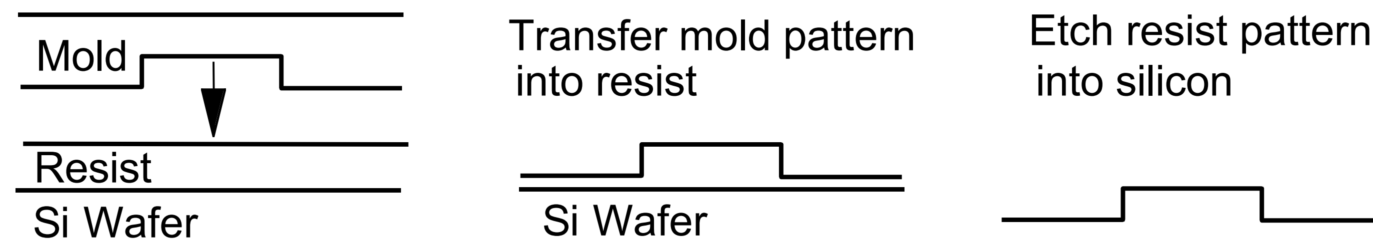
Nanoimprinting Technology

Fine features (10's nm)
Lower cost
Define many elements simultaneously

1) Make reusable mold by electron-beam lithography



2) Form nanoscale feature in substrate (Si)
All features formed <u>in parallel</u>



Steve Chou – Princeton University

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Self-Assembled Nanostructures
0D Islands and 1D Nanowires on Si

Conventional scaling will reach its limits

Use directed-assembly to extend Moore's law

- Determine critical dimensions by choice of materials and deposition kinetics ("self assembly"), not lithography
- Use lithography to position devices or arrays of devices ("directed assembly")

Use small-size effects to perform logic, storage, and computation

- Coulomb blockade
- Quantum confinement

Self (or Directed) Assembly

Methods of self- or directed- assembly

- Strain from lattice mismatch
- Catalytic wire growth on nanoparticle

Thermodynamically assembled structures

- Several percent defects
- Need defect-tolerant architecture

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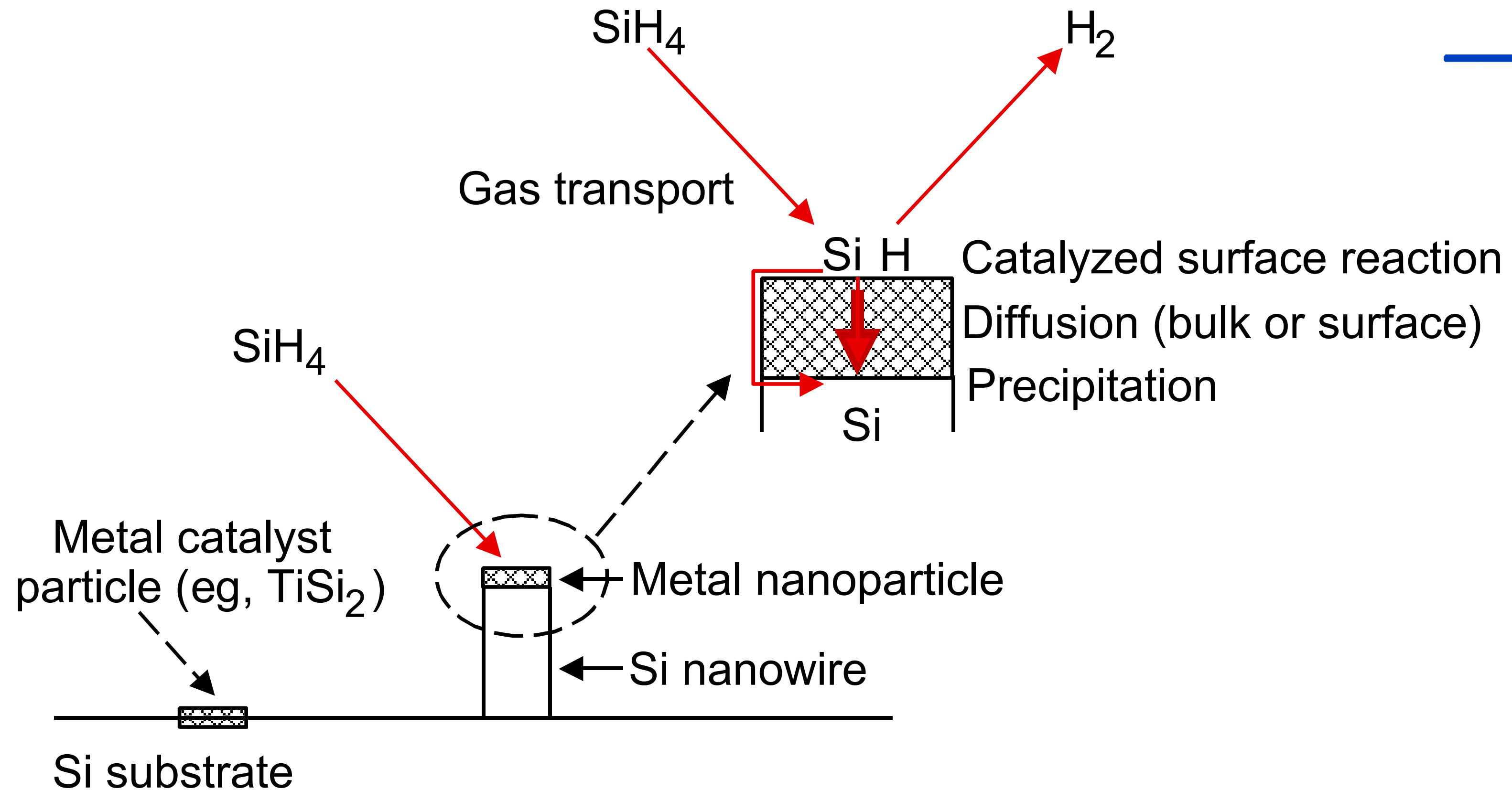
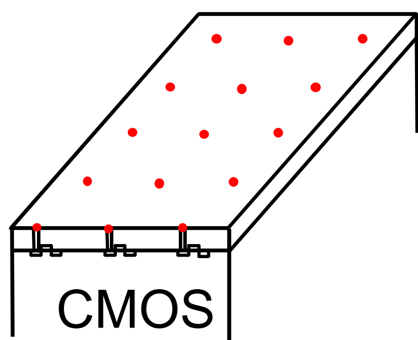
Metal Catalyzed Nanowire Growth

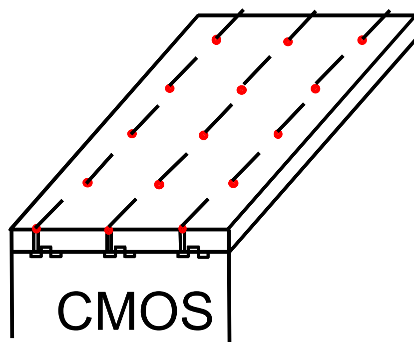


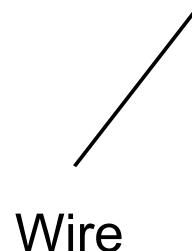
Integration of Nanowires with CMOS

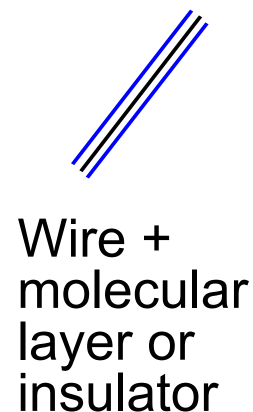
CMOS provides gain and interface circuitry
- Partially processed CMOS (700°C)
- Fully processed CMOS (400°C)

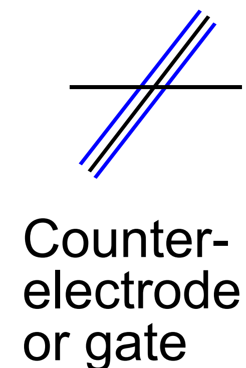
Perhaps as interconnections for molecular electronics
Perhaps place some modulating element within wire











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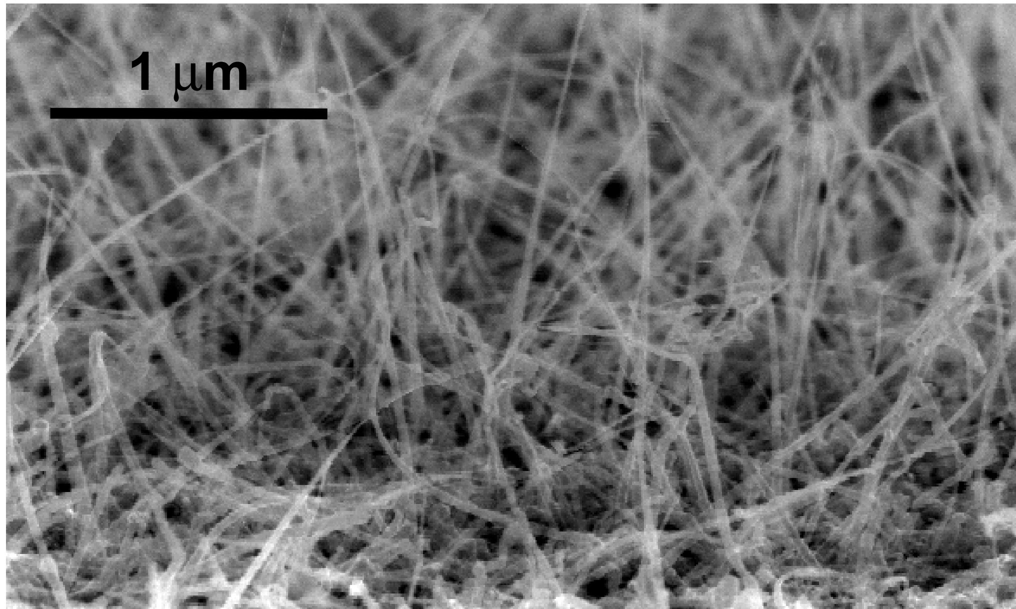
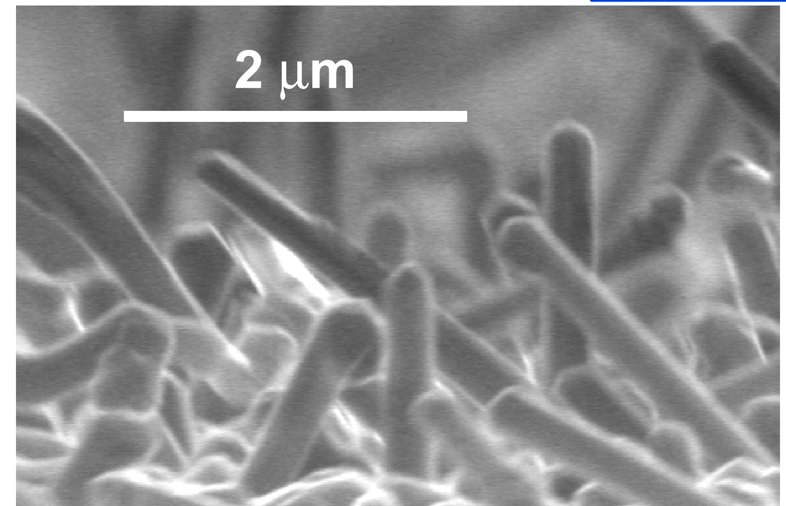
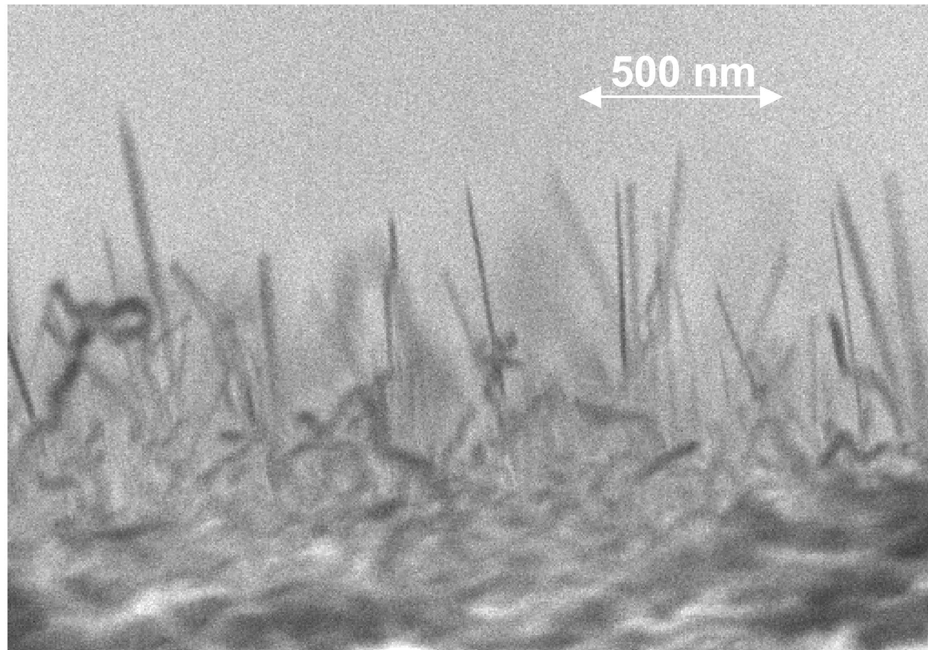
Metal-Catalyzed Si Nanowire Growth

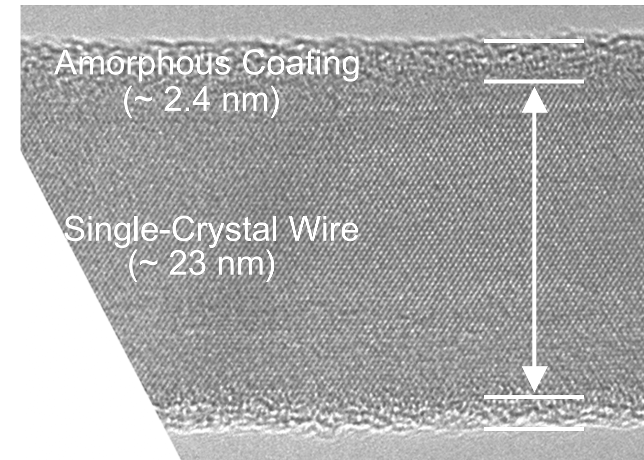




With Xuema Li and Tan Ha, Hewlett-Packard Labs

Dense Si Nanowires from $TiSi_x$ Islands





Micrographs by Thorsten Hesjedal,
Stanford University

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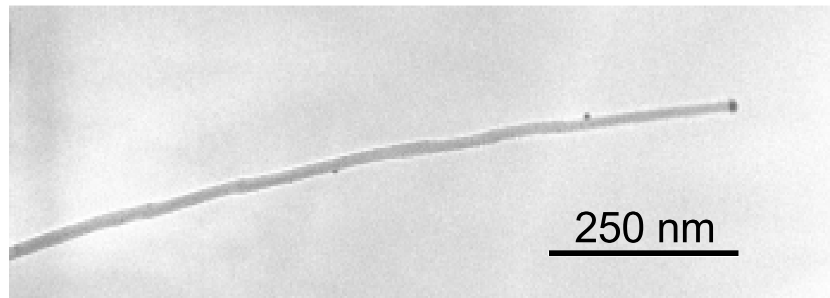
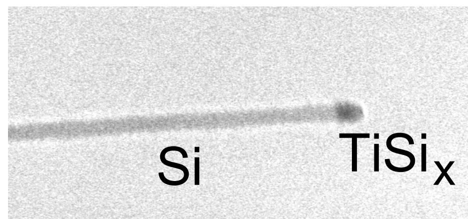
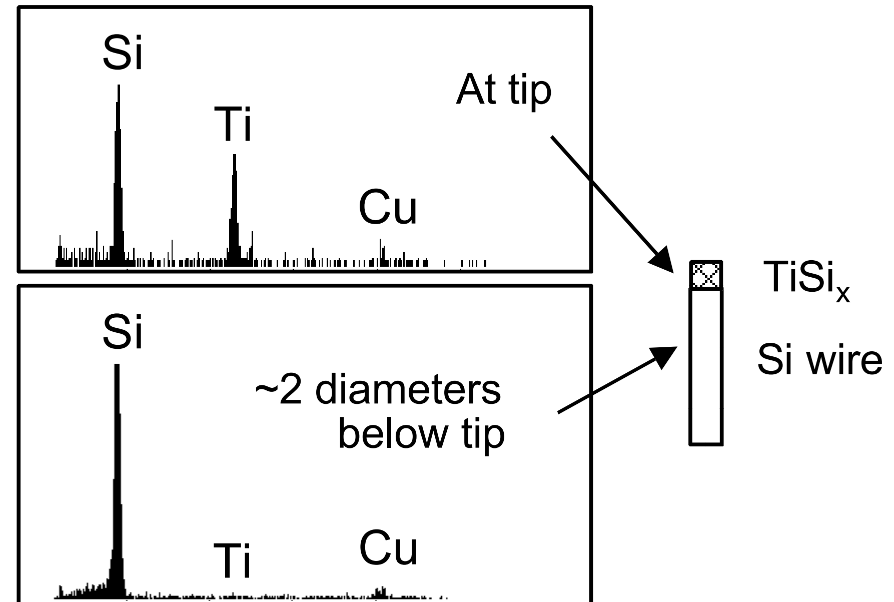
Ti-Nucleated Si Nanowire

Energy-Dispersive X-Ray Spectroscopy







TiSi$_x$

Si wire

Analysis by
Thorsten Hesjedal (Stanford University)
David Basile (Agilent Laboratories)

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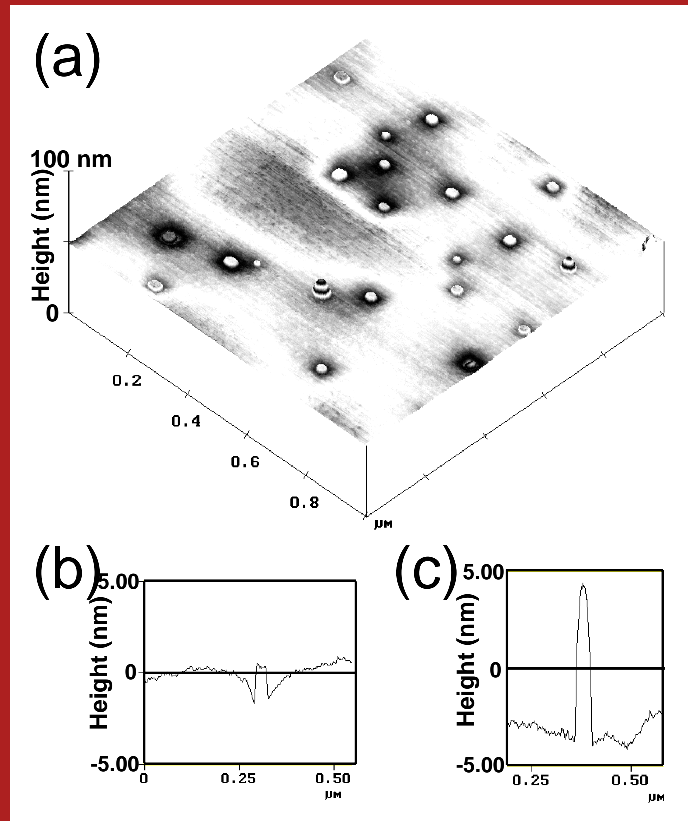
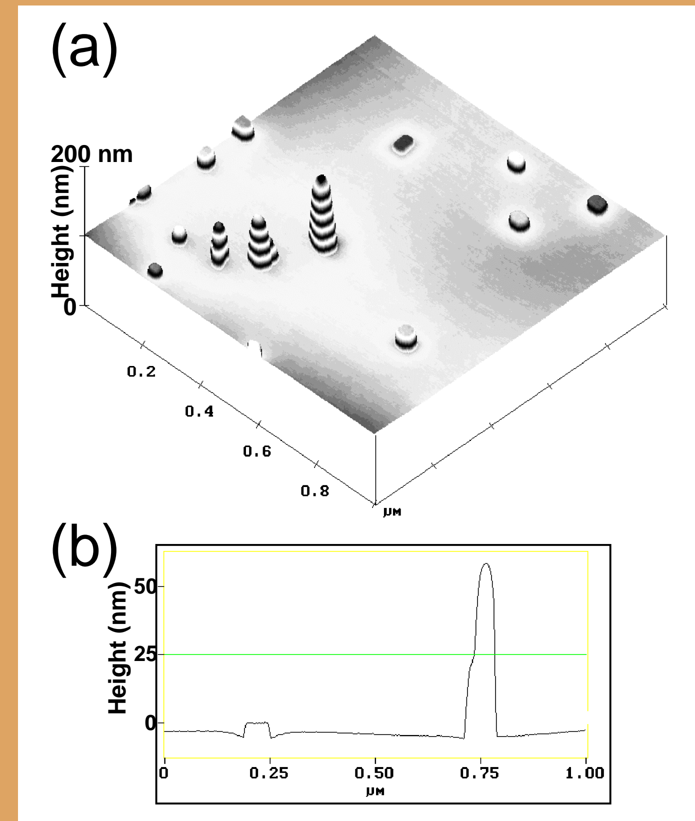
Surface Reaction Rate Limited Region of Growth

Initial Stage of Wire Growth



Subsequent Stage of Wire Growth

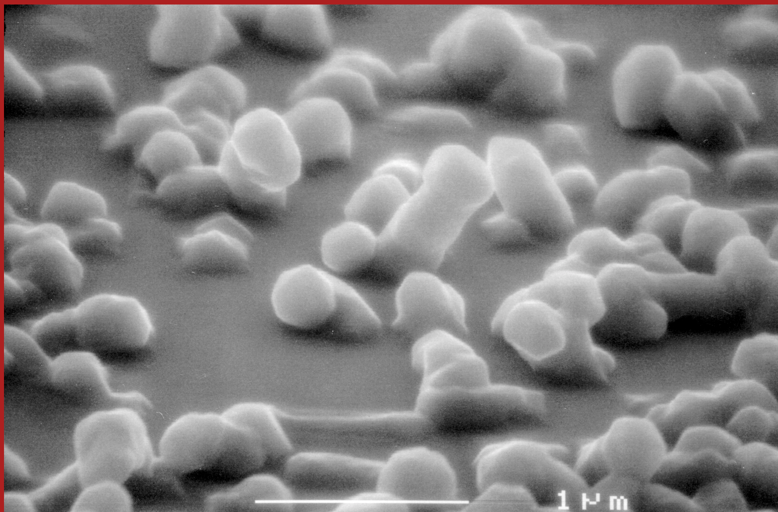


Higher temperature

Uncatalyzed growth rate significant

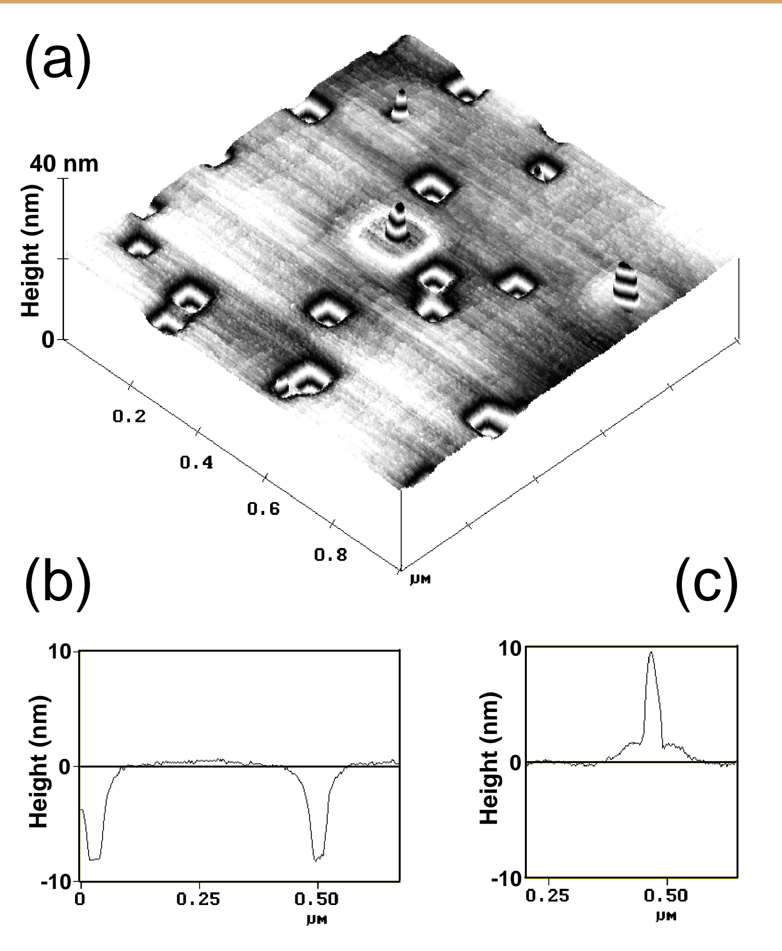
Surface Reaction Rate Limited Region

SiH_2Cl_2 at 920°C



Mass Transport Limited Region

SiH_4 at 920°C



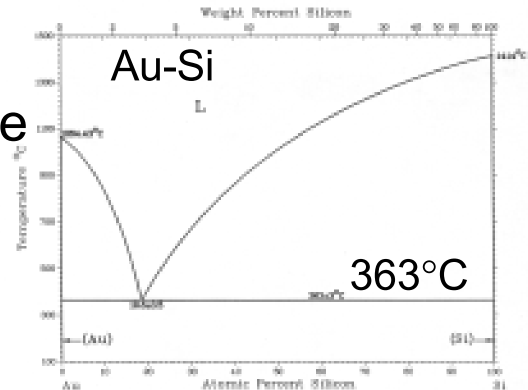
Catalytic Nuclei: Material

Desired characteristics:

Not a deep energy level in Si bandgap
Low solid solubility in Si
Liquid eutectic below deposition temperature (for VLS growth)

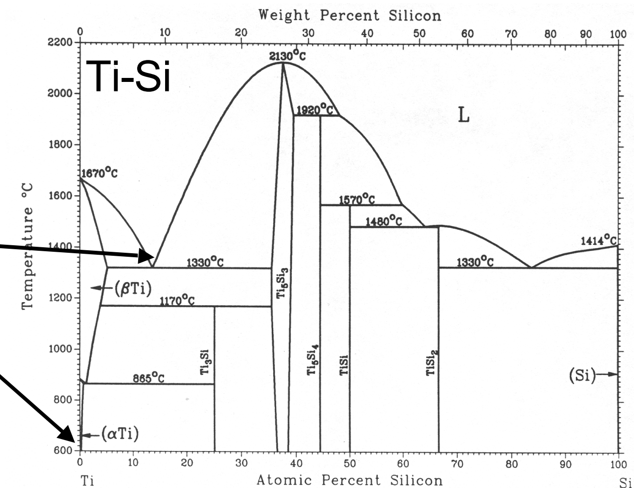
Au: Liquid eutectic: ~360°C for Si and Ge

E_t-E_i ~ 0: Mid-gap g-r center
N_{ss} = 10^{17} cm^{-3}
Need barrier layers if used with Si ICs



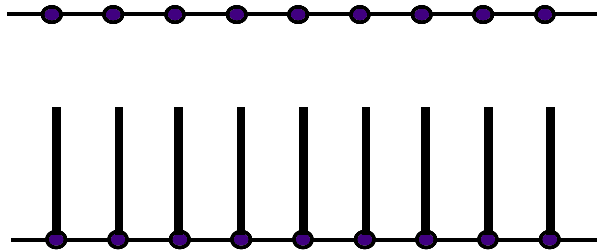
Ti: E_t-E_i ~ 0.34 eV

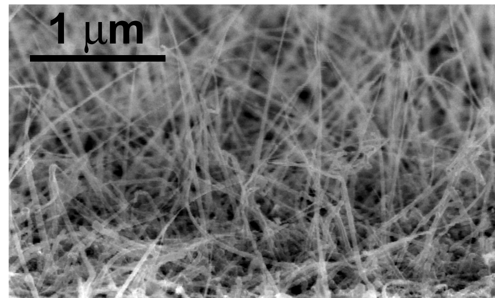
N_{ss} ~ 10^{12} cm^{-3}
Liquid eutectic: 1350°C
Deposition temperature: ~600°C
(probably not VLS growth)



Catalytic Nuclei: Form

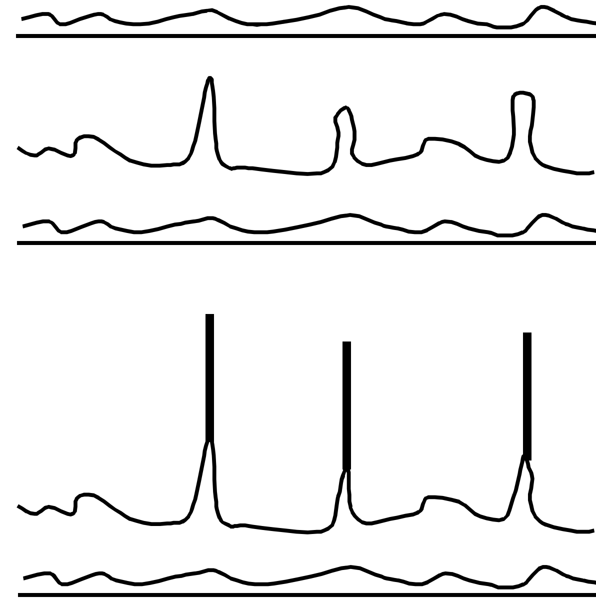
Isolated Nuclei





Si on evaporated Ti
Si grown at ~620°C

Layer

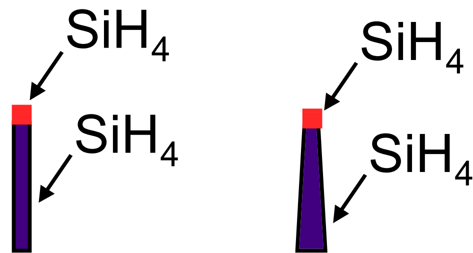


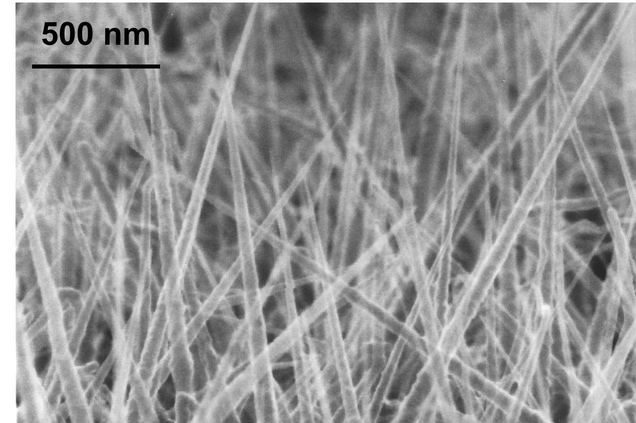
Si Nanowires on Ti

Wire diameter: 20-40 nm

Tapered at higher temperatures

- Uncatalyzed growth on sides of wires





Reduce taper by limiting uncatalyzed deposition rate

- Reduce temperature
- Less reactive Si source: *eg,* SiH_2Cl_2
- Add HCl

Nanowires formed in 600°C temperature range:
Compatible with partially processed CMOS

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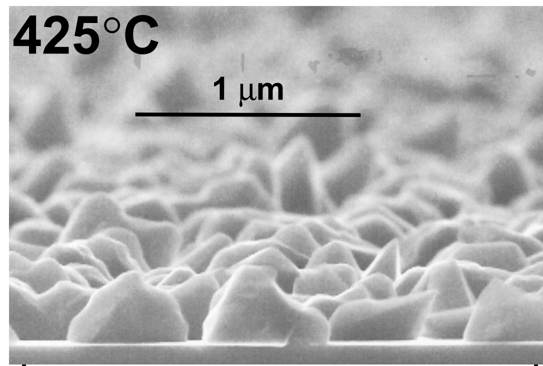
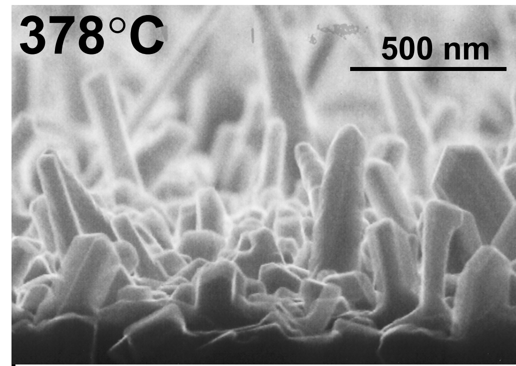
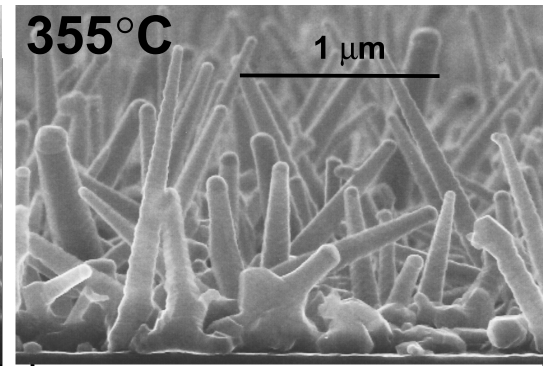
Lower Temperatures for CMOS Compatibility
Ge Nanowires on Au Nanoparticles

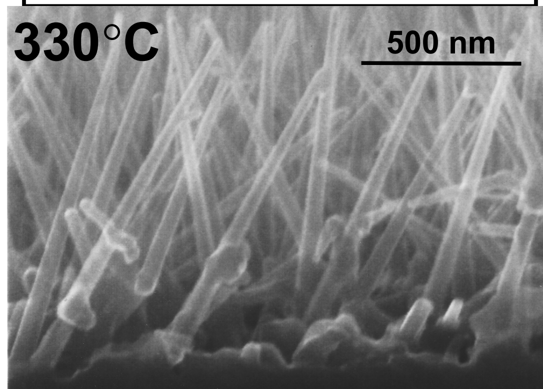
Temperature range for wire growth: ~315– 370°C

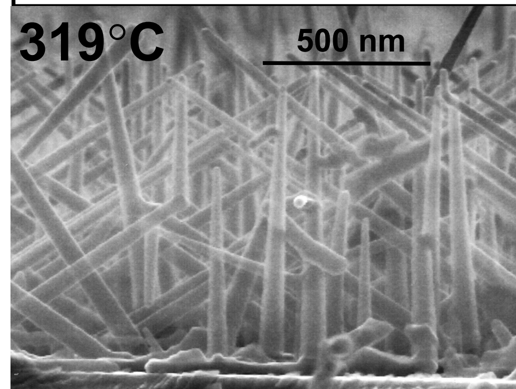
Wire diameter ~ 40 nm on ~20 nm Au nanoparticles

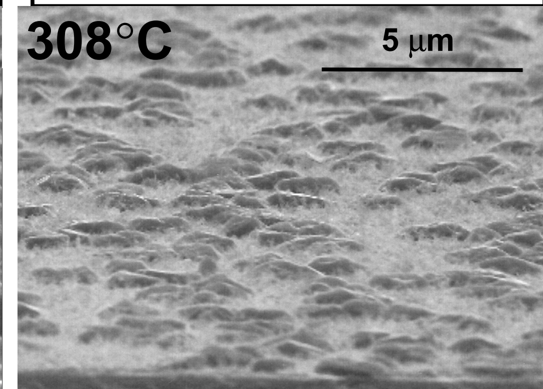












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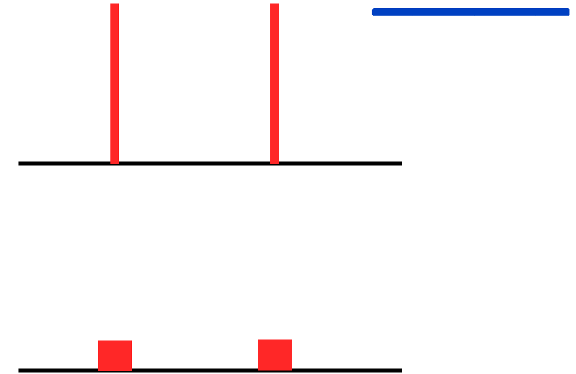
Stability of Si Nanowires

How stable are nanowires?
- Process integration easier if more stable

Instability caused by surface diffusion
- Native oxide expected to stabilize

Consider different ambients
- Inert vs. reducing
- Intermediate air-exposure
  - (In-situ *vs.* ex-situ annealing)



Inert ambient after air exposure: $N_{2:}$
- Stable to >950°C

Slightly reducing ambient after air exposure: 4%H_2/N_2
- Also stable to ~950°C

Strongly reducing ambient after air exposure: H_2

Strongly reducing ambient - no air exposure: H_2

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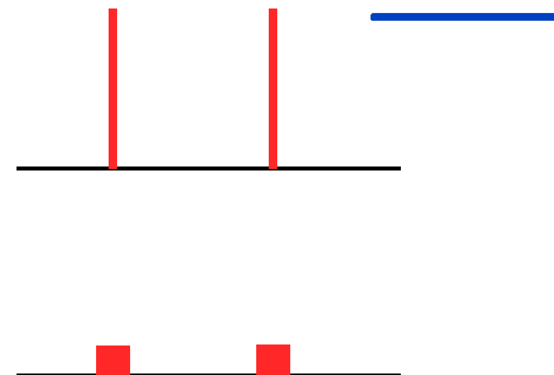

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Strongly reducing ambient - no air exposure: H_2

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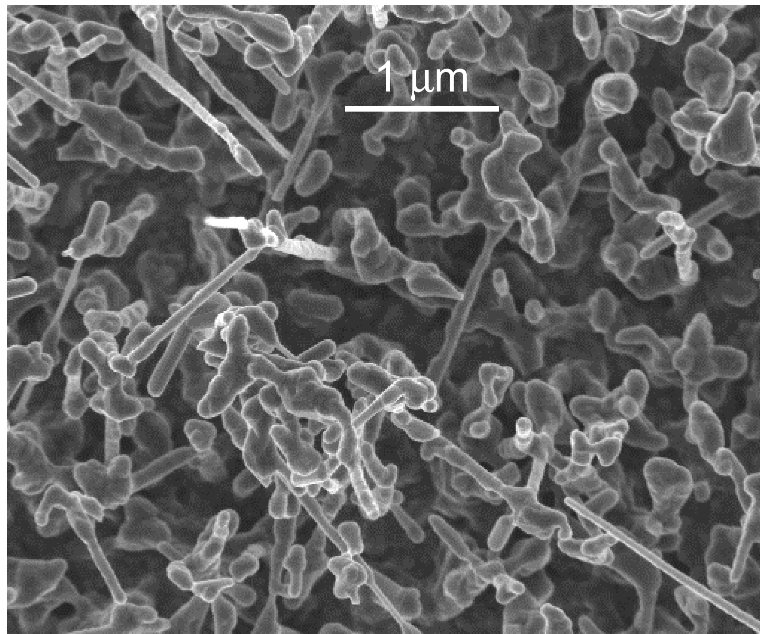
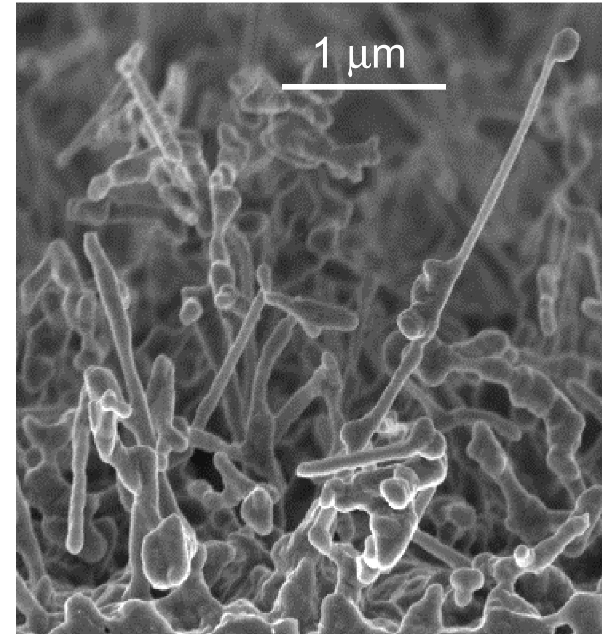
Stability (or lack of): 900°C in H_2
Si Nanowires on Ti

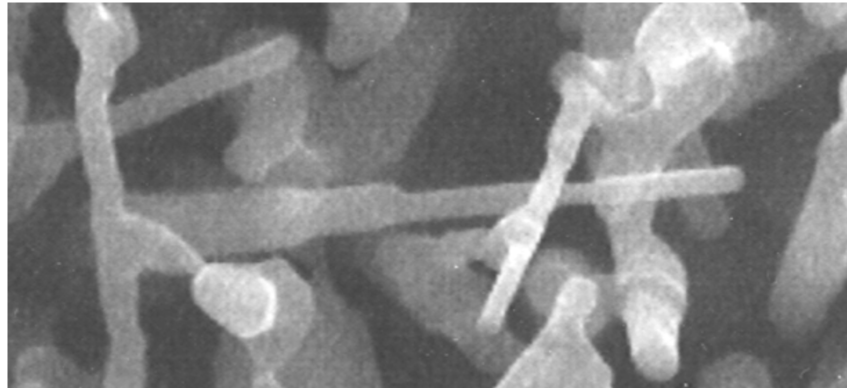


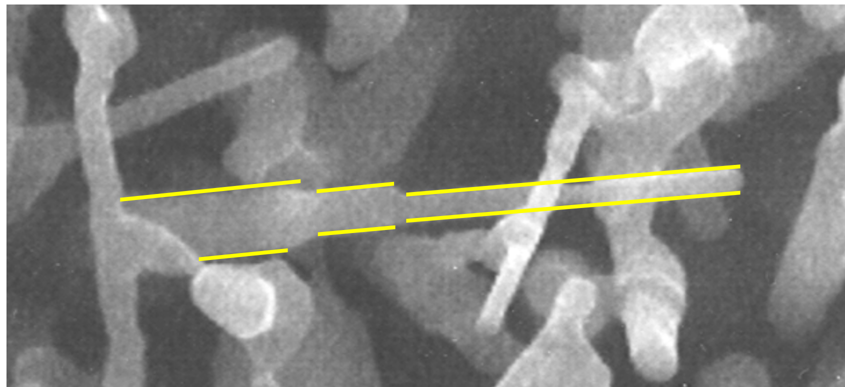
(Plan view)



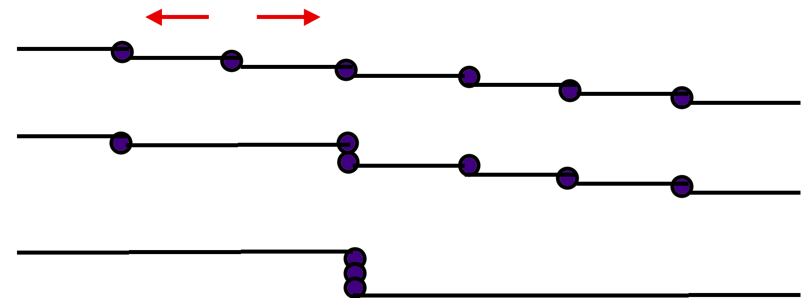
(Cross section)

Step Bunching on Tapered Nanowire

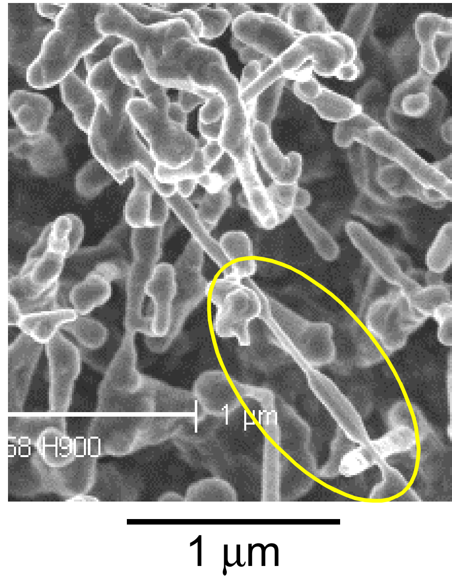




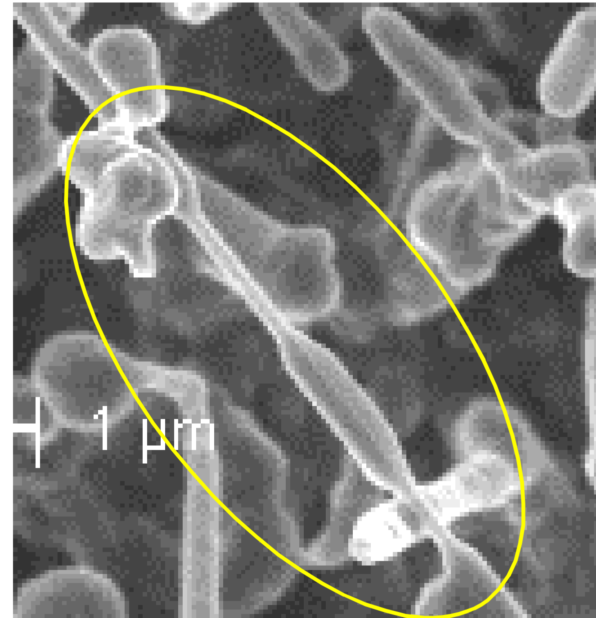
Rapid surface diffusion
Limited by step
detachment/attachment

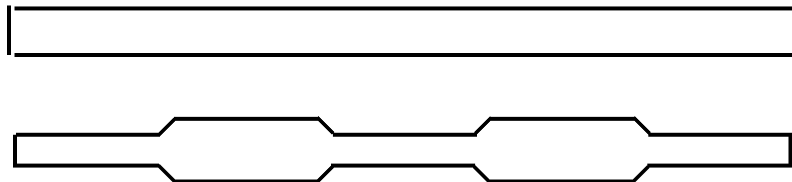


Instability along Uniform Nanowire



1 µm

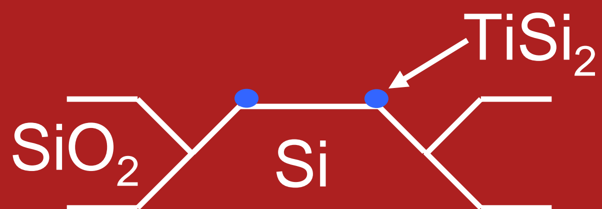


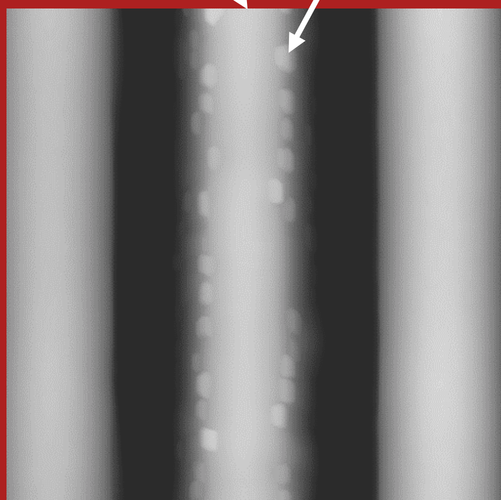


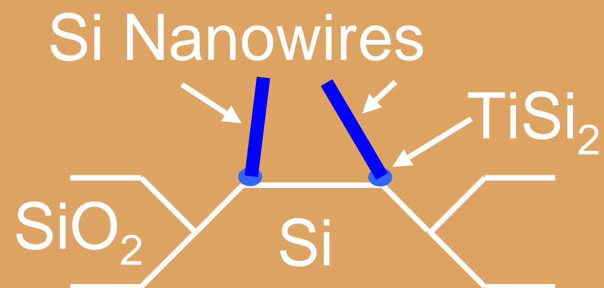
F. A. Nichols and W. W. Mullins, Trans. Met. Soc. AIME **233**, 1840 (1965).
Lord Rayleigh, Proc. London Math. Soc. **10**, 4 (1878).

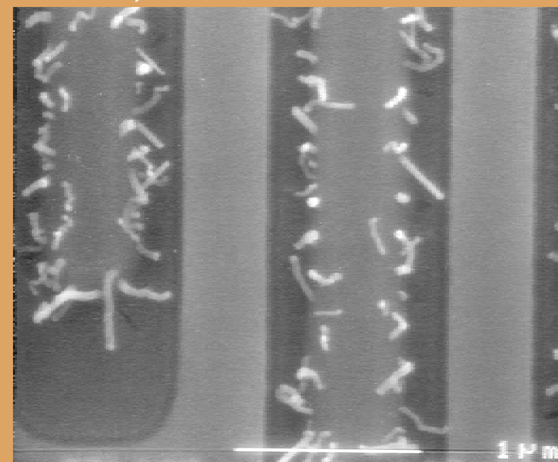
Forming Nanowires at Ordered Positions

Oxide-Patterned Si Substrate









Forming Self-Assembled Islands (Quantum Dots)

Deposit one material on another

Different lattice constants → strain

Large strain → islands

Small islands → quantum or Coulomb-blockade effects

Focus on Ge on Si

Why Ge on Si?

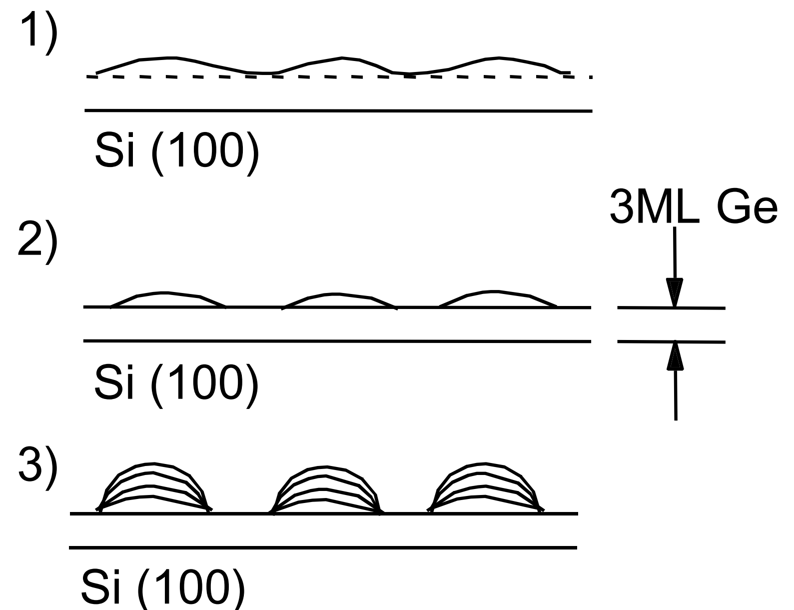
Compatible with Si IC technology

Deposition by

Chemical Vapor Deposition

(or Physical Vapor Deposition)

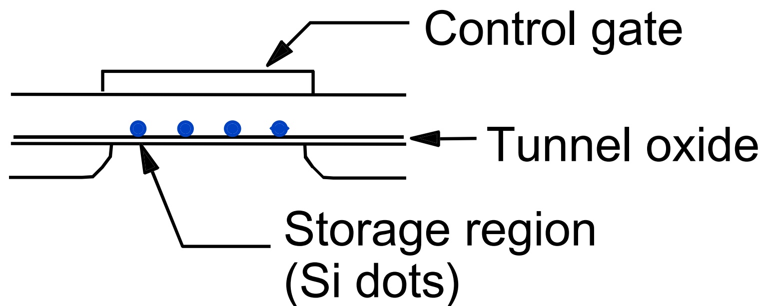
Energy and Kinetics Influence Island Formation



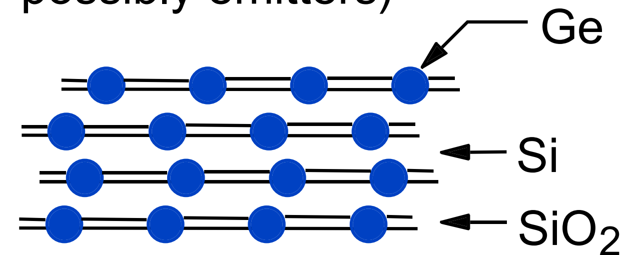
Possible Device Applications

Random Arrangement

Nonvolatile memory



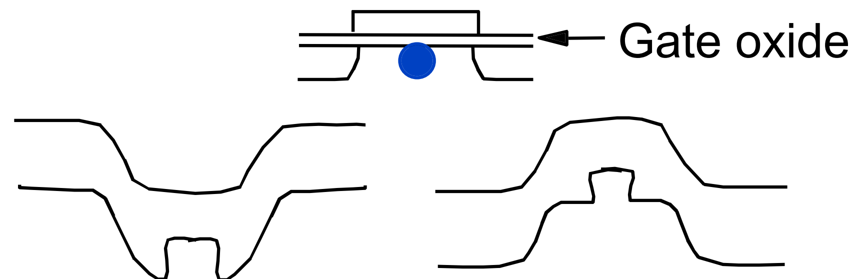
Long-wavelength photodetectors
(or possibly emitters)



Aligned

MOS for logic

Possible barrier to short-channel (substrate) effects



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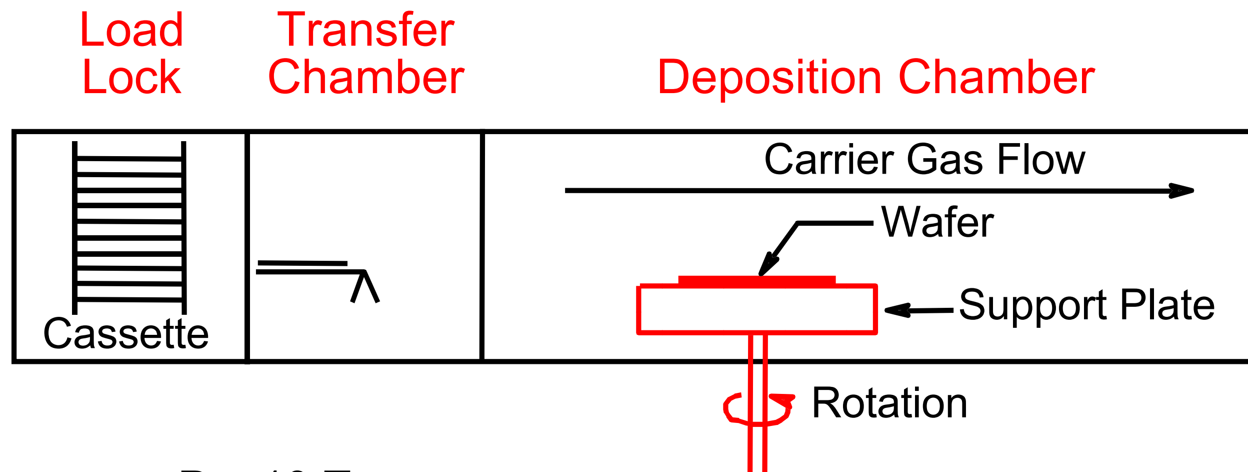
Chemical Vapor Deposition Reactor



P ~ 10 Torr

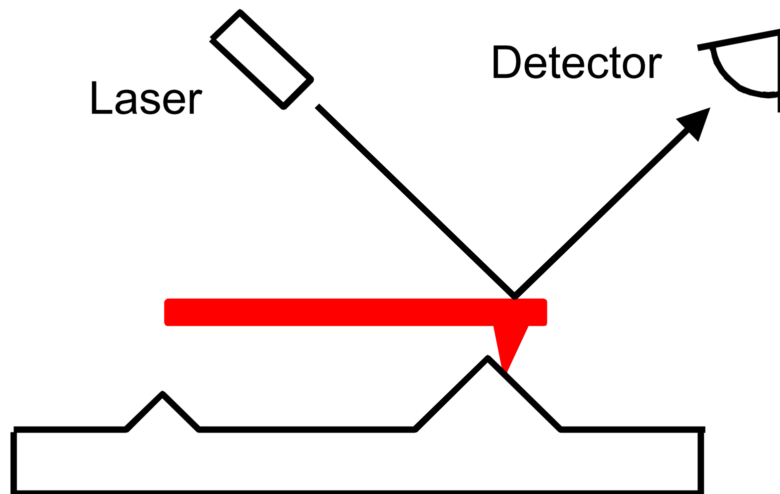
Carrier gas: H_2

Ge source gas: GeH_4

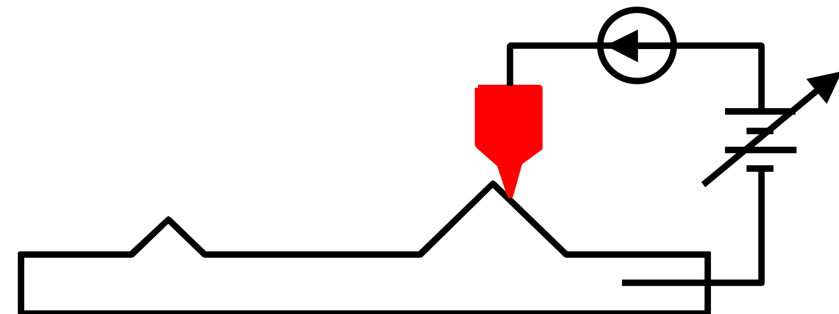
Layers deposited in two different single-wafer CVD reactors (and also by PVD)

Scanning-Probe Microscopy

Atomic-Force Microscope (AFM)



Scanning-Tunneling Microscope (STM)



CVD and *ex situ* characterization

PVD and *in situ* characterization

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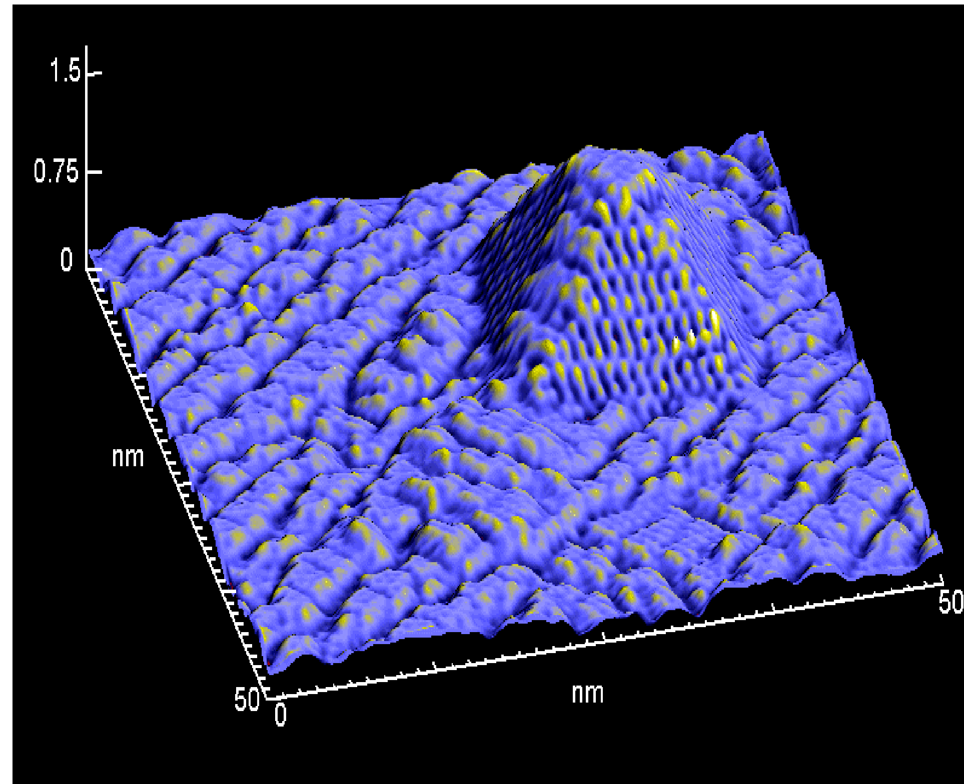
Very Small Ge Pyramid



Scanning Tunneling Micrograph by G. Medeiros-Ribeiro, HPL

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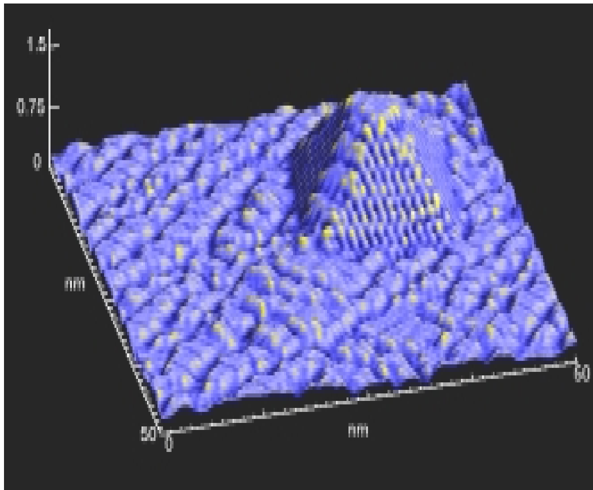
Self-Assembled Nanostructures

Strain from lattice mismatch_forms 3D structure

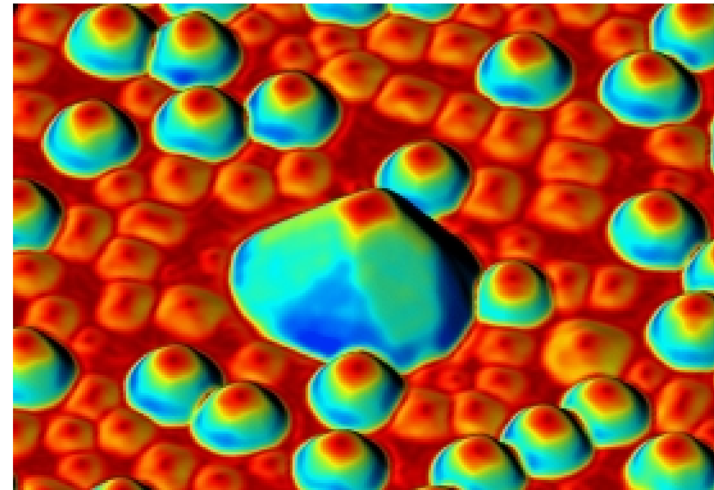
Small Ge "pyramid"
on Si(001)



Scanning-tunneling
micrograph

Gio Medeiros-Ribeiro, HPL

Array of Ge islands:
Pyramids, domes, superdomes



Atomic-force
micrograph

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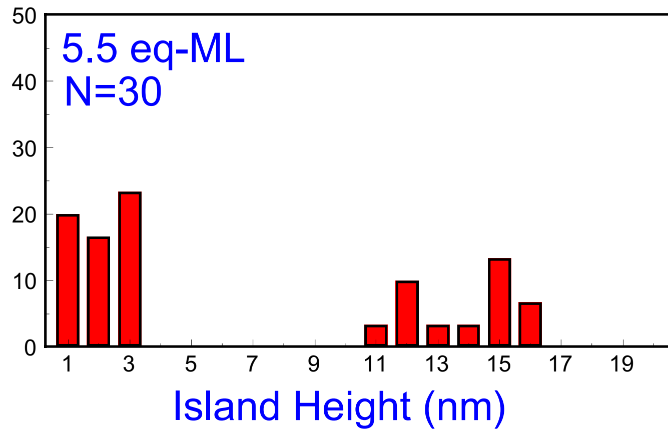
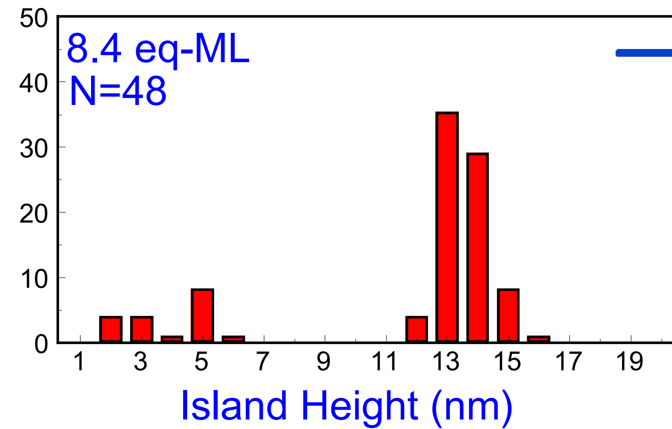
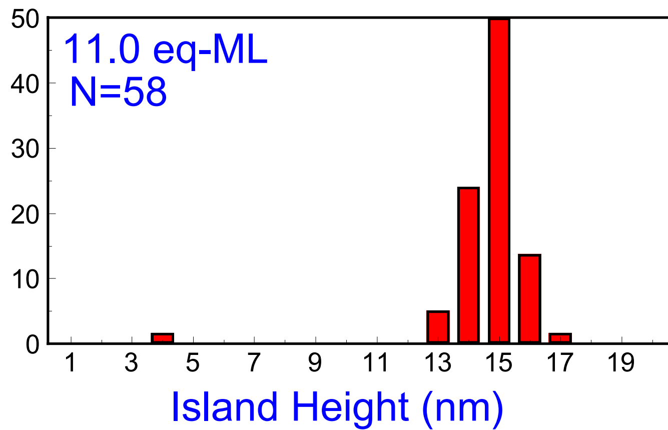
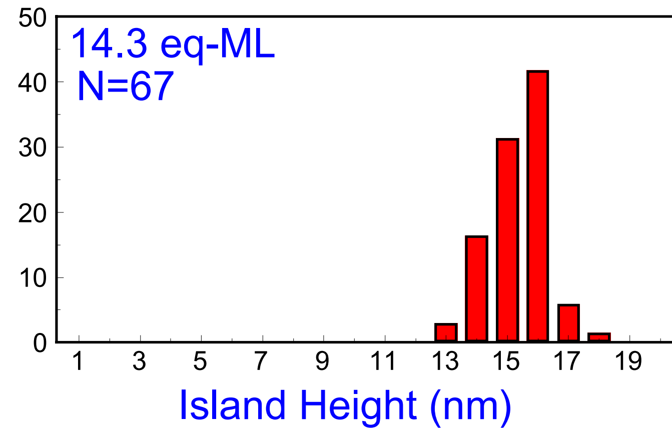
Distribution of Island Heights









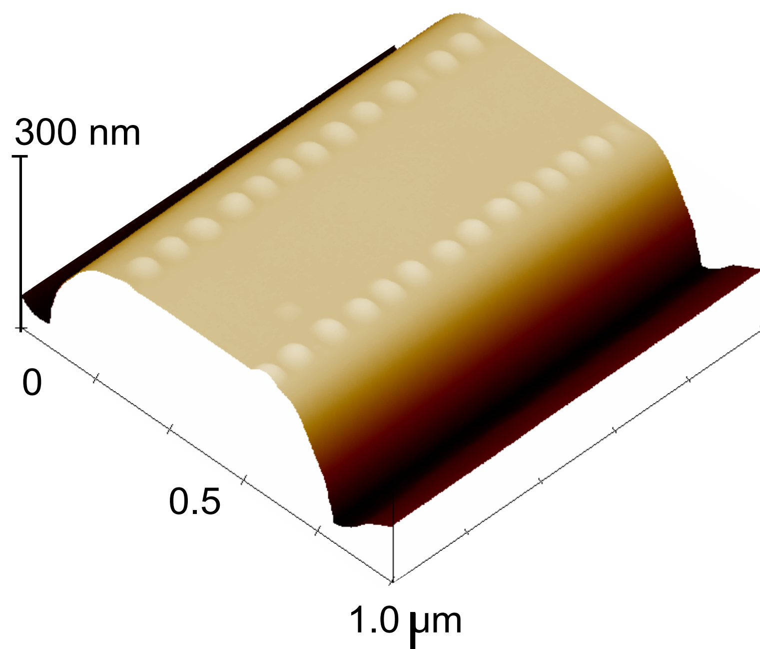
Percent of Islands

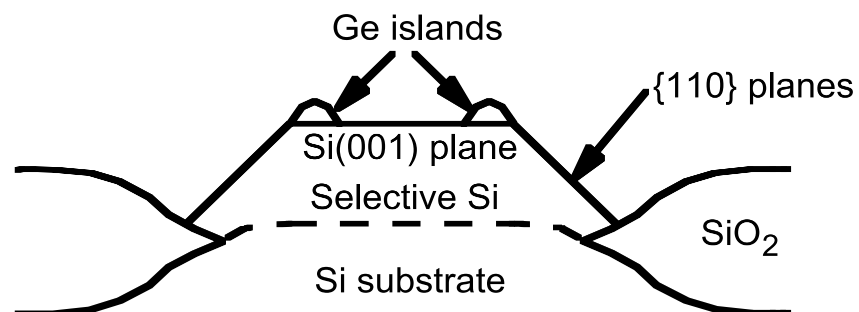
Percent of Islands

Percent of Islands

Percent of Islands

Positioning Islands: Self-Assembled Ge Islands on Patterned Si substrate



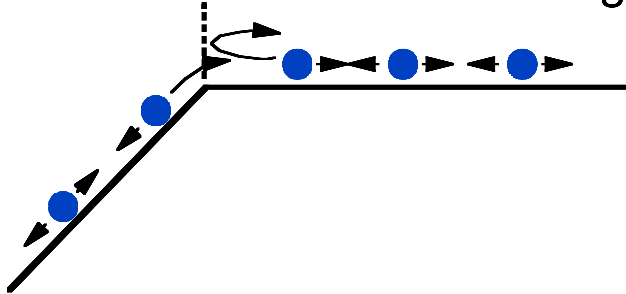


T.I. Kamins and R. Stanley Williams, Appl. Phys. Lett. **71**, 1201 (1997)

What Causes Alignment?

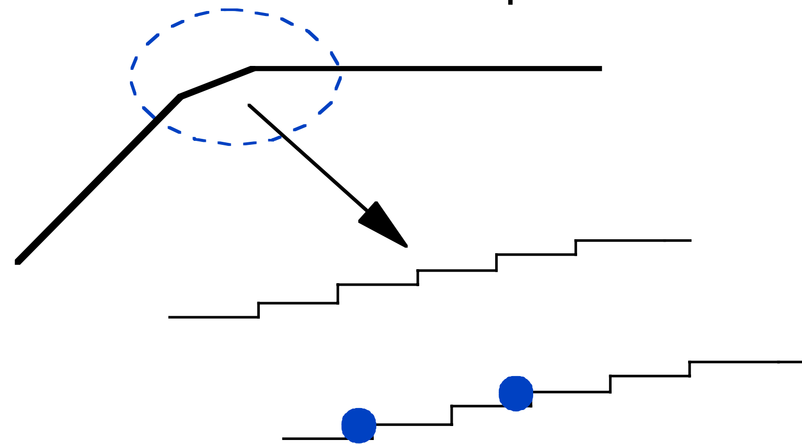
Surface Diffusion?

Anisotropic diffusion causes
Ge accumulation near edge



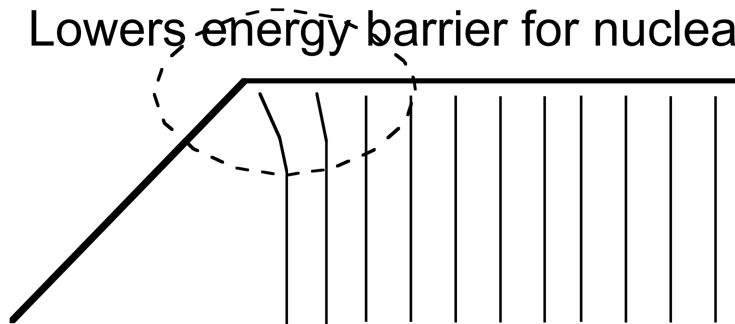
Steps near Edge?

Small facet at corner provides steps
Ge nucleates on steps



Strain?

Ge stretches Si lattice near edges
Relieves stress
Lowers energy barrier for nucleation



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Anisotropic Stress

Ge on Si:

Lattice mismatch same in x and y directions
$\Rightarrow$ equi-axed islands

Different lattice mismatch in different directions
$\Rightarrow$ anisotropic islands (ie, “wires”)

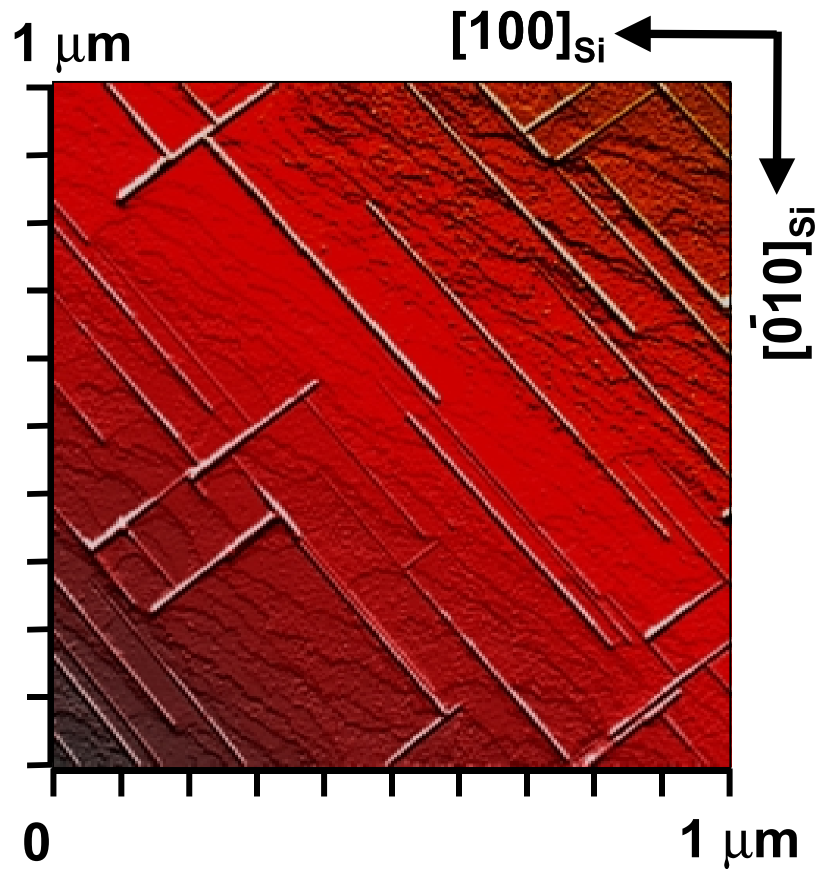
Anisotropic lattice mismatch:

ErSi2 [0001] || Si<110>: +6.5%
ErSi2 [11$\bar{2}$0] || Si<110>: -1.3%

Constraint on growth in one direction
Elongated (wire) growth in perpendicular direction

Y. Chen, D. A. A. Ohlberg, G. Medeiros-Ribero,
Y. A. Chang, and R. Stanley Williams,
Applied Physics Letters **76**, 4004 (26 June 2000)

$ErSi_2$ on Si



Yong Chen and Doug Ohlberg, HPL

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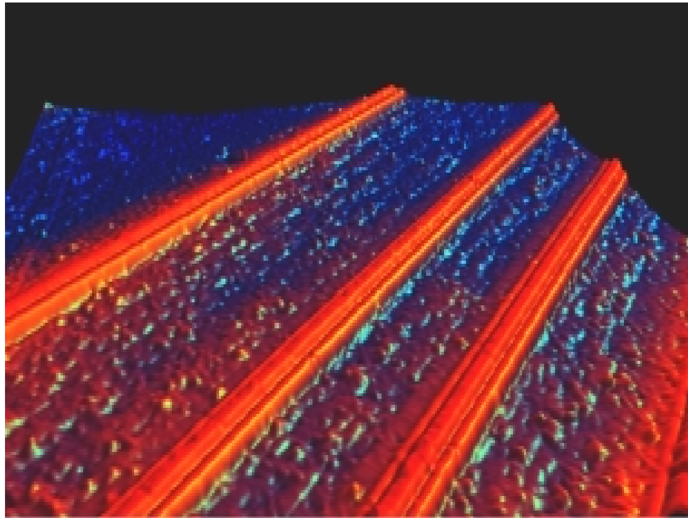
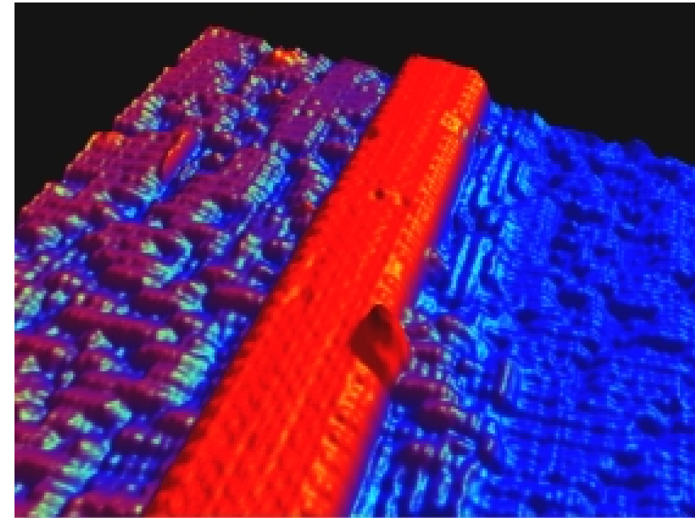
Self-Assembled Nanostructures

Anisotropic lattice strain forms 1D structure

$ErSi_2$ "wires" on Si(001)





Scanning tunneling micrographs

Yong Chen and Doug Ohlberg, HPL

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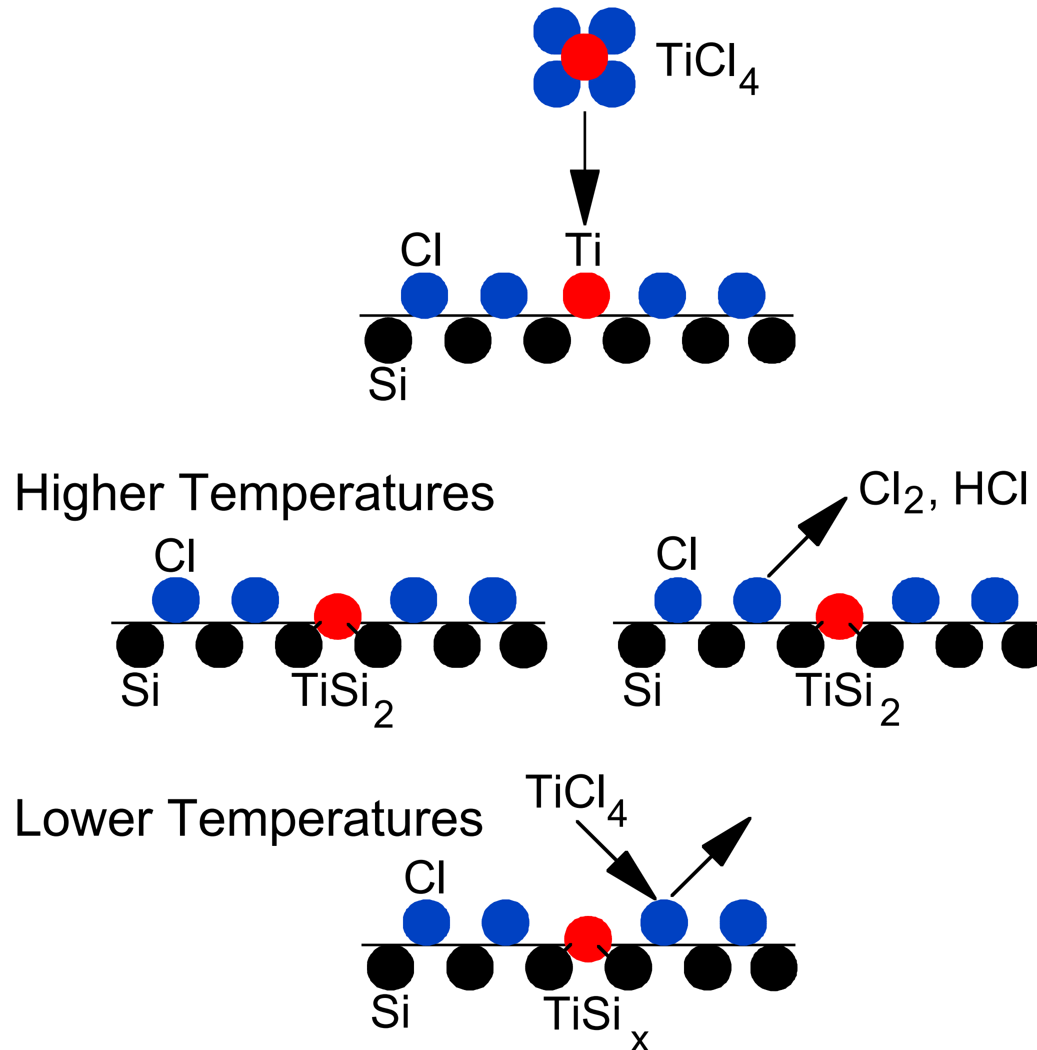
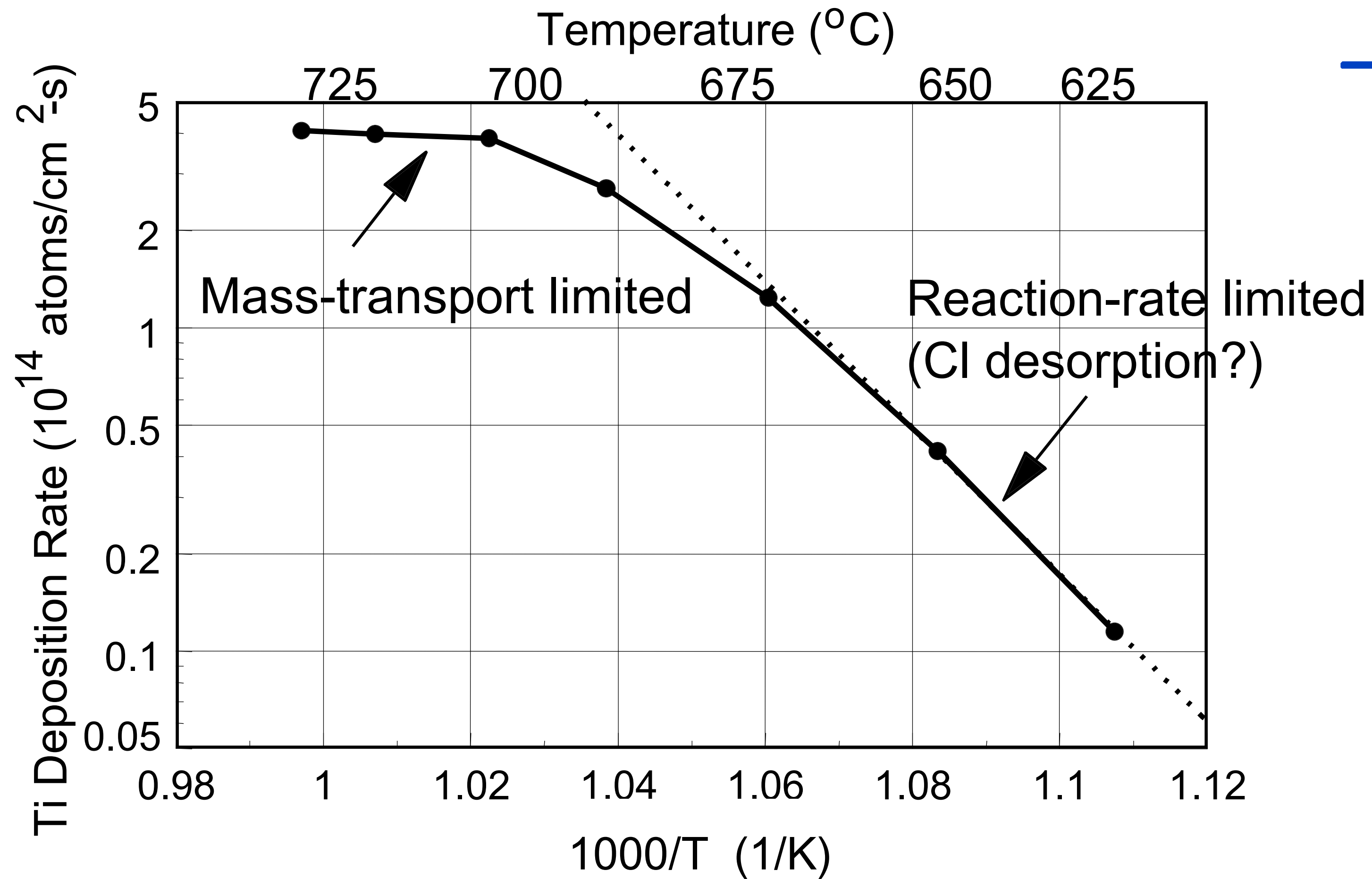
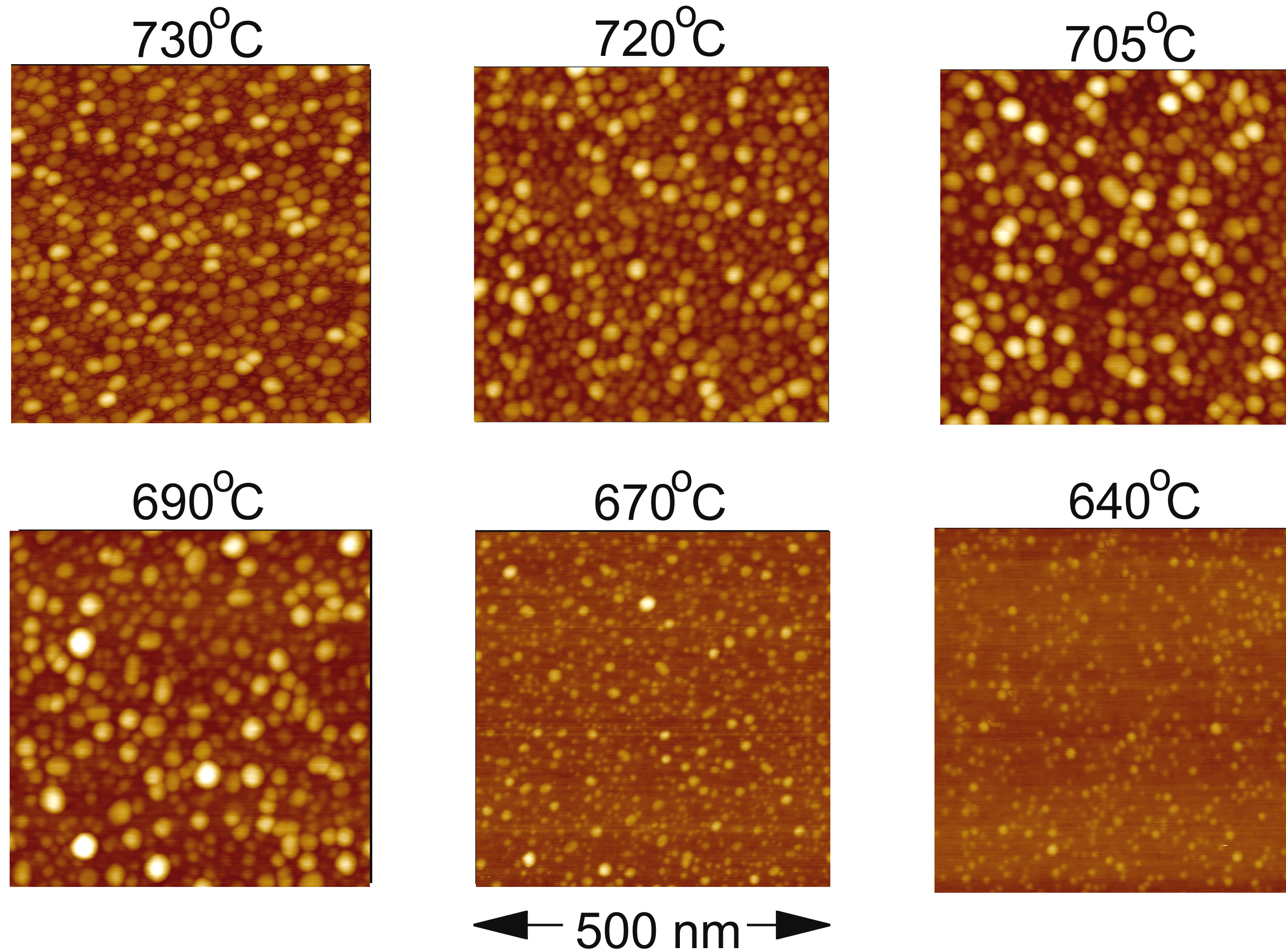
Deposition of Ti from $TiCl_4$



Deposition Rate of Ti from $TiCl_4$



Deposition of Ti from $TiCl_4$



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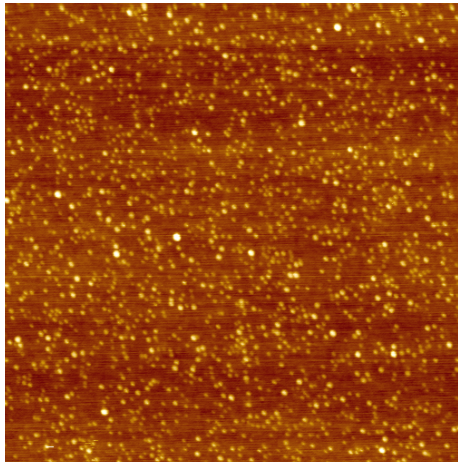
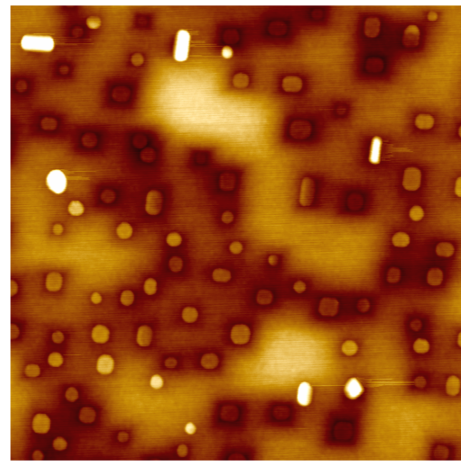
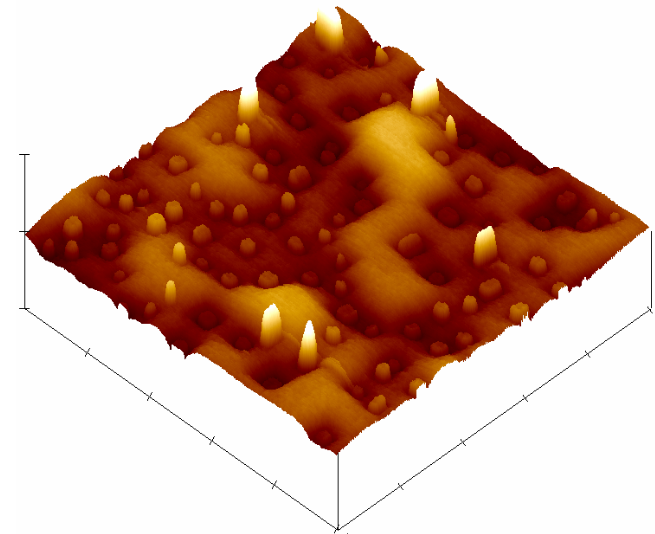
Annealing CVD Ti Islands

After Deposition at 640°C

Annealed at 920°C

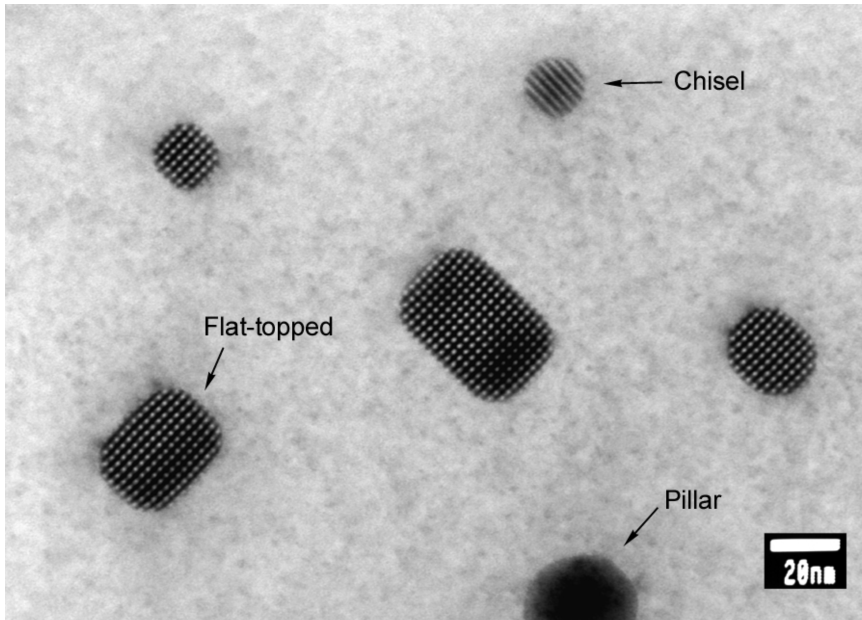




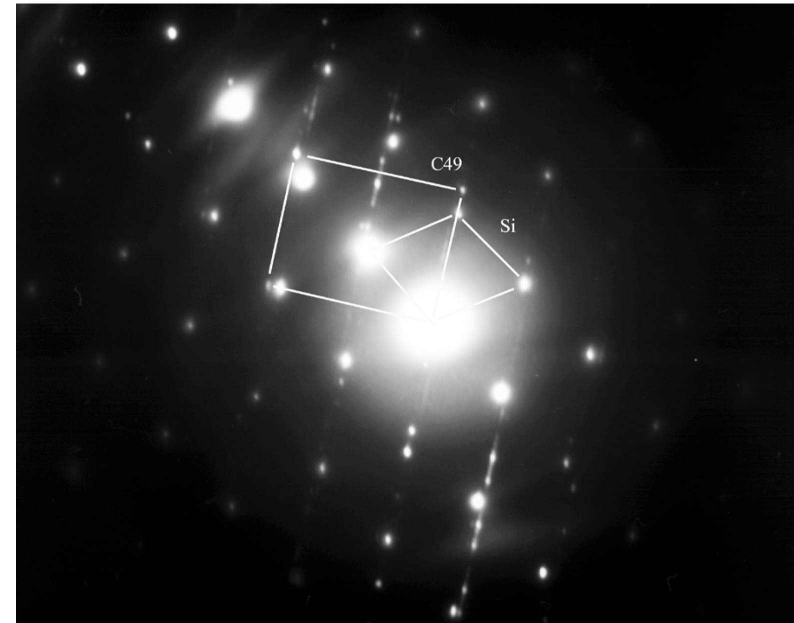


1.0 μm

Transmission Electron Microscopy of Annealed $TiSi_2$ Islands



Plan View



Cross Section

Transmission electron microscopy by
David Basile and Margaret Wong of
Agilent Laboratories

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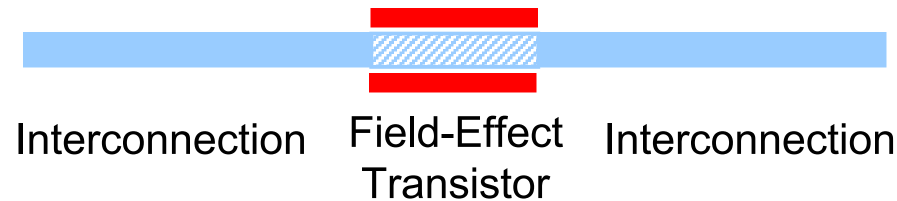
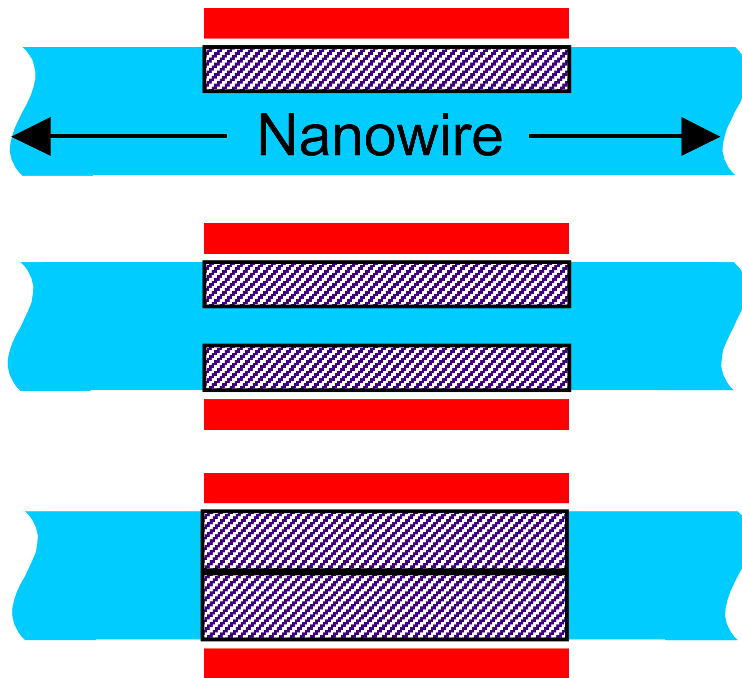
Nanowire: Integrated Device and Interconnection



Trade-off: Series resistance vs. Transistor Characteristics

Two cases: Uniform doping
Selective doping

Nanowire: Uniform Doping



Normally ON transistor

$D < 2\,x_{dmax}$

Doping low enough so can deplete
entire wire diameter

Limits conductance of interconnect

- Voltage drop along wire
- Time to charge next gate

Sensitive to size and doping

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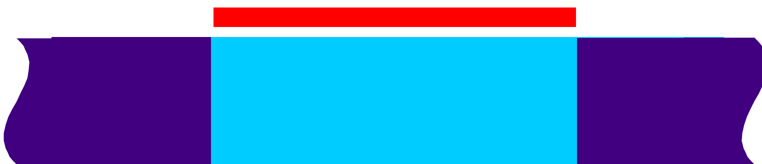
Selective Doping

Interconnection   Device   Interconnection

Bulk (e.g., implant)
Surface induced

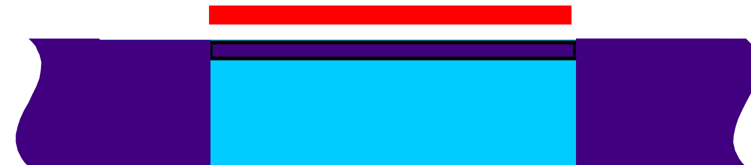
Heavy doping (~sol.sol.)

Light doping (~ intrinsic or opposite type)



Normally OFF transistor

$D \nless 2\, x_{dmax}$



Induce channel

Intrinsic: Not sensitive to dopant fluctuations

Sensitive to wire diameter

Addressing Moore's Second Law
Crossbar Array

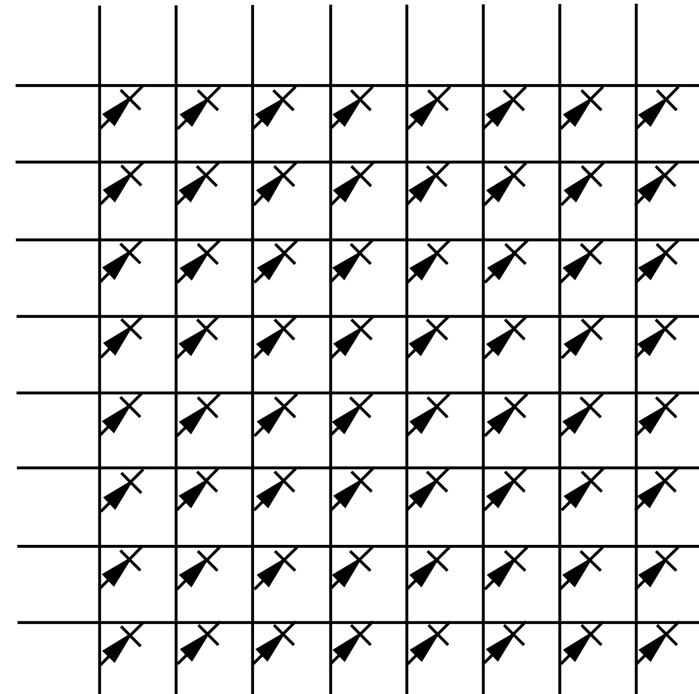
Dense
- Device at intersection of two wires

Structurally simple
- Need well-defined threshold to
  - avoid switching when "half selected"

Repetitive
- Allows reconfiguration
- Defect tolerance

Wires (perhaps)
- Si nanowires or C nanotubes

Gain
- In devices
- In "wires"
- In underlying CMOS



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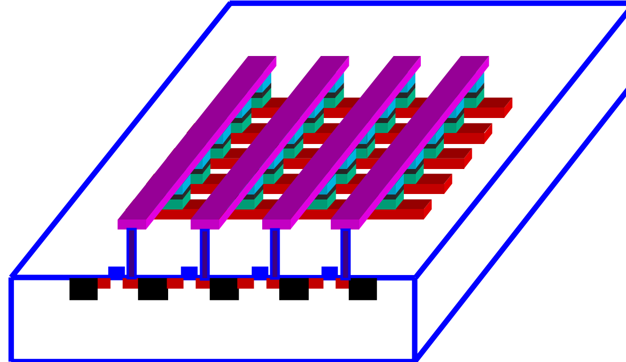
Cross-Bar Memory Array above Logic



Bit at crossing of wires
- Nonvolatile (unlike DRAM)

Can be built above CMOS
- Physically place elements closer together
  - Minimize delay between logic and storage

Multiple layers possible (unlike Flash memory)
- “3D IC”
- Increase density
  - Effective use of expensive CMOS area

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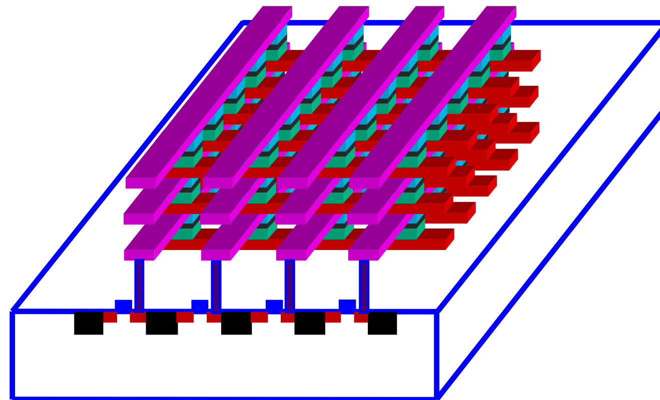
Three-Dimensional Electronics



Increase density
Physically place elements close together
Shorter wires
    Wires and vias must not limit area
        available for devices

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Defect Tolerance

Self-assembled, self-ordered system will not be perfect
- Several percent defects

How to live with less-than-perfect parts in a system?
- Structurally simple architecture (*eg,* crossbar array)
  - Self-assembled parallel straight wires
- Map defects
- Configure around defects
- (Can also be applied to conventional fabrication to reduce costs)

Teramac (HP Labs Project)

Demonstration of configurable computer made with “known bad” parts
(location of defects initially unknown)
Implemented with partially defective FPGAs
Mainly wires, crossbar switches, look-up tables
Normal computer: Design (configure), build, test
Teramac: Build, test (to locate defects), configure around defects

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W.B. Culbertson, R. Amerson, R.J. Carter, P. Kuekes, and G. Snider, Proc. 1997 IEEE Symp. On FPGAs for Custom Computing Machines
J.R. Heath, P.J. Kuekes, G.S. Snider, and R.Stanley Williams, Science, vol. 280, pp. 1716-1720 (12 June 1998)

Summary

Limits of scaling

Alternative devices

- Single-electron transistor
- Quantum cellular automata
- Molecular electronics
- Quantum computing

Self-assembled nanostructures

- Forming small structures
  - Putting them where we want them
- Metal-catalyzed wire growth
  - Ti-catalyzed Si nanowire growth
  - Stability of wires
- Strain from lattice mismatch
  - Zero-dimensional islands: Ge, Ti
  - One-dimensional wires: $ErSi_2$
- Patterned substrate to position features
- Speculation about nanowire transistor

Defect-tolerant architecture