Nanowires: Speculation on Integrating Devices and Interconnections

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Stanford University
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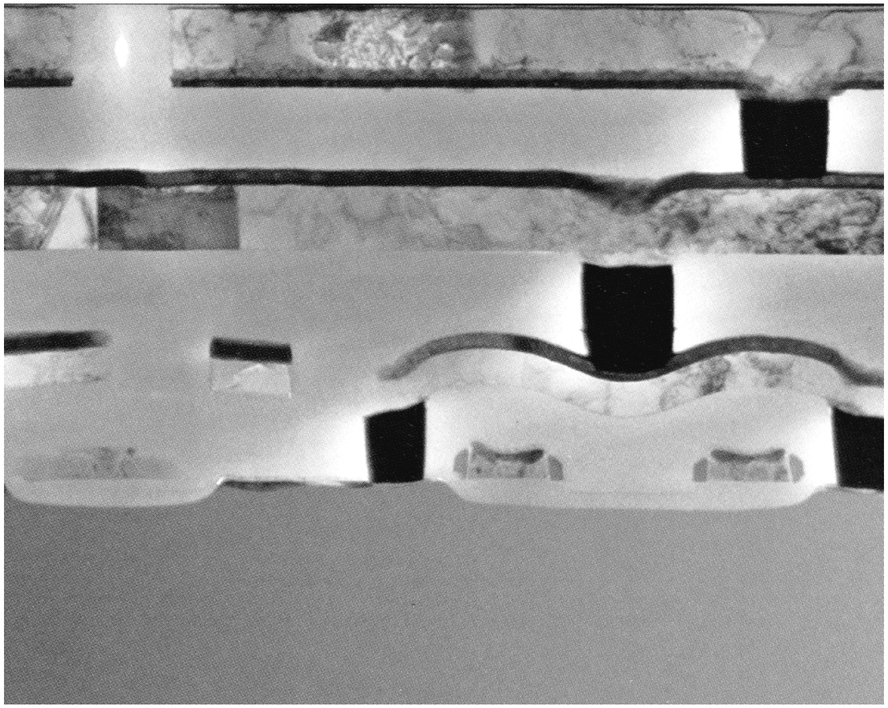
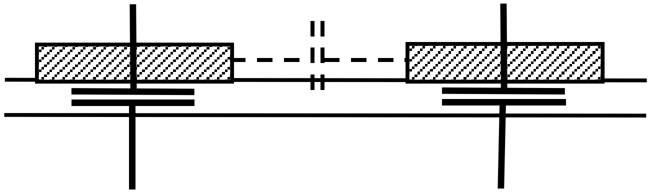
Multilevel Interconnection System

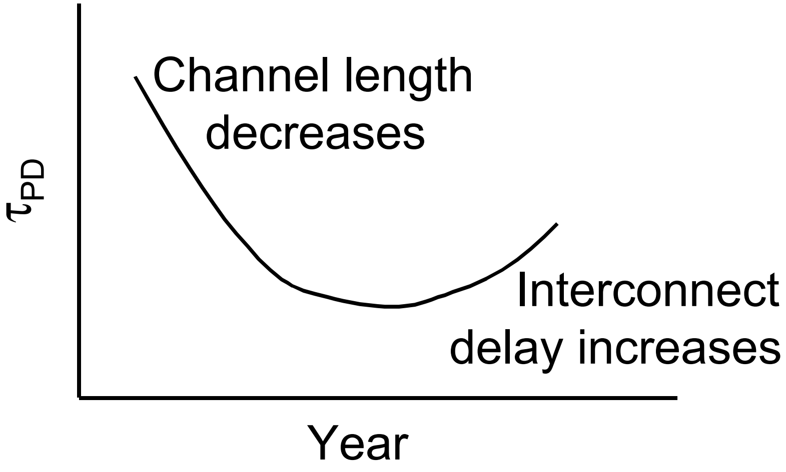
(Cross Section Transmission Electron Micrograph)

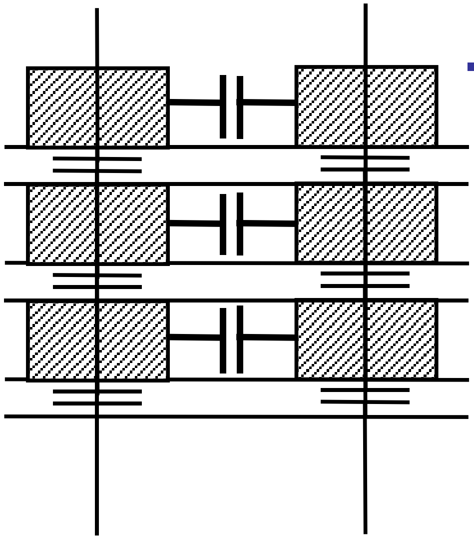


Courtesy Rudolph Technologies, Inc.

Interconnection Capacitance







Capacitance between metal lines can limit circuit performance

Consider device as adjunct to interconnections

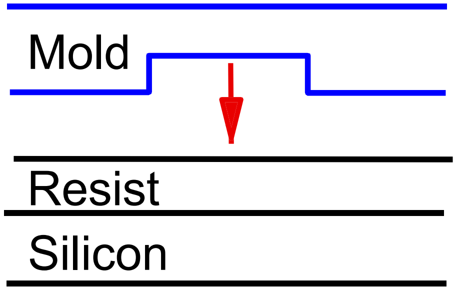
Wires → Nanowires

Nanowire:
Integrated Device and Interconnection

Interconnection Device Interconnection

Interconnection Field-Effect Transistor Interconnection

Nanoimprinting

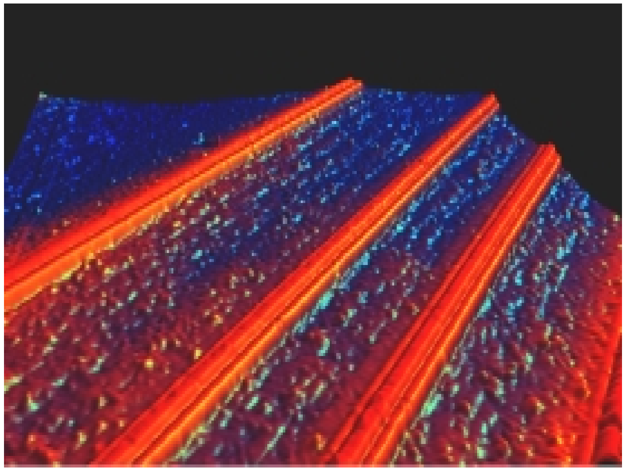


Mold

Resist

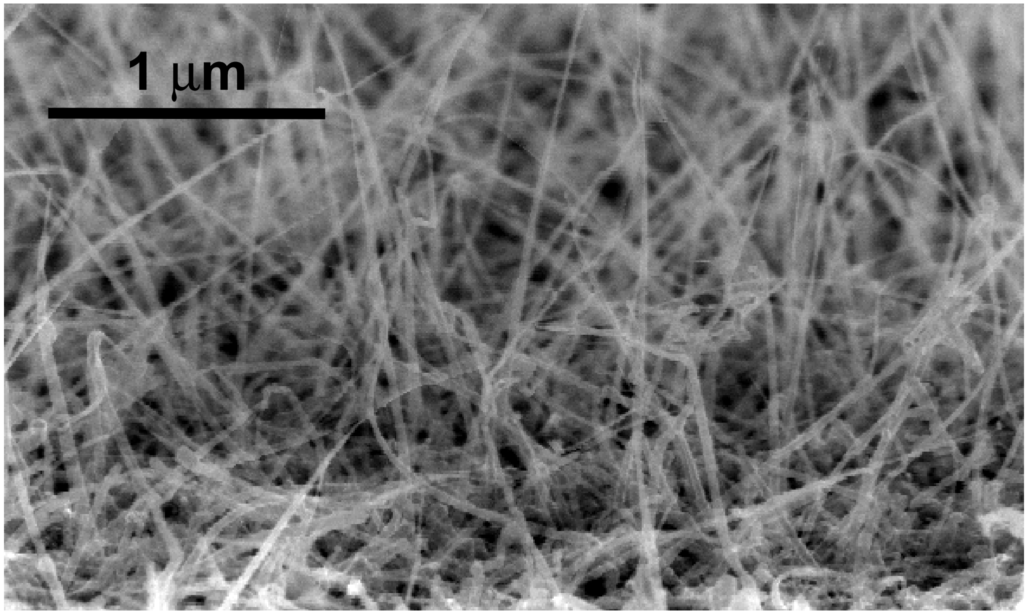
Silicon

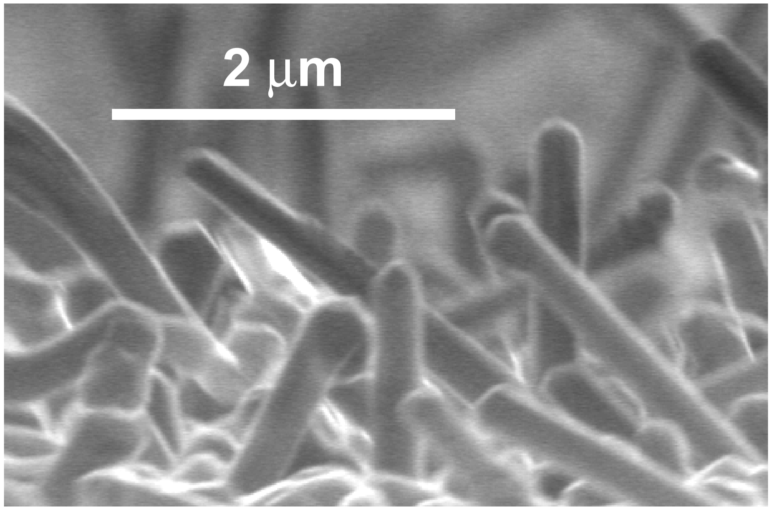
One-dimensional structure from anisotropic lattice strain



Yong Chen and Doug Ohlberg
Hewlett-Packard Labs

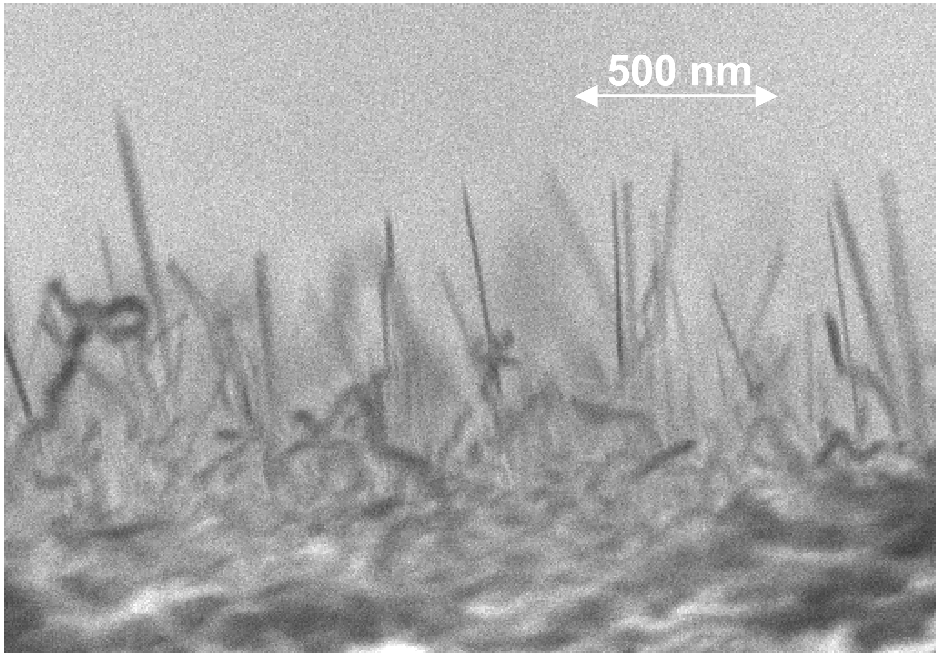
Metal-Catalyzed Si Nanowire Growth

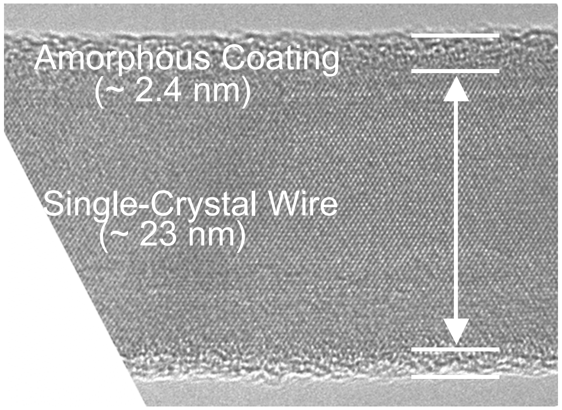




With Xuema Li and Tan Ha, Hewlett-Packard Labs

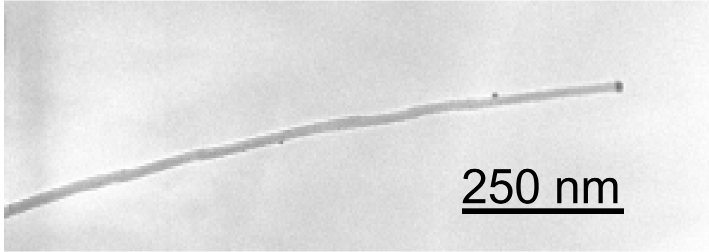
Dense Si Nanowires from $TiSi_x$ Islands

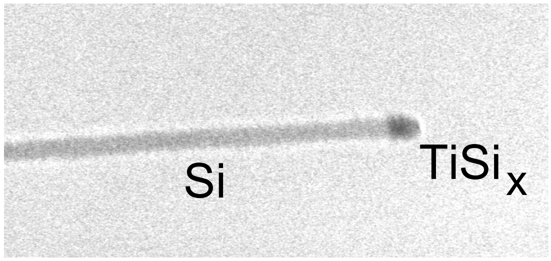


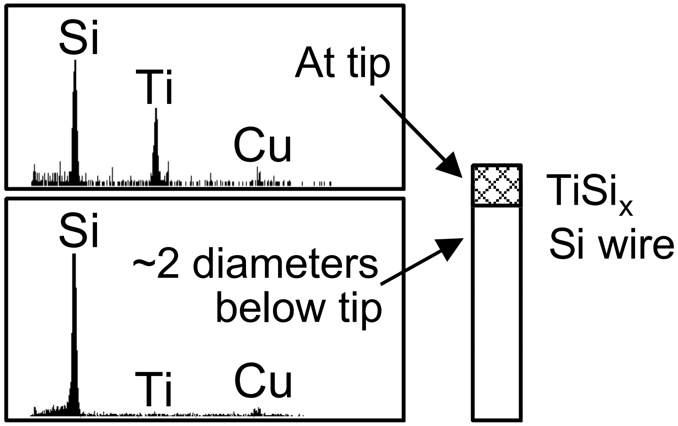


Micrographs by Thorsten Hesjedal,
Stanford University

Single-Crystal Si Nanowire with Metal Particle at Tip

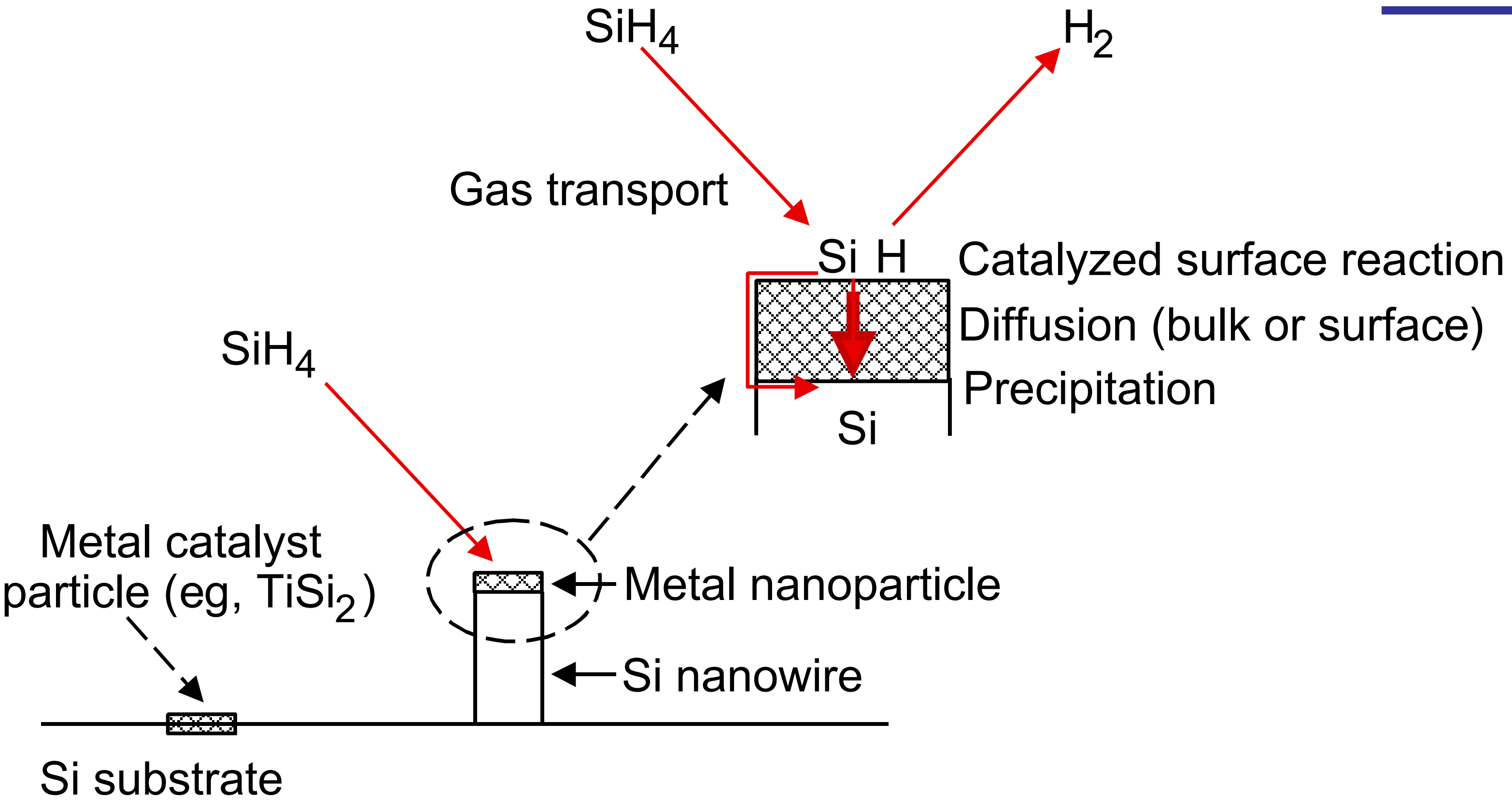






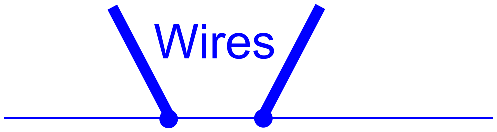
Analysis by T. Hesjedal, Stanford University
and D. Basile, Agilent Laboratories

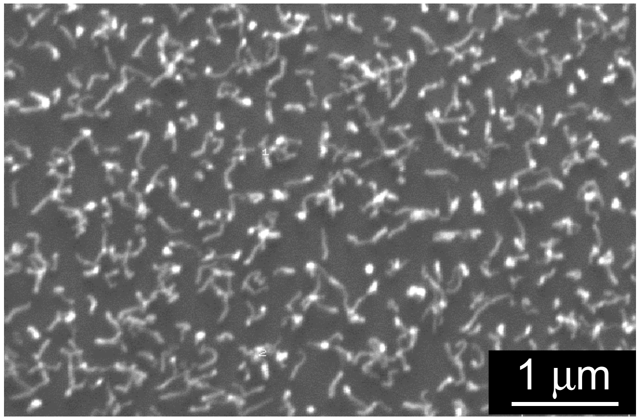
Mechanism of Nanowire Growth



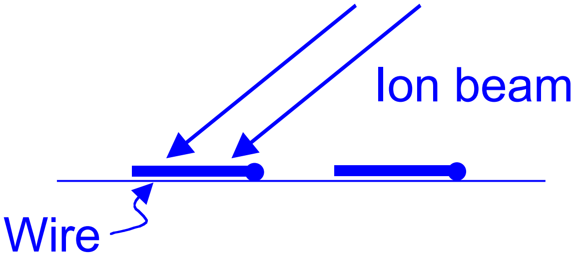
Aligning Nanowires Using an Ion Beam

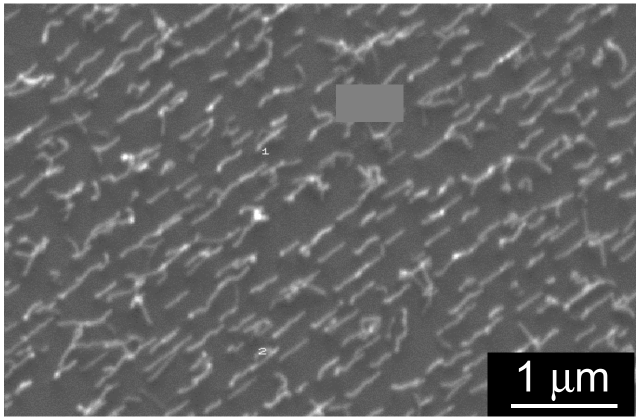
Sparse array after deposition





Sparse array after alignment



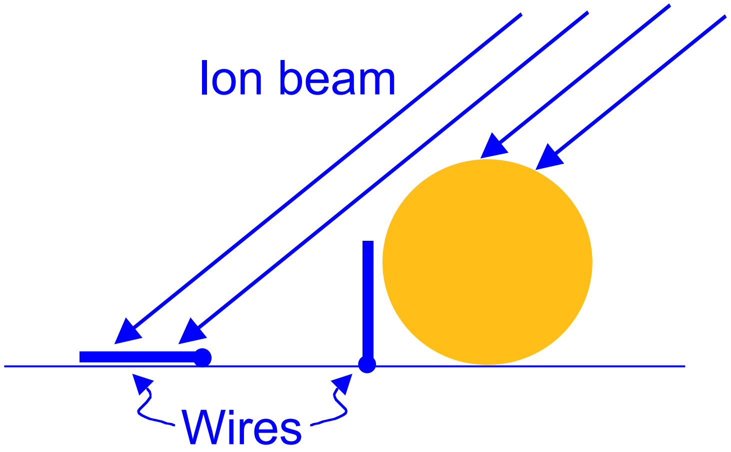


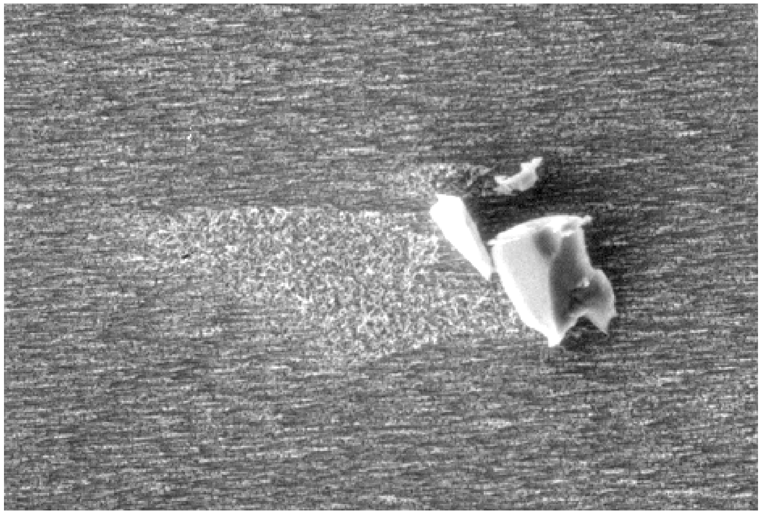
With Y.-L. Chang, Agilent Laboratories

Aligning Nanowires Using an Ion Beam

Shadowed wires

Dense array after shadowed alignment

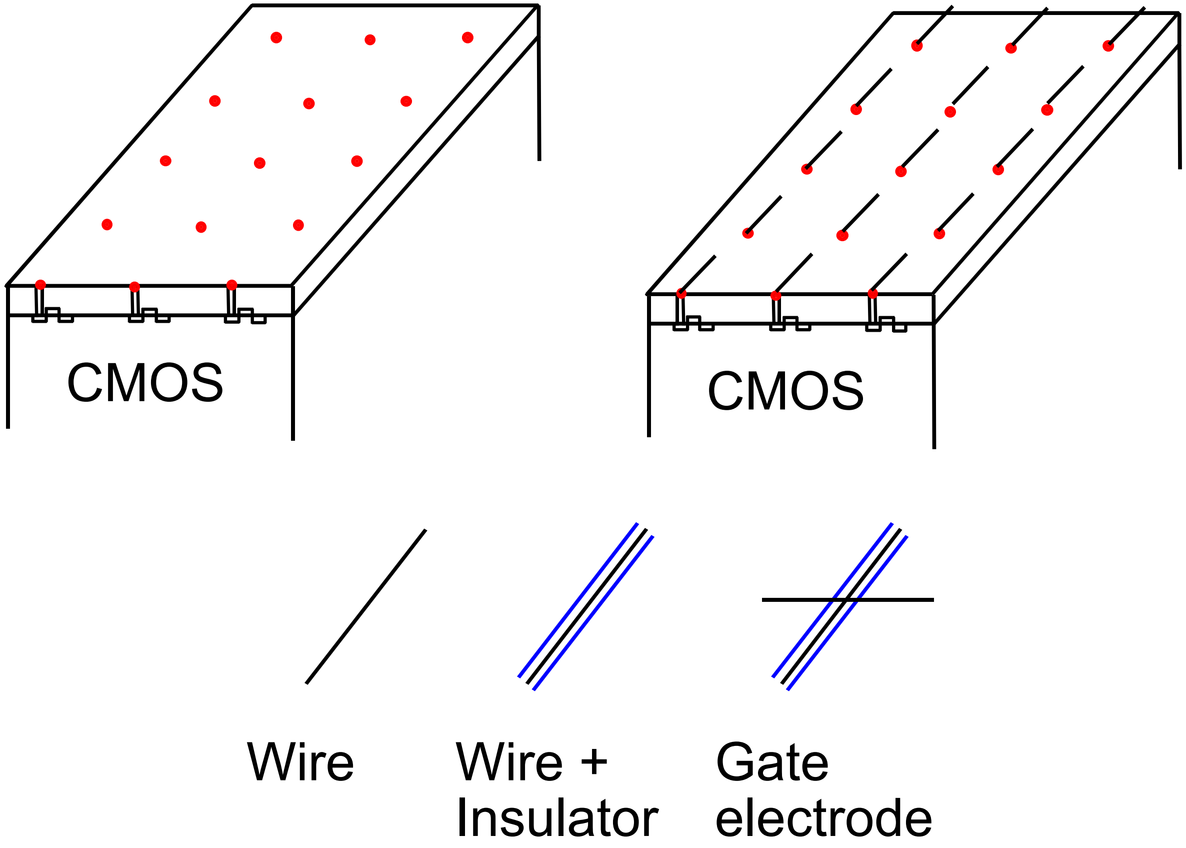




With M. Juanitas, Agilent Laboratories

Fabricate Nanowires on CMOS

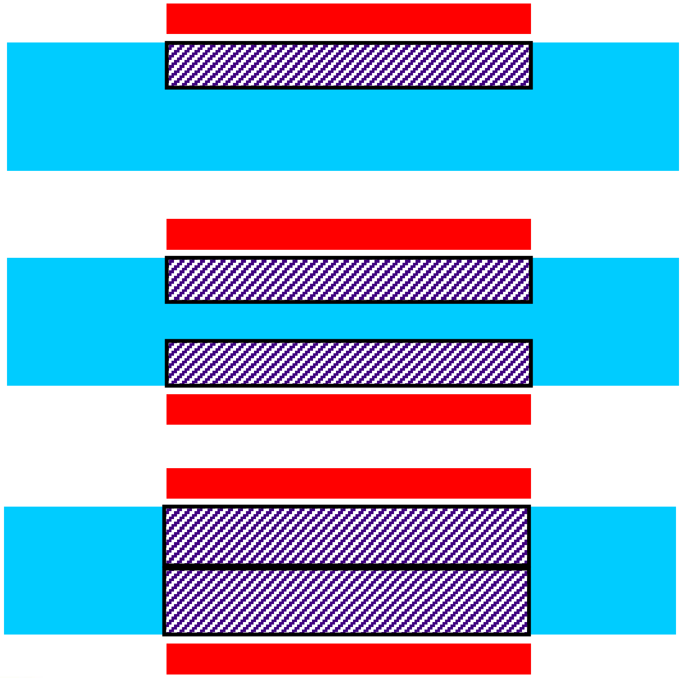
(CMOS for Gain and Interface Circuitry)



Nanowire: Uniform Doping

Normally ON transistor

$D < 2\, x_{dmax}$



Doping low enough so can deplete entire wire diameter

Limits conductance of interconnect

- Voltage drop along wire
- Time to charge next gate

Sensitive to size and doping

Back-Of-Envelope Estimates

One-dimensional analysis

  Need 2 or 3-dimensional analysis

Use equations for planar geometry

Let L = D

Assume no fabrication limits

Assume no short-channel effects

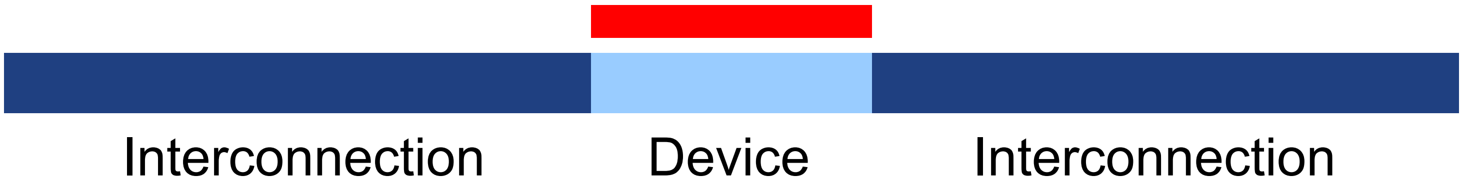
Nonsense,

…but should stimulate discussion

Uniformly Doped Nanowire Transistors

	D = 20 nm	**D = 5 nm**
$X_{dmax} = \sqrt{\frac{4\,\varepsilon_s\,\phi_B}{q\,N_D}} \sim \frac{D}{2}$	10 nm	2.5 nm
$N_{Dmax} \sim 5 \times 10^7 / D^2 \sim 1/D^2$	$1.3 \times 10^{19}\ \text{cm}^{-3}$	$2.1 \times 10^{20}\ \text{cm}^{-3}$
$N = \frac{\pi}{4} D^2\, L_D\, N_{Dmax} \sim D$	81	21
$\frac{\Delta N}{N} \sim \sqrt{N} \sim 1/D^{1/2}$	11%	22%
$\rho = \frac{1}{ne\mu} \sim D^2$	$5 \times 10^{-3}\ \Omega\text{-cm}$	$4 \times 10^{-4}\ \Omega\text{-cm}$
$R = \frac{\rho\, L_l}{A_x} \sim \frac{D^2}{D^2\ \mu(N_D)}$	$1.5 \times 10^5\ \Omega$	$2 \times 10^5\ \Omega$
$I \sim \frac{V}{R} \sim O\ (D^0)$	6 μA	5 μA
$Q = q\,N \sim D$	1.3×10^{-17} C	3×10^{-18} C
$\tau = Q / I \sim D$	2.2 ps	0.6 ps

Selective Doping

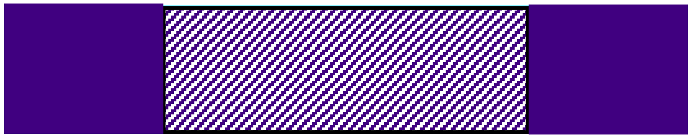


Bulk (eg implant)
Surface induced

Selective Doping

Heavy doping (~sol.sol.)

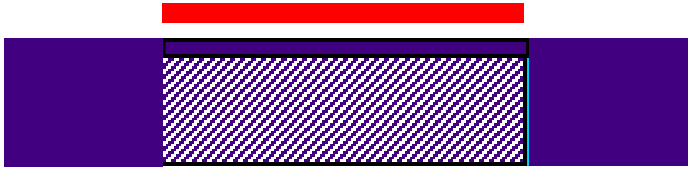
Light doping (~ intrinsic or opposite type)



Intrinsic

Normally OFF transistor

$D \nless 2\, x_{d\max}$



Induce channel

Sensitive to wire diameter

Analogous to fully depleted or partially depleted SOI

Selectively Doped Nanowire Transistors

	D = 20 nm	**D = 5 nm**
$X_{dmax} >> \frac{D}{2}$	>>10 nm	>>2.5 nm
$C_{ox}=\frac{\varepsilon_{ox} A_s}{x_{ox}} = \frac{\varepsilon_{ox} \pi D L_D}{x_{ox}} \sim D^2$	2.2×10^{-17} F	1.4×10^{-18} F
$N = C_{ox} V/q \sim D^2$	140	9
$\frac{\Delta N}{N} \sim \sqrt{N} \sim D^{-1}$	8%	33%
$\rho = \frac{1}{ne\mu} \sim D^0$	1.5×10^{-4} Ω-cm	1.5×10^{-4} Ω-cm
$R = \frac{\rho L_l}{A_x} \sim 1/D^2$	5×10^3 Ω	8×10^4 Ω
$I \sim \frac{V}{R}$	200 μA	12 μA
$\tau = R C \sim D^0$	0.1 ps	0.1 ps

Summary

Metal-catalyzed nanowires (D < 20 nm)

Alignment possible

Uniform doping limits performance

Selective doping more flexible

Detailed modeling needed
    (with realistic fabrication constraints)