Metal-Catalyzed Nanowires for Integrated Devices and Interconnections

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Metal-Catalyzed Nanowires for Integrated Devices and Interconnections

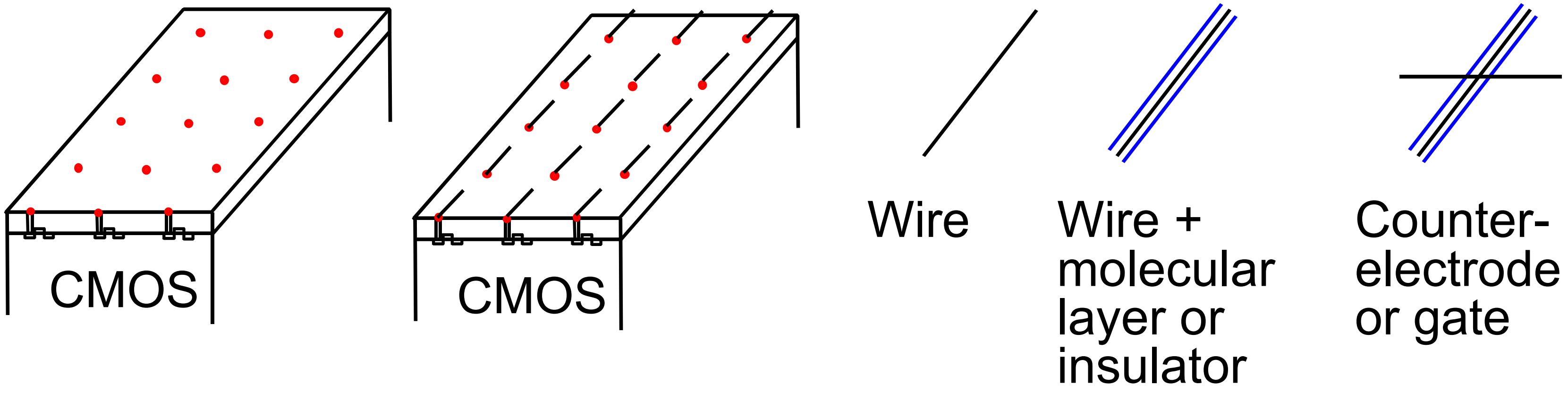
Si (and Ge) Nanowires

Outline

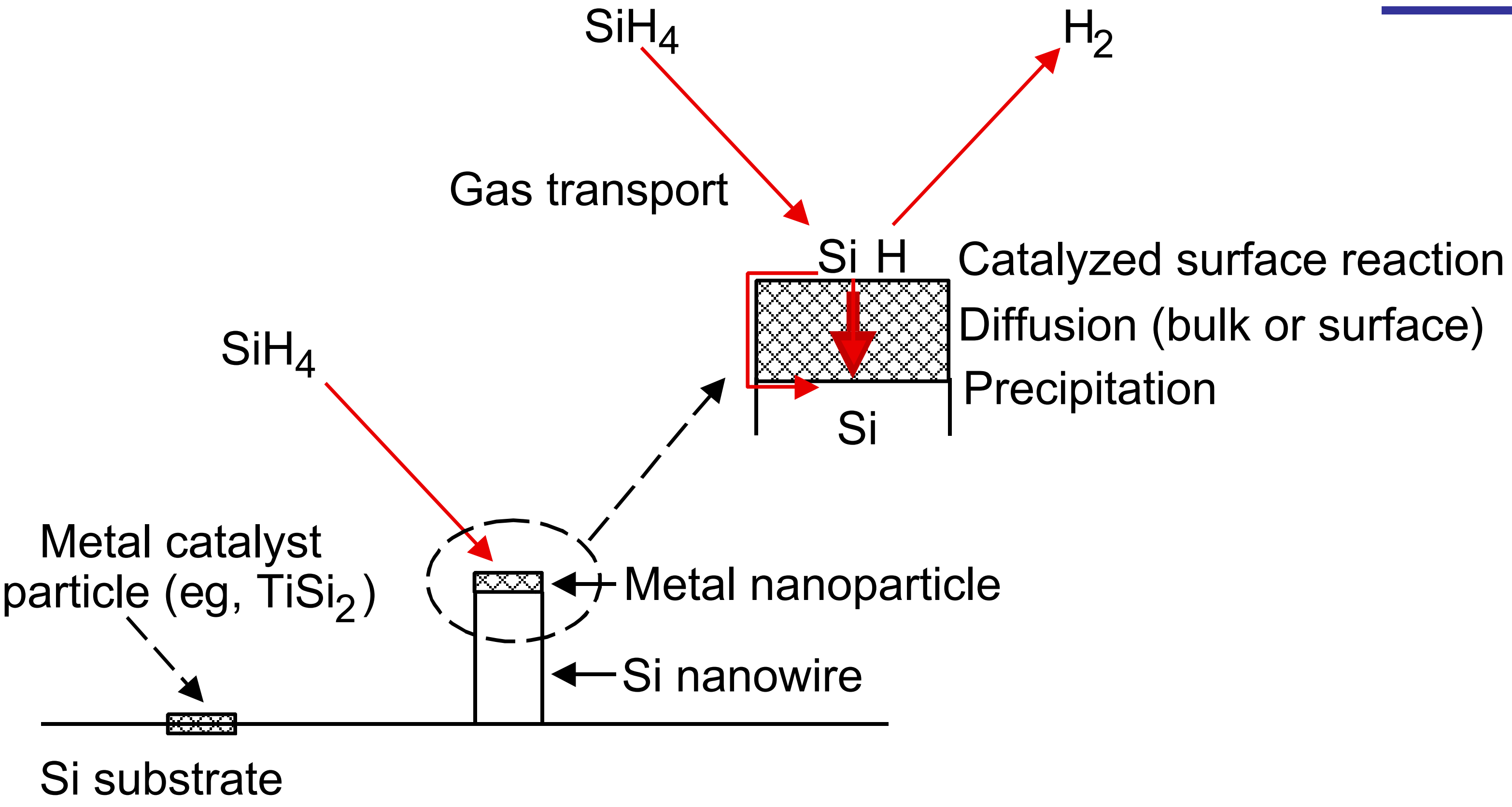
- Metal-catalyzed growth
  - Catalyst nanoparticles
  - Wire growth
- Stability during further processing
- Speculation about integrating devices and interconnections

Integration of Nanowires with CMOS

- CMOS provides gain and interface circuitry
  - Partially processed CMOS (700°C)
  - Fully processed CMOS (400°C)
- Perhaps as interconnections for molecular electronics
- Perhaps place some modulating element within wire



Metal Catalyzed Nanowire Growth



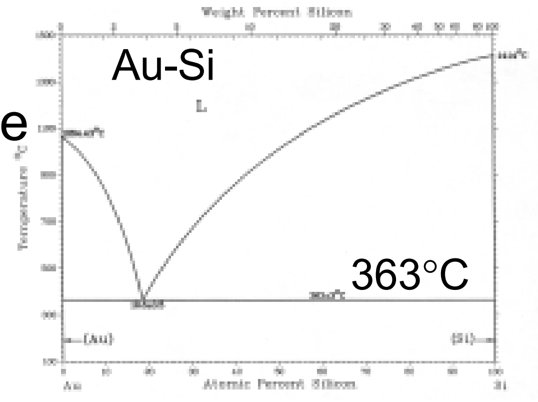
Catalytic Nuclei: Material

Desired characteristics:

Not a deep energy level in Si bandgap

Low solid solubility in Si

Liquid eutectic below deposition temperature (for VLS growth)



Au: Liquid eutectic: ~360°C for Si and Ge

E_t-E_i ~ 0: Mid-gap g-r center

$N_{ss} = 10^{17}$ cm^{-3}

Need barrier layers if used with Si ICs

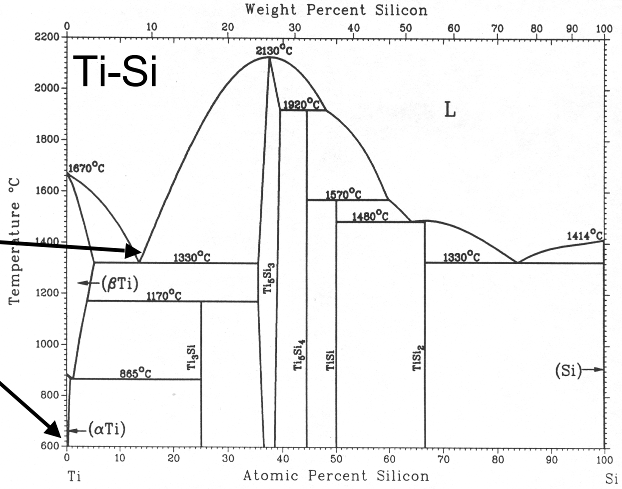
Ti: E_t-E_i ~ 0.34 eV

N_{ss} ~ 10^{12} cm^{-3}

Liquid eutectic: 1350°C

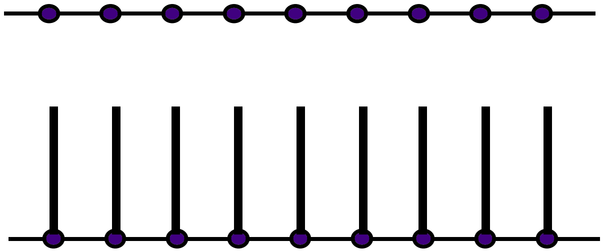
Deposition temperature: ~600°C

(probably not VLS growth)

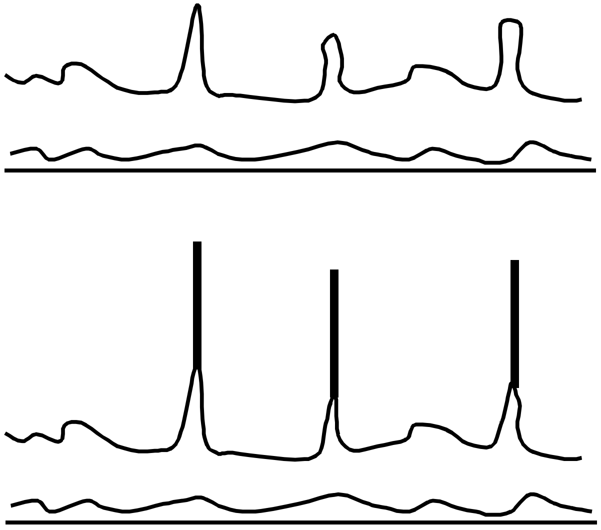


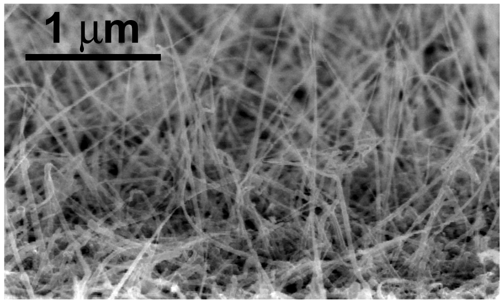
Catalytic Nuclei: Form

Isolated Nuclei



Layer





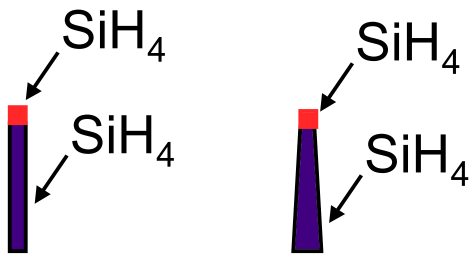
Si on evaporated Ti
Si grown at ~620°C

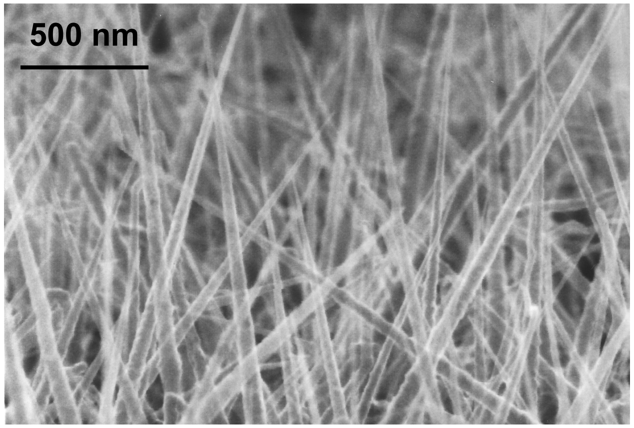
Si Nanowires on Ti

Wire diameter: 20-40 nm

Tapered at higher temperatures

- Uncatalyzed growth on sides of wires





Reduce taper by limiting uncatalyzed deposition rate

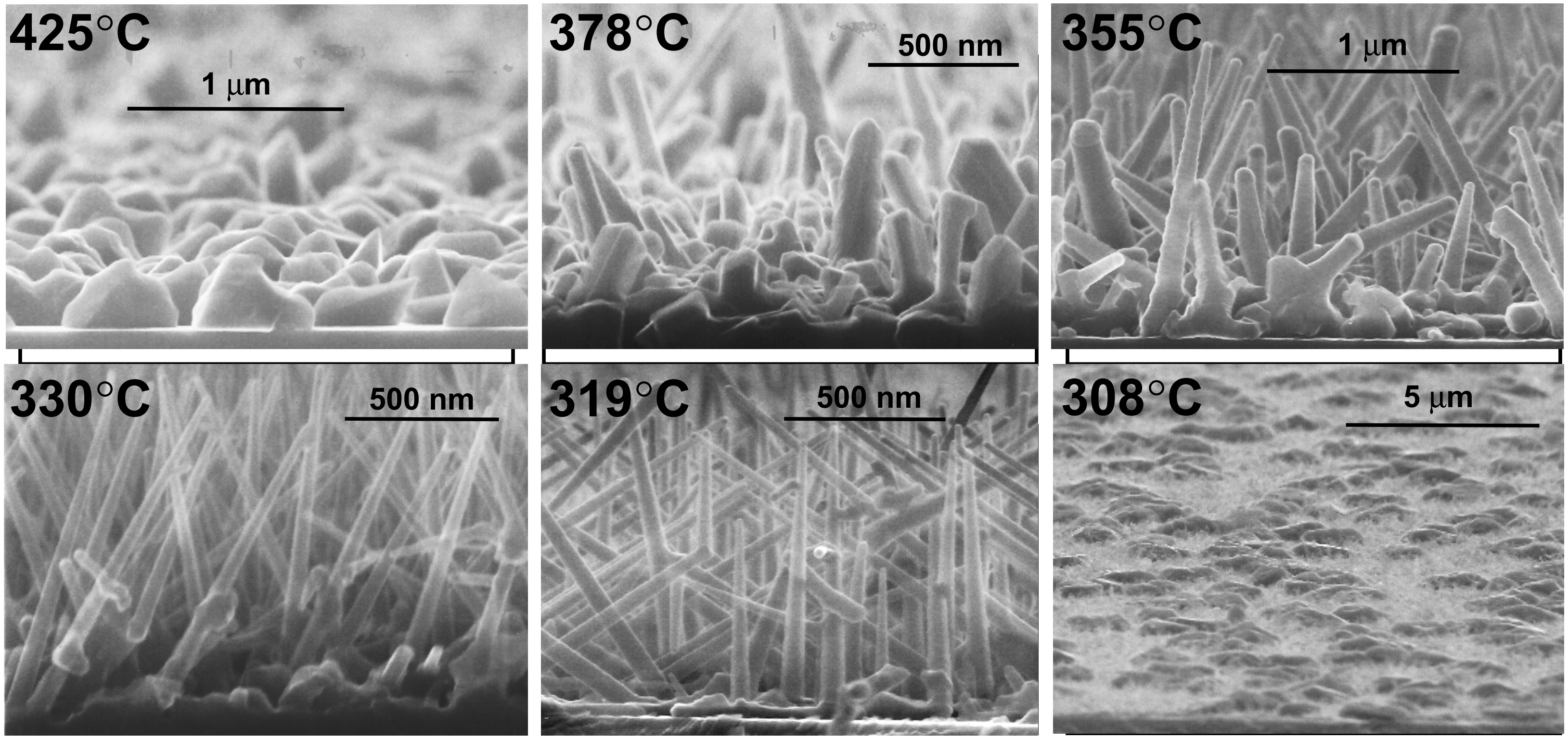
- Reduce temperature
- Less reactive Si source: *eg,* SiH_2Cl_2
- Add HCl

Nanowires formed in 600°C temperature range:
Compatible with partially processed CMOS

Lower Temperatures for CMOS Compatibility
Ge Nanowires on Au Nanoparticles

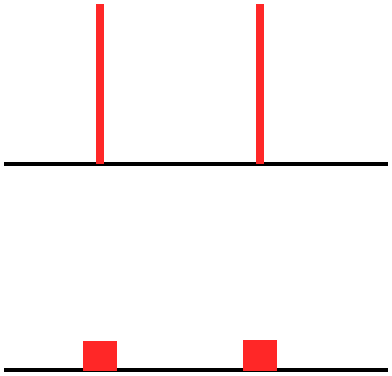
Temperature range for wire growth: ~315– 370°C

Wire diameter ~ 40 nm on ~20 nm Au nanoparticles



Stability of Si Nanowires

- How stable are nanowires?
  - Process integration easier if more stable
- Instability caused by surface diffusion
  - Native oxide expected to stabilize
- Consider different ambients
  - Inert vs. reducing
  - Intermediate air-exposure
    - (In-situ *vs.* ex-situ annealing)



- Inert ambient after air exposure: N_2:
  - Stable to >950°C
- Slightly reducing ambient after air exposure: 4%H_2/N_2
  - Also stable to ~950°C
- Strongly reducing ambient after air exposure: H_2
- Strongly reducing ambient - no air exposure: H_2

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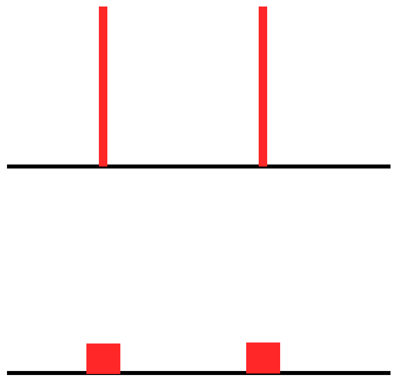

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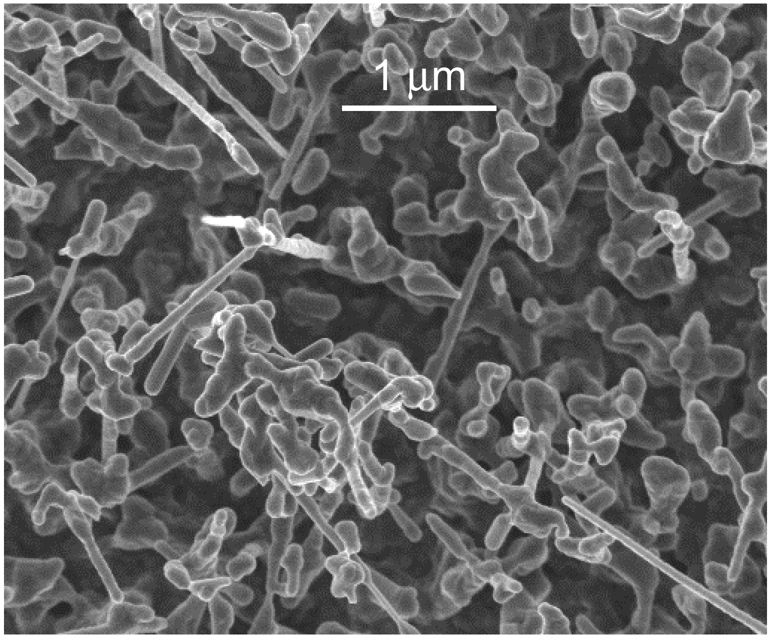
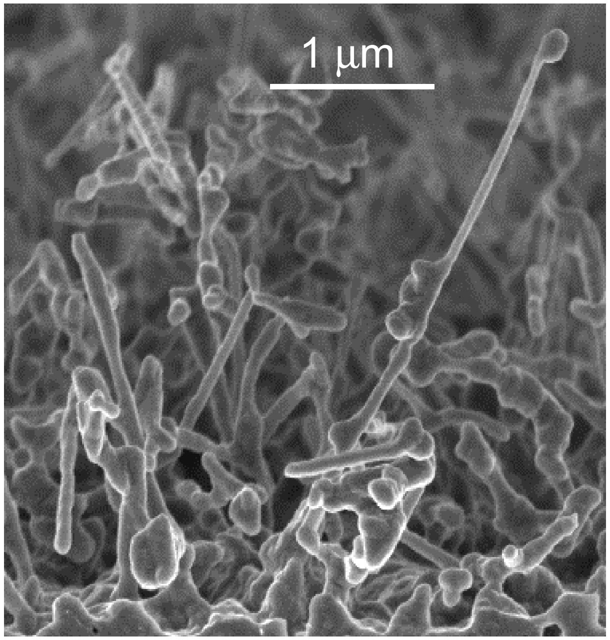
Stability (or lack of): 900°C in H_2
Si Nanowires on Ti

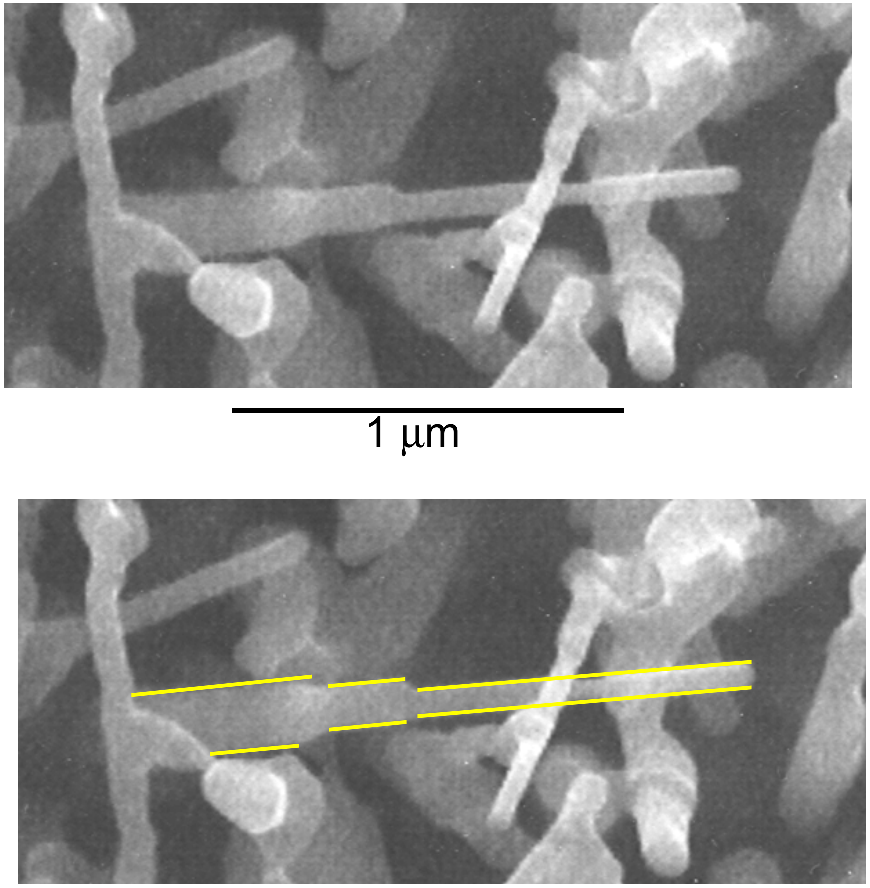


(Plan view)

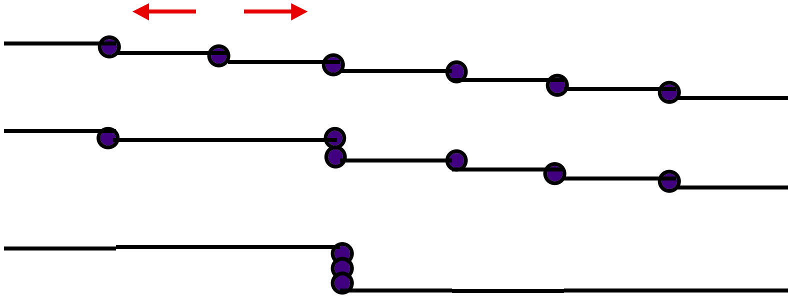


(Cross section)

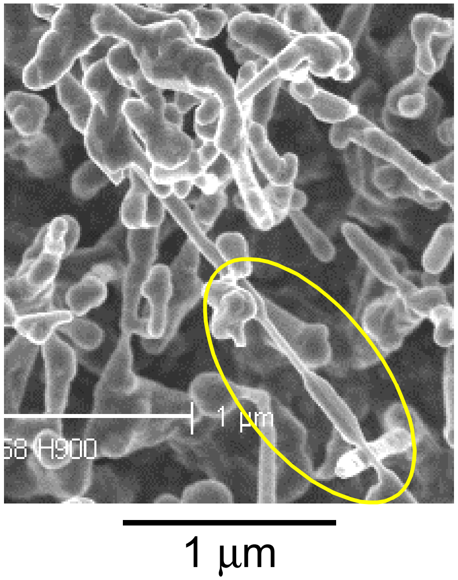
Step Bunching on Tapered Nanowire

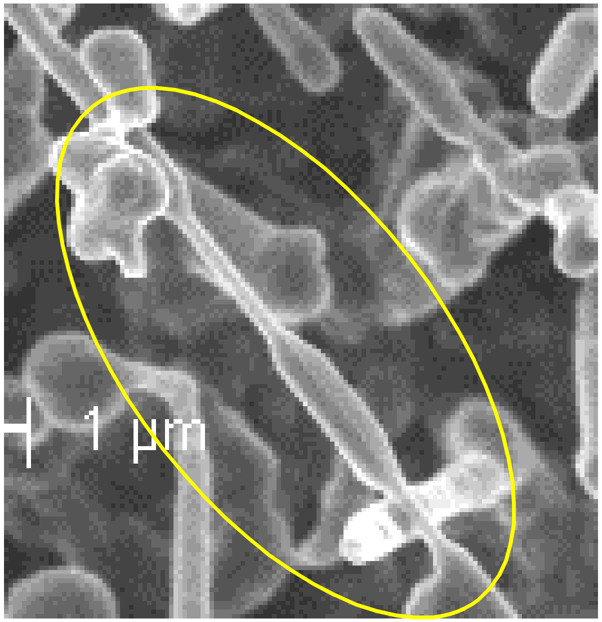


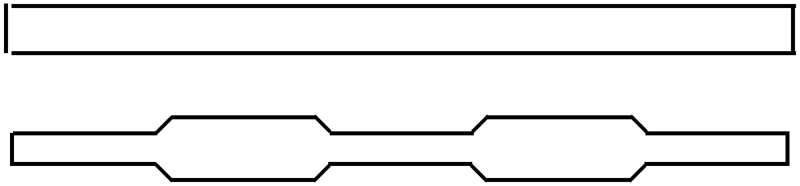
Rapid surface diffusion
Limited by step
detachment/attachment



Instability along Uniform Nanowire



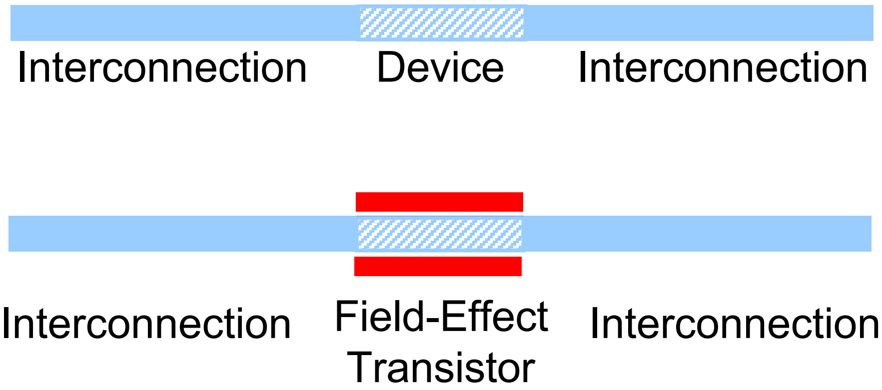




F. A. Nichols and W. W. Mullins, Trans. Met. Soc. AIME **233**, 1840 (1965).

Lord Rayleigh, Proc. London Math. Soc. **10**, 4 (1878).

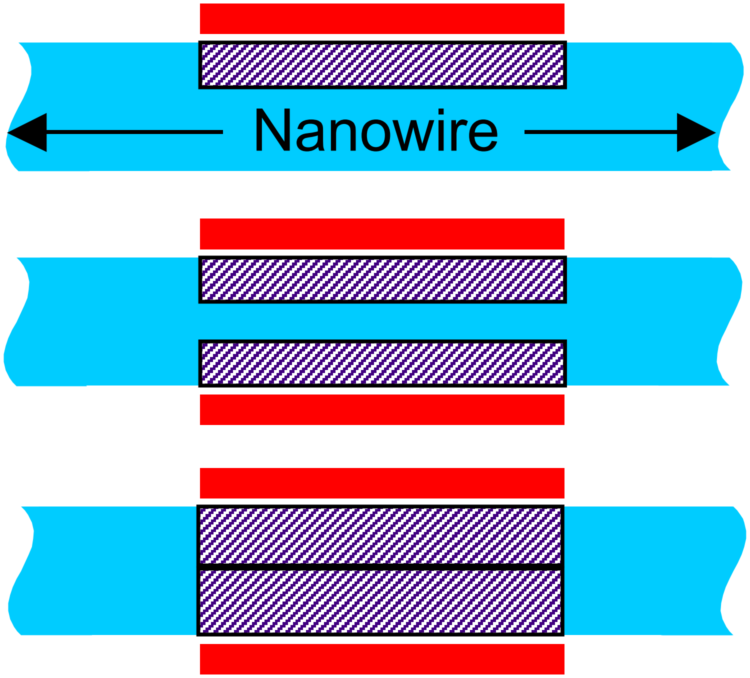
Nanowire: Integrated Device and Interconnection



Trade-off: Series resistance vs. Transistor Characteristics

Two cases: Uniform doping
Selective doping

Nanowire: Uniform Doping



Normally ON transistor

$D < 2\ x_{dmax}$

Doping low enough so can deplete entire wire diameter

Limits conductance of interconnect

- Voltage drop along wire
- Time to charge next gate

Sensitive to size and doping

Back-Of-Envelope Estimates

One-dimensional analysis
  Need 2 or 3-dimensional analysis
Use equations for planar geometry
Let L = D
Assume no fabrication limits
Assume no short-channel effects

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One-dimensional analysis
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Let L = D
Assume no fabrication limits
Assume no short-channel effects
Nonsense, of course,
…but should stimulate discussion

Uniformly Doped Nanowire Transistors

	D = 20 nm	**D = 5 nm**
$X_{dmax} = \sqrt{\frac{4\, \varepsilon_{\mathbf{s}}\, \phi_B}{q\, N_D}} \sim \frac{D}{2}$	10 nm	2.5 nm
$N_{Dmax} \sim 5 \times 10^7 / D^2 \sim 1/D^2$	$1.3 \times 10^{19}\ \mathrm{cm}^{-3}$	$2.1 \times 10^{20}\ \mathrm{cm}^{-3}$

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$N_{Dmax} \sim 5 \times 10^7 / D^2 \sim 1/D^2$	1.3×10^{19} cm^{-3}	2.1×10^{20} cm^{-3}
$N = \frac{\pi}{4} D^2 L_D N_{Dmax} \sim D$	81	21
$\frac{\Delta N}{N} \sim \sqrt{N} \sim 1/D^{1/2}$	11%	22%
$\rho = \frac{1}{ne\mu} \sim D^2$	5×10^{-3} Ω-cm	4×10^{-4} Ω-cm
$R = \frac{\rho\,L_l}{A_x} \sim \frac{D^2}{D^2\,\mu(N_D)}$ ($L_l = 1\ \mu$m)	$1.5 \times 10^5\ \Omega$	$2 \times 10^5\ \Omega$

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$I \sim \frac{V}{R} \sim O\,(D^0)$	6 μA	5 μA
$Q = q\,N \sim D$	1.3×10^{-17} C	3×10^{-18} C
$\tau = Q / I \sim D$	2.2 ps	0.6 ps

Selective Doping

Interconnection Device Interconnection

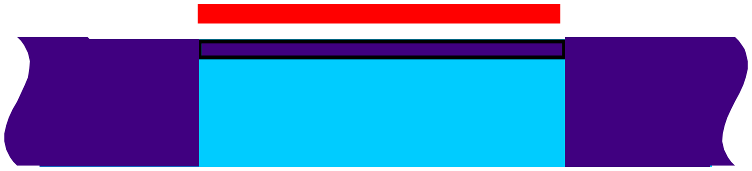
Bulk (e.g., implant)
Surface induced

Heavy doping (~sol.sol.)

Light doping (~ intrinsic or opposite type)

Normally OFF transistor

$D \nless 2 x_{dmax}$



Induce channel

Intrinsic: Not sensitive to dopant fluctuations

Sensitive to wire diameter

Selectively Doped Nanowire Transistors

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$X_{dmax} >> \frac{D}{2}$	>>10 nm	>>2.5 nm

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$N = C_{ox} V/q \sim D^2$	140	9
$\frac{\Delta N}{N} \sim \sqrt{N} \sim D^{-1}$	8%	33%
$\rho = \frac{1}{ne\mu} \sim D^0$	1.5×10^{-4} Ω-cm	1.5×10^{-4} Ω-cm
$R = \frac{\rho L_l}{A_x} \sim 1/D^2$ ($L_l = 1$ μm)	5×10^3 Ω	8×10^4 Ω

Selectively Doped Nanowire Transistors

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$R = \frac{\rho L_l}{A_x} \sim 1/D^2$ (L_l = 1 μm)	5×10^3 Ω	8×10^4 Ω
$I \sim \frac{V}{R}$	200 μA	12 μA
$\tau = R C \sim D^0$	0.1 ps	0.1 ps

Metal-Catalyzed Nanowires for Integrated Devices and Interconnections

Si (and Ge) Nanowires

Summary

- Metal-catalyzed growth
  - Catalyst nanoparticles
  - Wire growth
- Stability during further processing
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