Self-Assembled Nanostructures: Ge on Si

Presented by
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Outline

Limits of Device Scaling

- Alternative Device Concepts

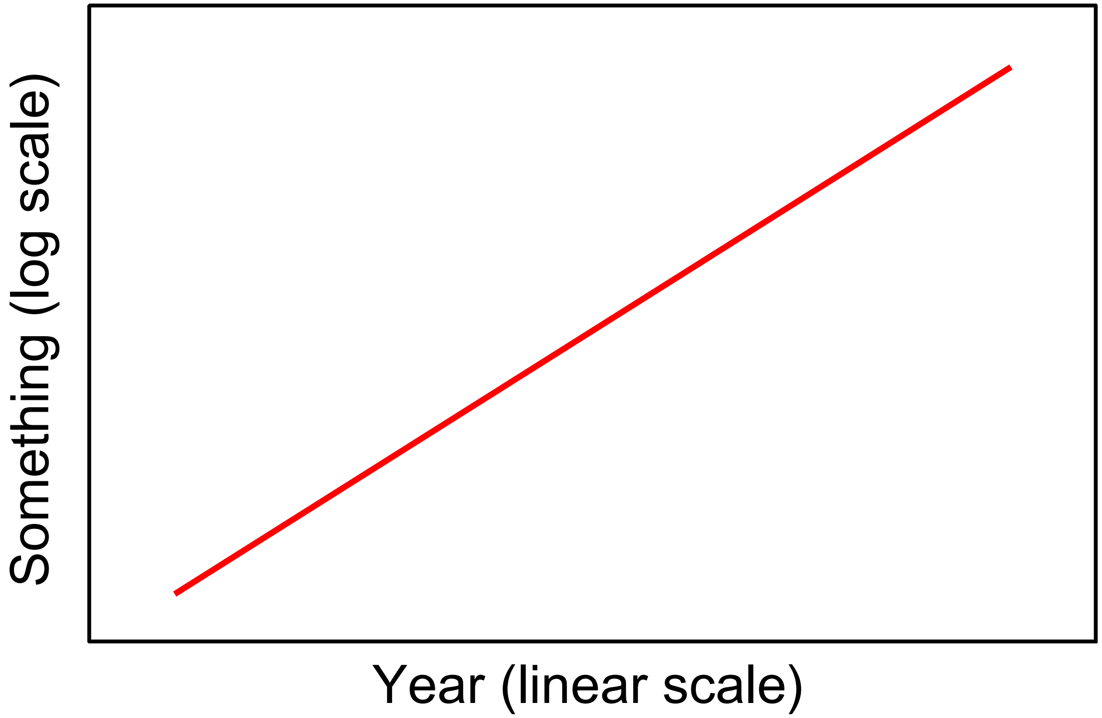
Self-Assembled Nanostructures

- Forming small structures
  - Putting them where we want them
- Zero-dimensional structures
  - Strain from lattice mismatch

Enabling Concept

- Defect Tolerance

Moore's Law (General Case)

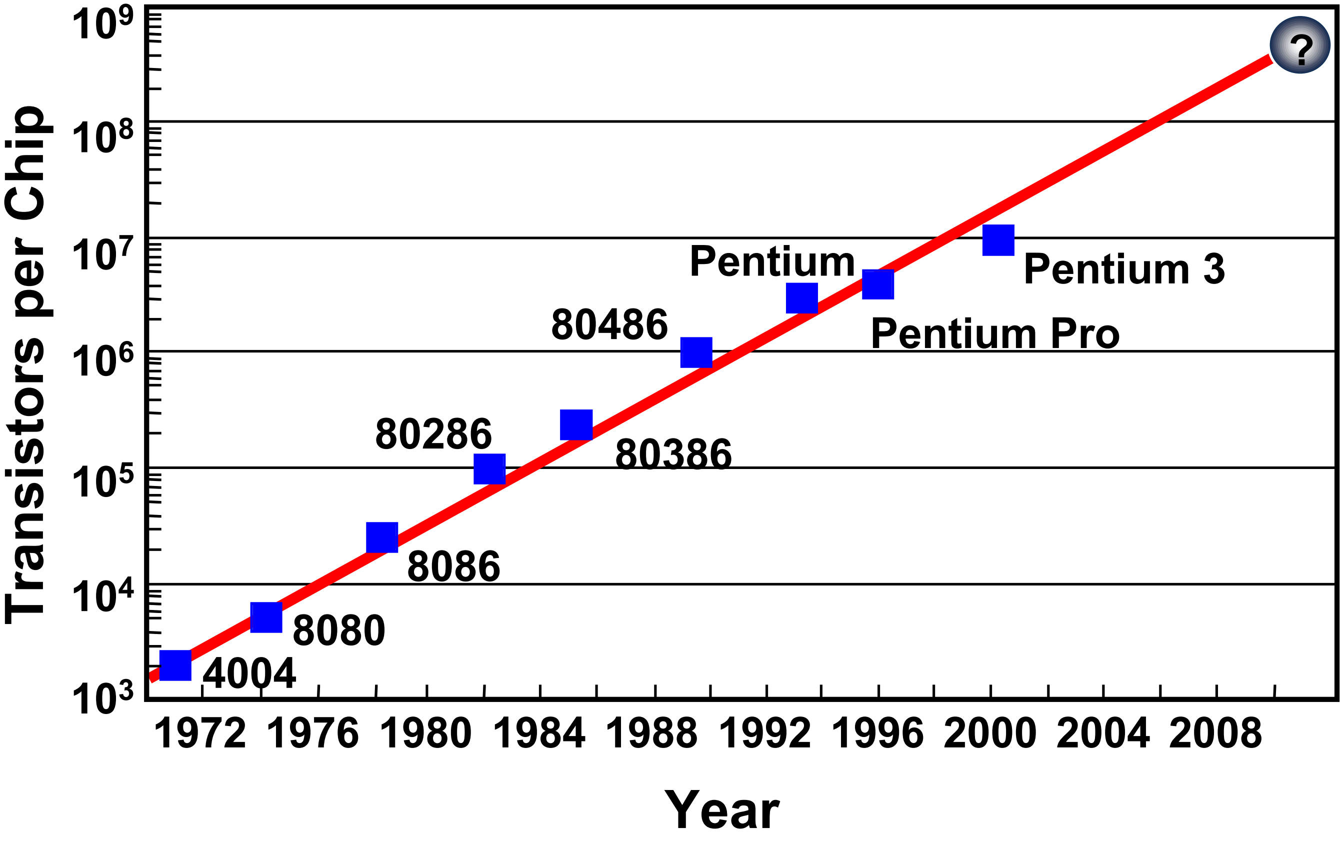


Even Dilbert uses Moore's Law

(Reference: Scott Adams “Dilbert,” July 15, 1997)

Moore's Law

Number of Transistors

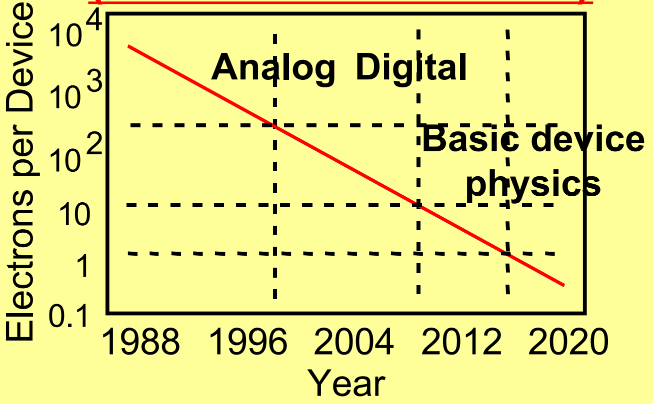


Critical Issues

Device size and density

- Physically small features
- Operation with small features
- Limited number of electrons
- Interconnections

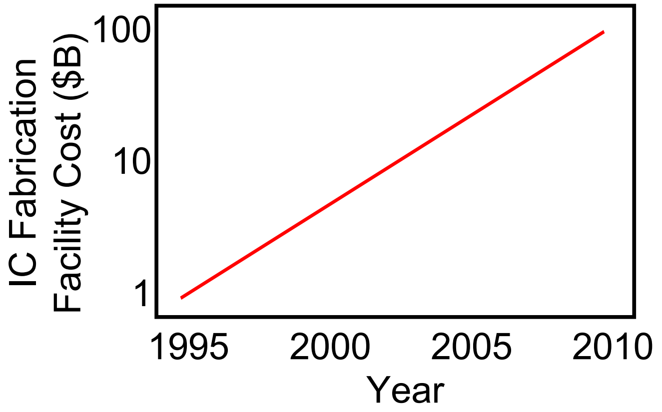
Moore's Law (Number of Electrons)



Cost

- Minimize expensive lithography
- Self (or directed) assembly
- Simpler architecture
- Defect-tolerant architecture

Moore's "Second Law" Cost of IC Fabrication Facility



Potential Devices

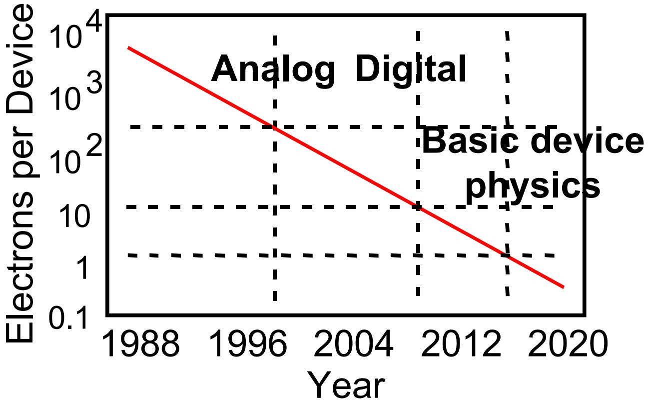
Single-electron devices
Quantum cellular automata
Molecular electronics
Quantum computing

Critical Issues

Device size and density

Physically small features
Operation with small features
Limited number of electrons
Interconnections

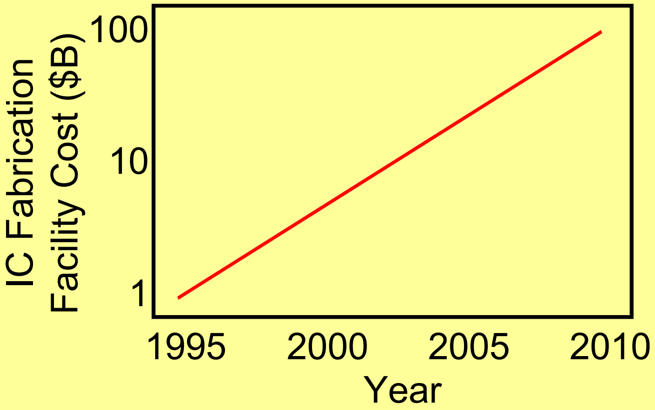
Moore's Law
(Number of Electrons)



Cost

Minimize expensive lithography
Self (or directed) assembly
Simpler architecture
Defect-tolerant architecture

Moore's "Second Law"
Cost of IC Fabrication Facility



Self-Assembled Nanostructures
Zero Dimensional Islands on Si

Use directed-assembly to extend Moore's law

- Determine critical dimensions by choice of materials and deposition kinetics ("self assembly"), not lithography
- Use lithography to position devices or arrays of devices ("directed assembly")

Use small-size effects to perform logic, storage, and computation

- Coulomb blockade or quantum confinement

Methods of self- or directed- assembly

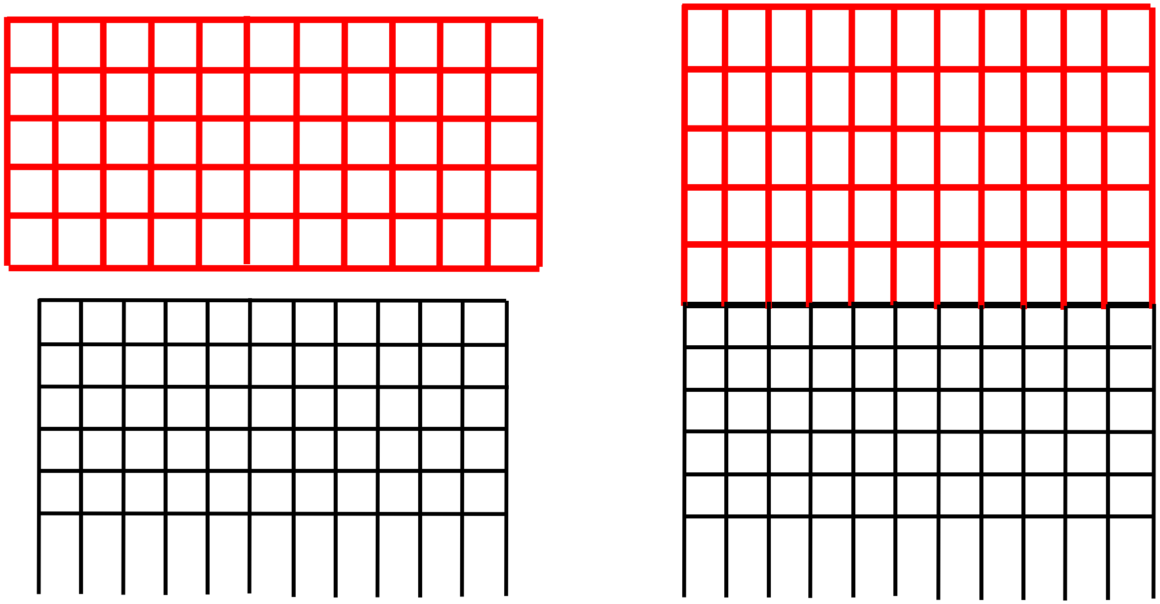
- Strain from lattice mismatch
- Catalytic wire growth on nanoparticle

Thermodynamically assembled structures

- Several percent defects
- Need defect-tolerant architecture

Strained-Layer Epitaxy

Compress SiGe lattice to match silicon



SiGe

Si

SiGe

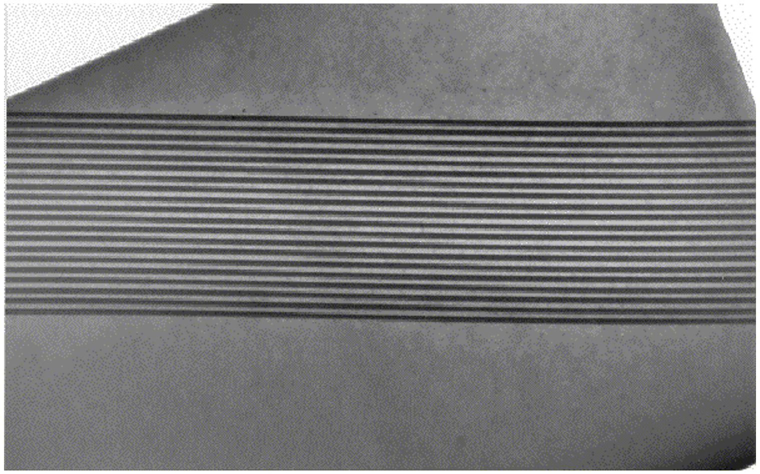
Si

Can Accommodate Moderate Strain Multilayer Si/SiGe Structure

150 nm Si cap

20 x 3 nm SiGe
19 x 3.5 nm Si

Si substrate



- Average SiGe layer thickness: 3 nm + 0.2 nm
- Average Si layer thickness: 3.5 nm + 0.2 nm
- Si source: SiH_2Cl_2
- Temperatures: 625°C (SiGe), 690°C (Si)

Large Strain + Surface Diffusion Allows Surface Roughening

Deposit one material on another

Large strain → self-assembled islands (quantum dots)

Small islands → quantum or Coulomb-blockade effects

Focus on Ge on Si

Why Ge on Si?

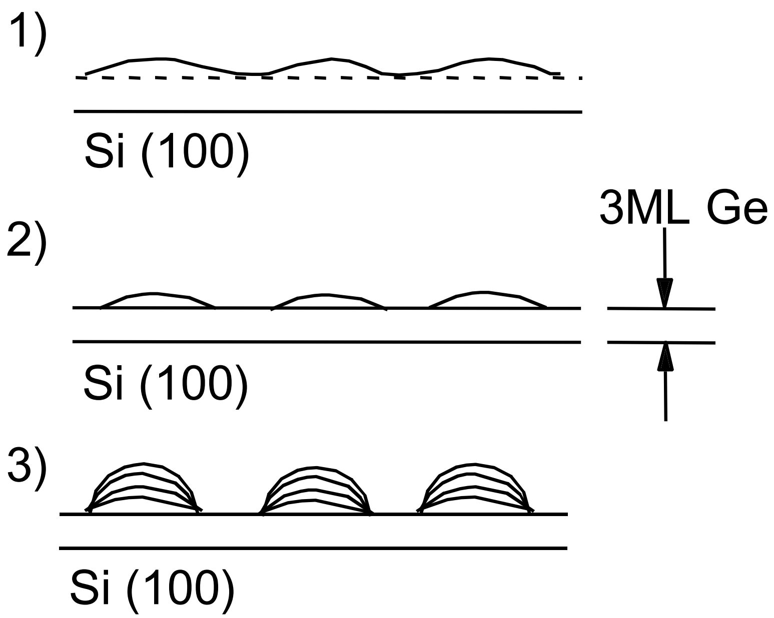
Compatible with Si IC technology

Deposition by

Chemical Vapor Deposition

(or Physical Vapor Deposition)

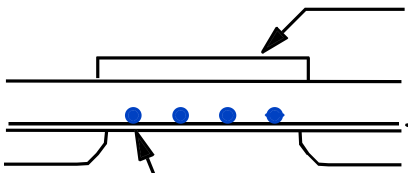
Energy and Kinetics Influence Island Formation



Possible Device Applications

Random Arrangement

Nonvolatile memory

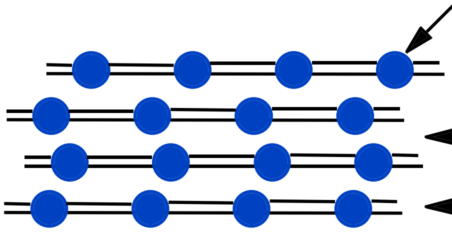


Control gate

Tunnel oxide

Storage region
(Si dots)

Long-wavelength photodetectors
(or possibly emitters)



Ge

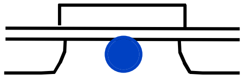
Si

SiO_2

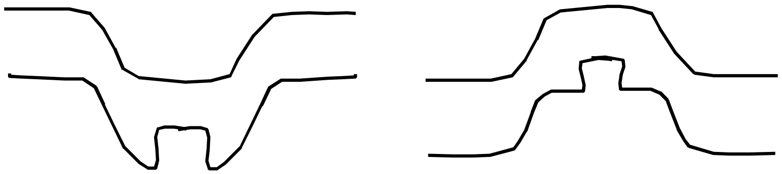
Aligned

MOS for logic

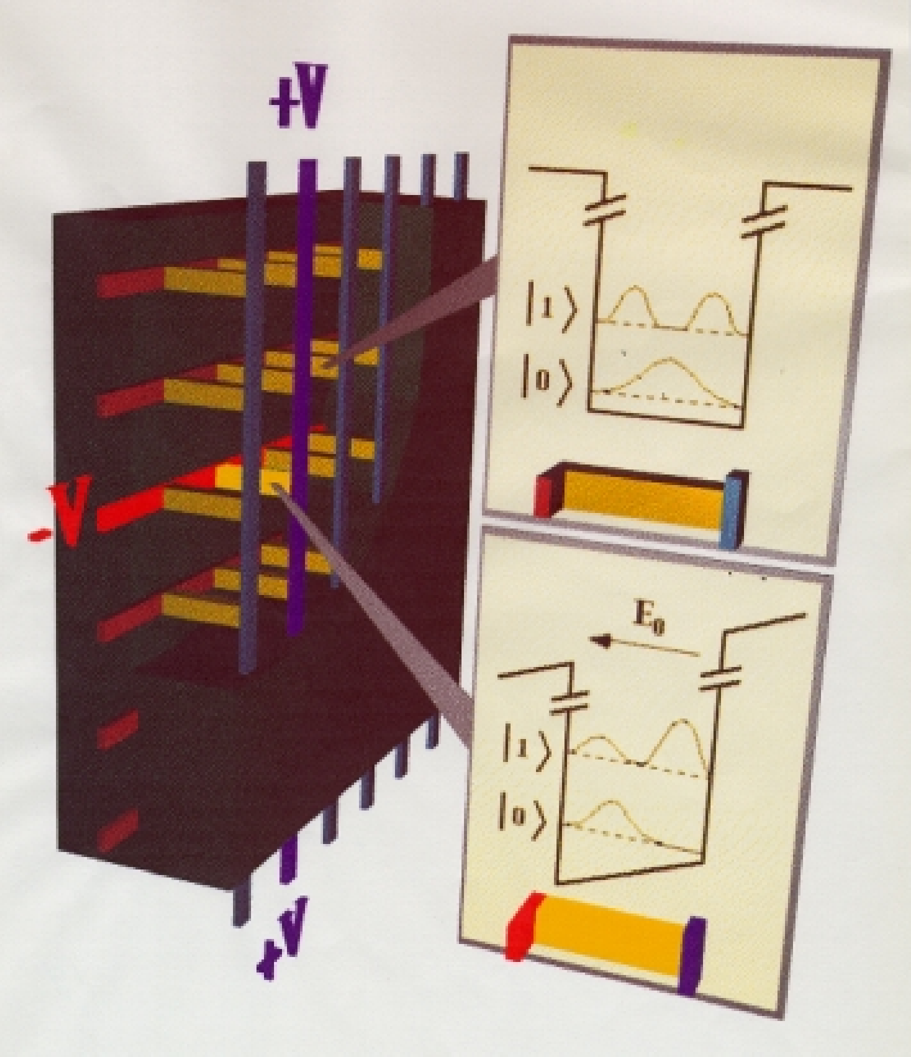
Possible barrier to short-channel (substrate) effects



Gate oxide



Quantum Dot Computer



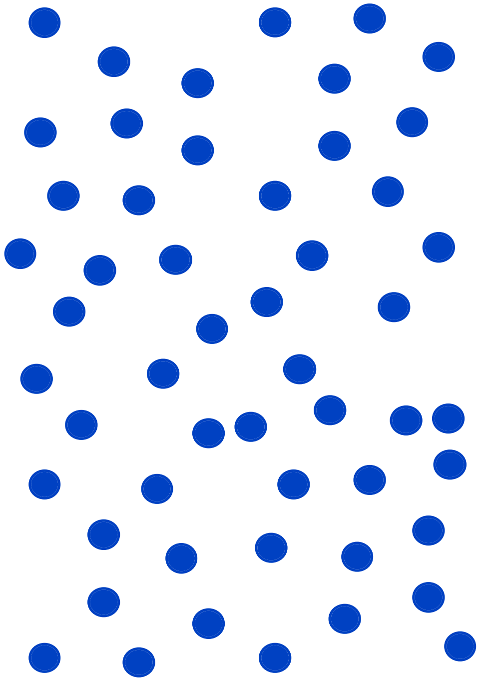
Oxford University

Artur Ekert

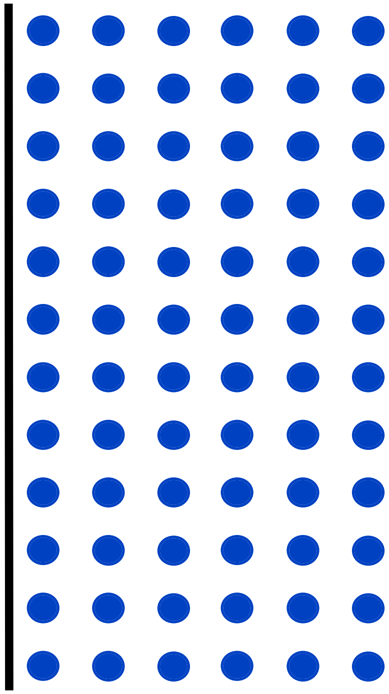
Key to Using Self-Assembled Islands

Forming and Positioning Islands

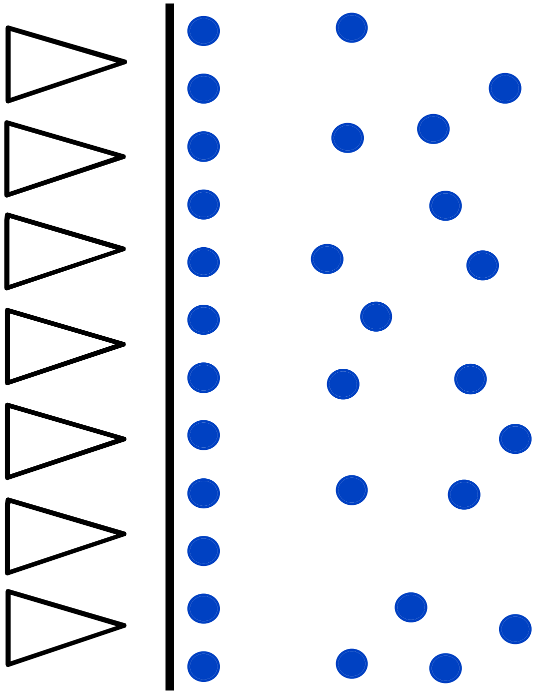
Uniform Size
(Randomly Arranged)



Ordered



Aligned



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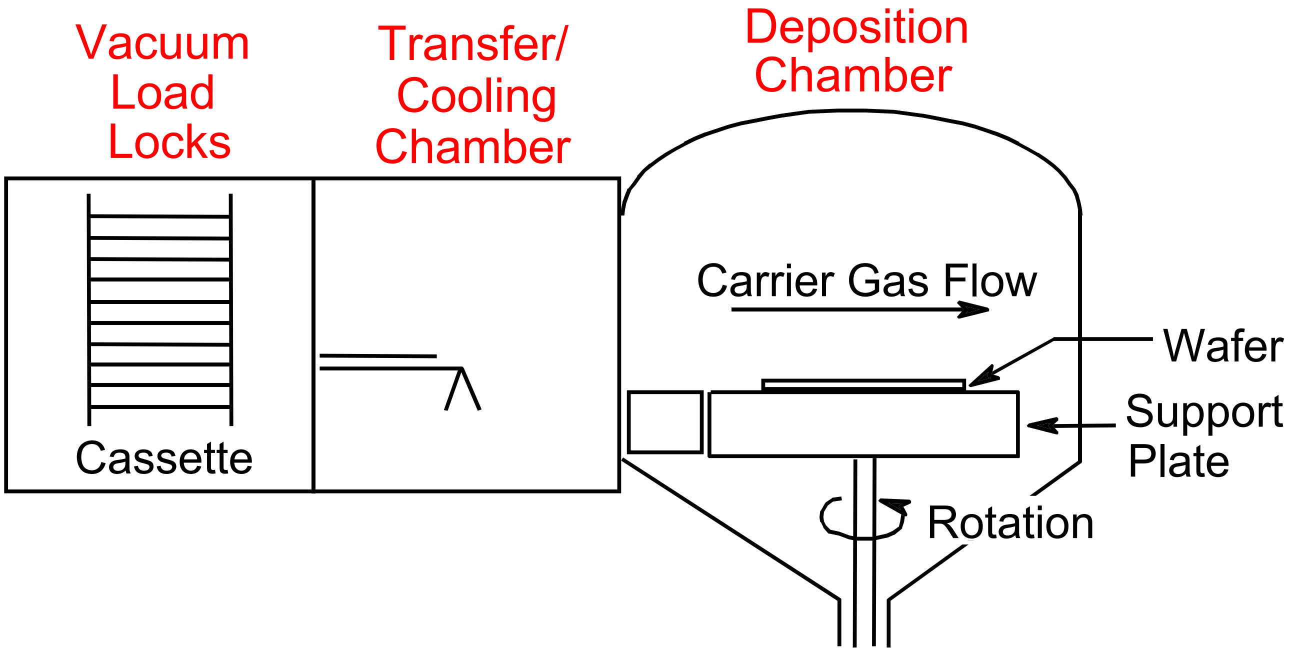


Cluster/multichamber system

RP wafer transfer

Cooldown chamber

Chamber volume: 11 liters

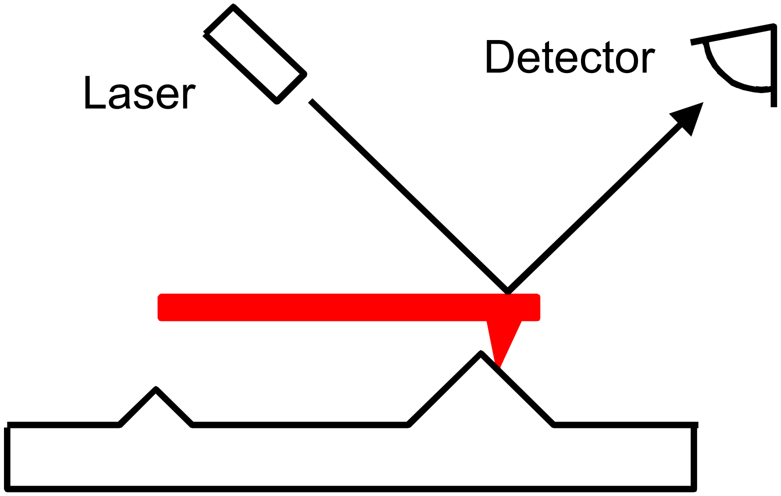
P ~ 1 - 600 Torr (10 Torr)

T ~ 550 - 1200°C (600°C)

Layers deposited in two different single-wafer CVD reactors
(and also by PVD)

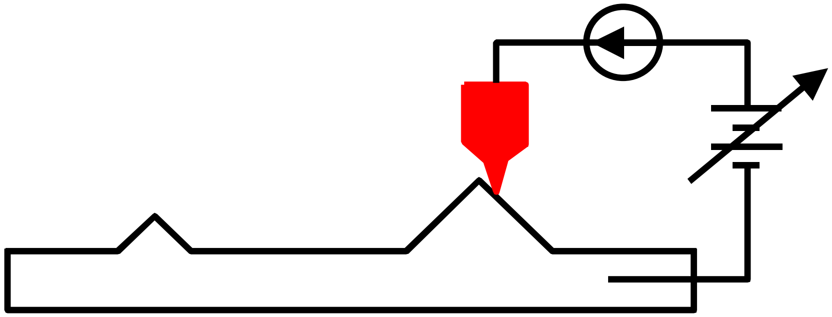
Scanning-Probe Microscopy

Atomic-Force Microscope (AFM)



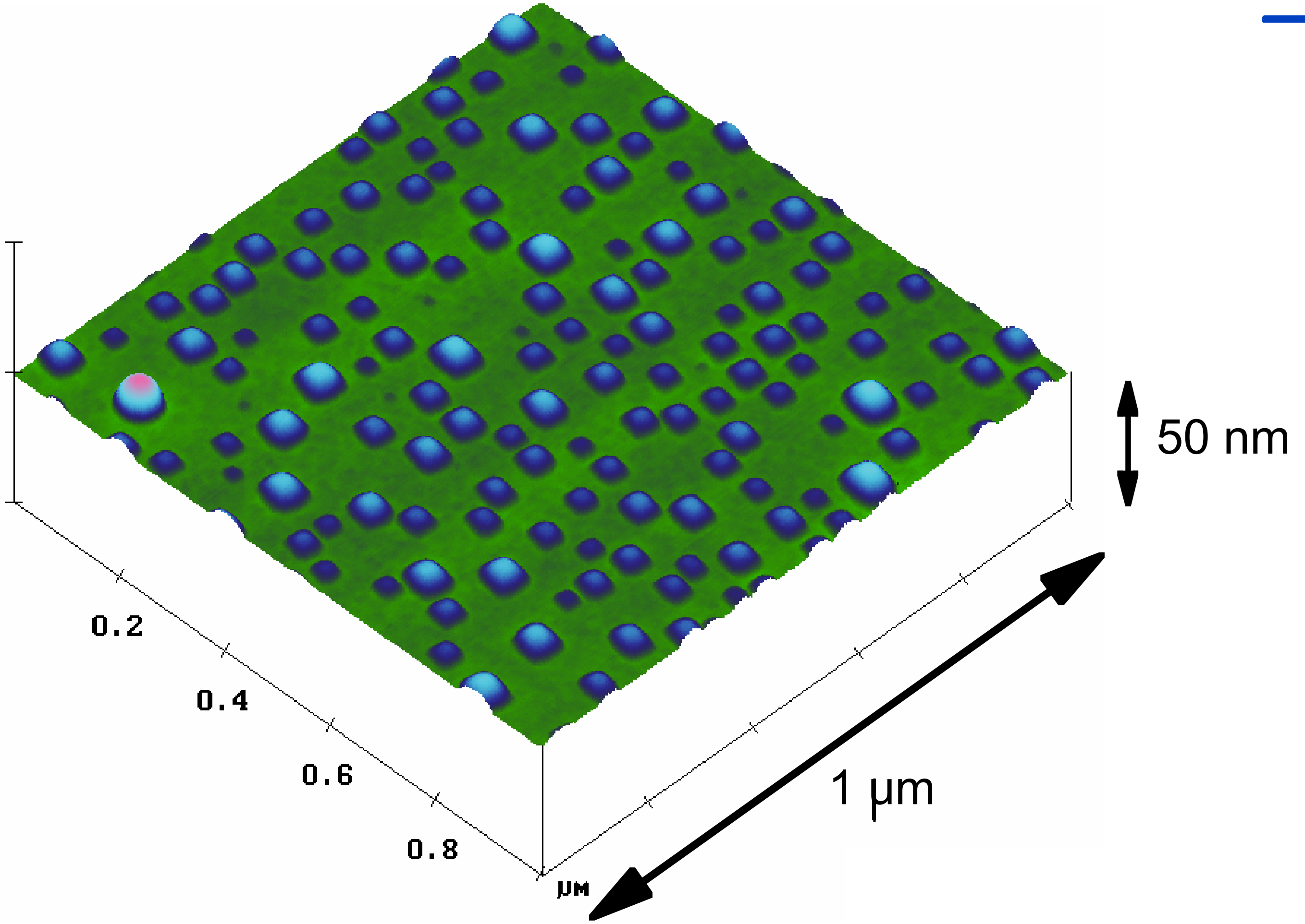
CVD and *ex situ* characterization

Scanning-Tunneling Microscope (STM)

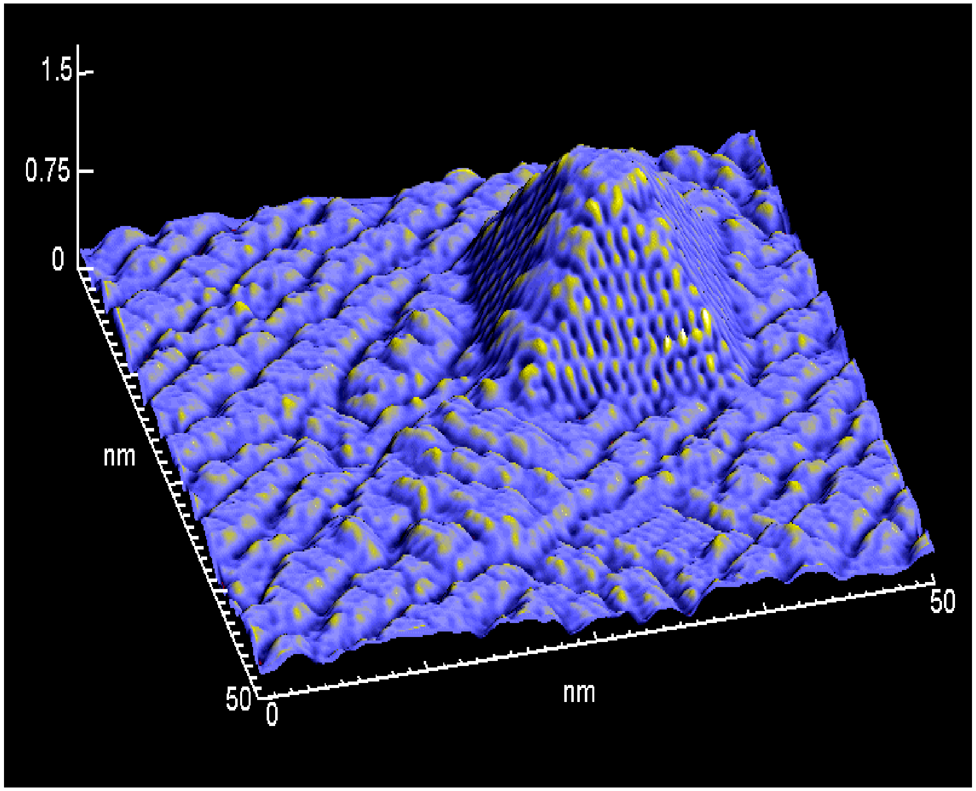


PVD and *in situ* characterization

Ge/Si(001): 6 eq-ML at 600°C

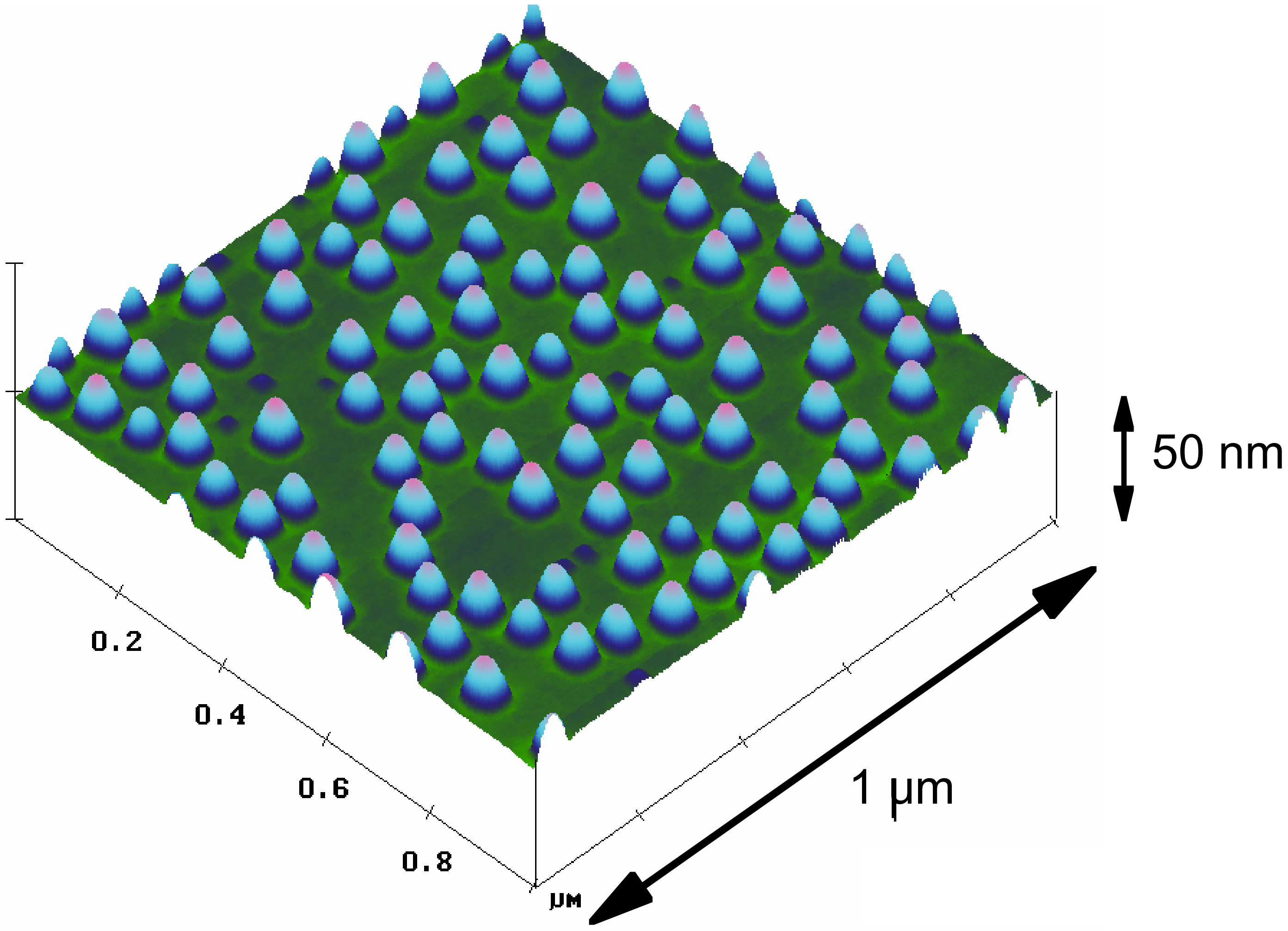


Very Small Ge Pyramid



Scanning Tunneling Micrograph by G. Medeiros-Ribeiro, HPL

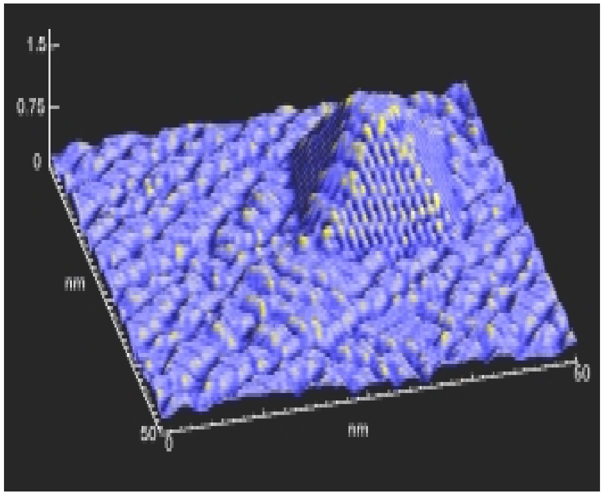
Ge/Si(001): 11 eq-ML at 600°C Domes



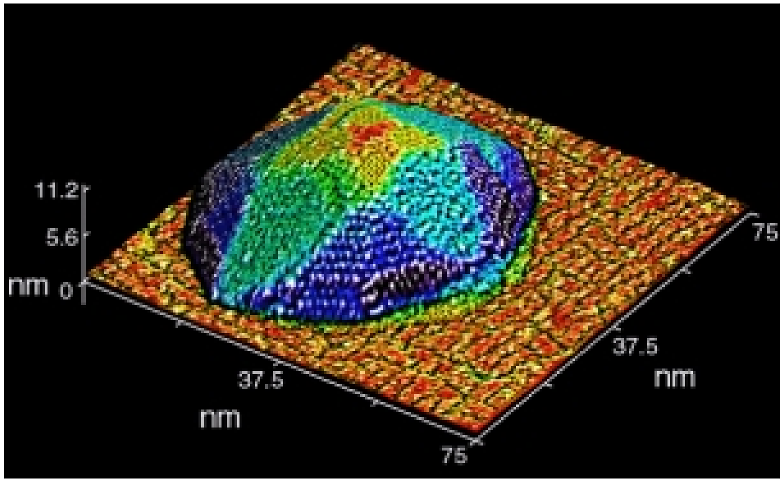
Self-Assembled Nanostructures

Strain from lattice mismatch forms 3D structure

Small Ge “pyramid”
on Si(001)



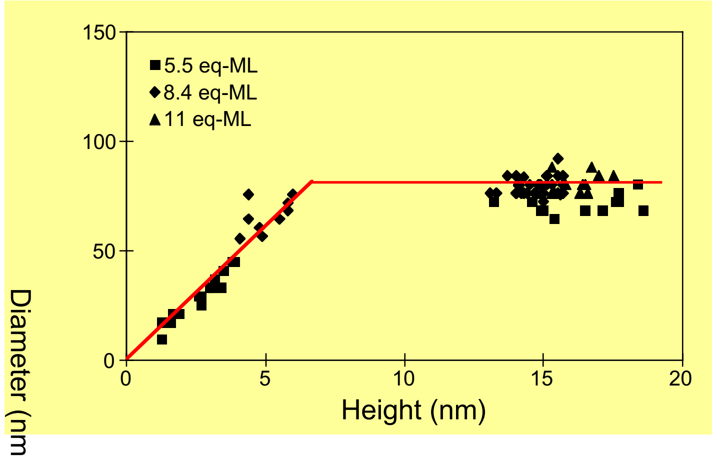
Larger Ge “dome”:
on Si(001)



Scanning-tunneling micrographs

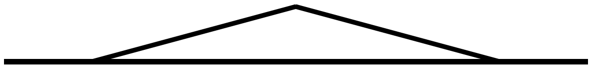
Gio Medeiros-Ribeiro, HPL

Island Distribution



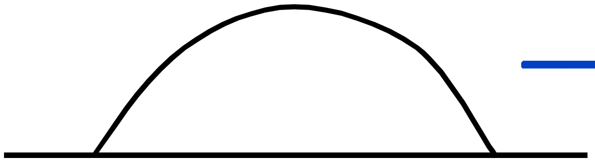
Domes have favored size
Pyramids do not

Pyramids



Bounded by {105} facets only
Proportional:
- Surface area
- Interface area
- Edge length

Domes

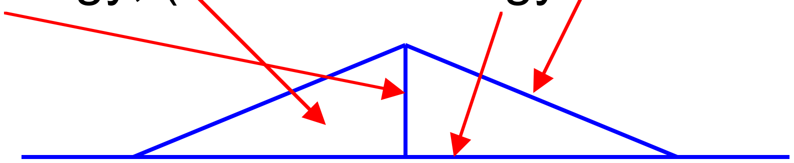


Bounded by several facets
- Area ratio can vary

Need not be proportional:
- Surface area
- Interface area
- Edge length

Can vary to minimize energy
Harder to add atoms beyond
this energy minimum
Strain relaxation near top of island

Minimize Energy

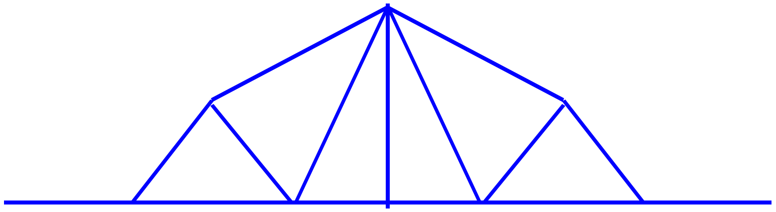


Volume strain energy, facet surface energy, edge energy, (interface energy - surface energy)

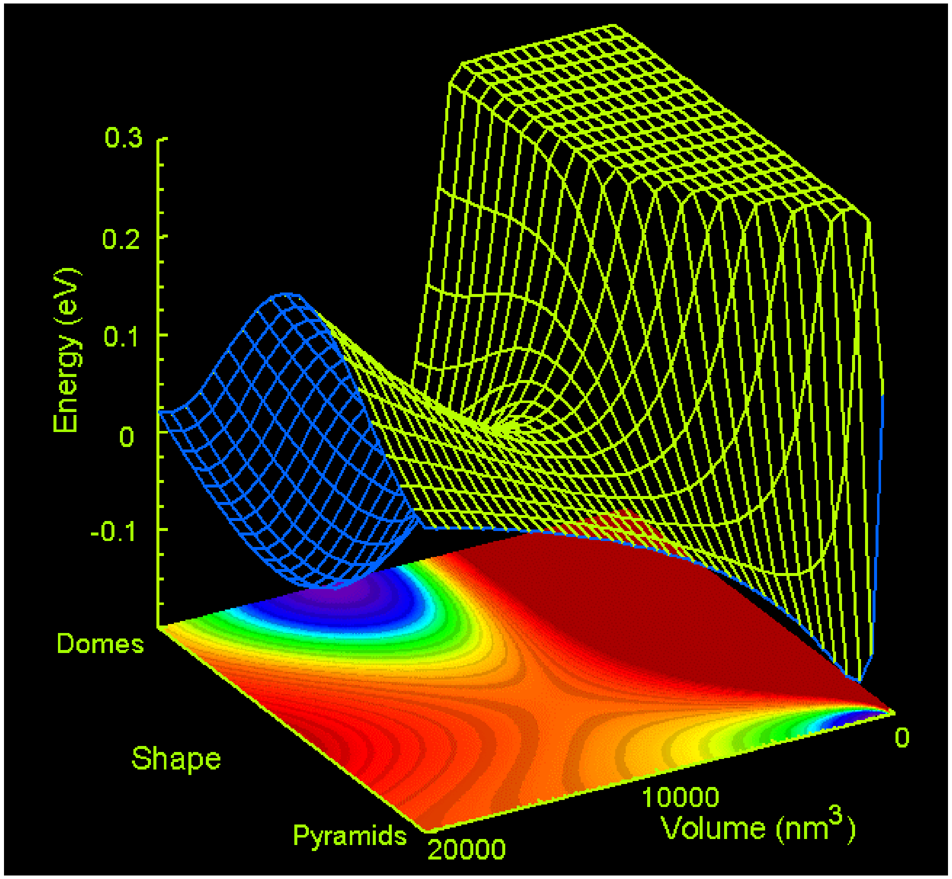
$$\Delta E(n) = C\,n + B\,n^{2/3} + A\,n^{1/3}\ln(a_c/n^{1/3})$$

C (C< 0): volume strain energy
B (B<>0): facet and interface energies
A (A> 0): edge energies

$$\Delta E(n)/n = C + B\,n^{-1/3} + A\,n^{-2/3}\ln(a_c/n^{1/3})$$



Shape Determined by Energy Minimization



Manipulating Islands

How to get
- Uniform size distribution?
- Smaller islands?

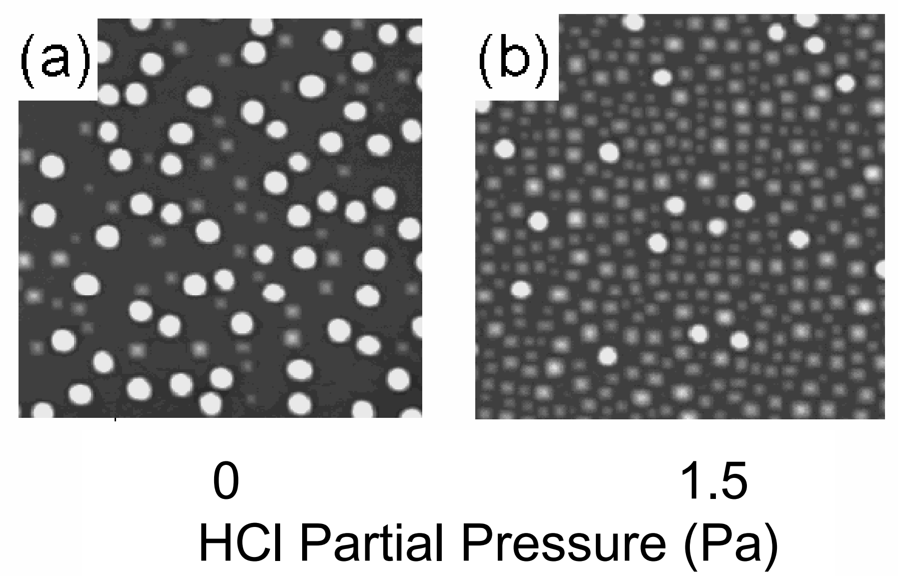
Domes have narrower distribution
Potentially more useful

How to get smaller domes?
Change kinetics or thermodynamics

- Add HCl during deposition:
  Primarily changes kinetics
- Etch with HCl after deposition
  Reduces island height, not base
- Use Ti ($TiSi_x$)
  Larger lattice mismatch

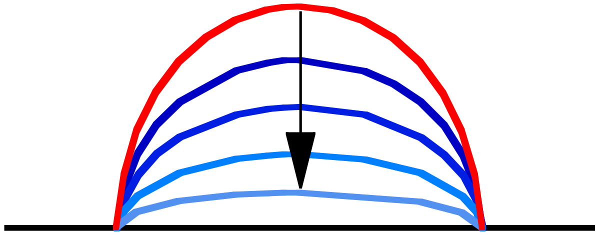
Using HCl to Control Islands

Adding HCl during Deposition



Adsorbed Cl impedes Ge surface diffusion

Etching with Gaseous HCl after Deposition



Shorter, but not narrower

Manipulating Islands

How to get smaller domes?
Change thermodynamics

Island shape determined by
- Volume energy
- Surface energy
- Interface energy
- Edge and corner energies

Add something that binds well to surface, changes surface energy (and perhaps ratio of energies of different surfaces)

Phosphorus or arsenic
n-type dopants
Initiation of arsenic incorporation slow
Little in thin layer
Phosphorus more useful as dopant

Doped Ge islands

$GeH_4 + PH_3 + H_2$

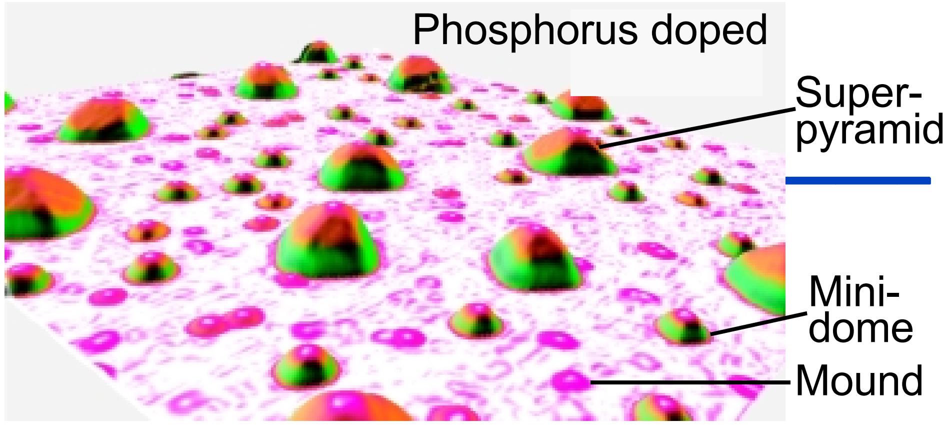
Temperature: 600°C

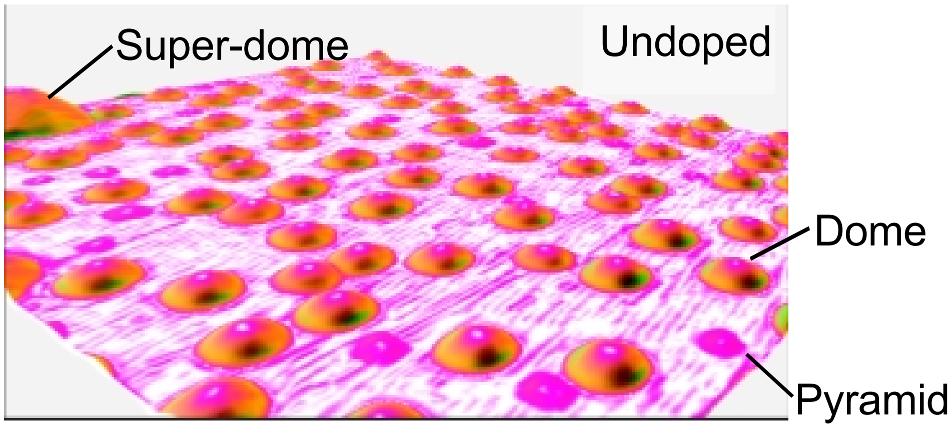
Partial pressures:

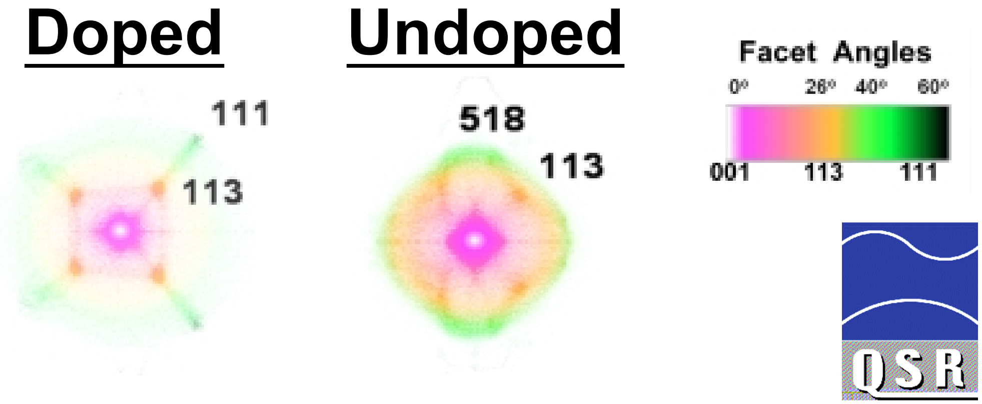
GeH_4: 3-6×10^{-2} Pa (2.5-5×10^{-4} Torr)

PH_3: 1.7×10^{-3} Pa (1.4×10^{-5} Torr)

H_2: 1.3 kPa (10 Torr)







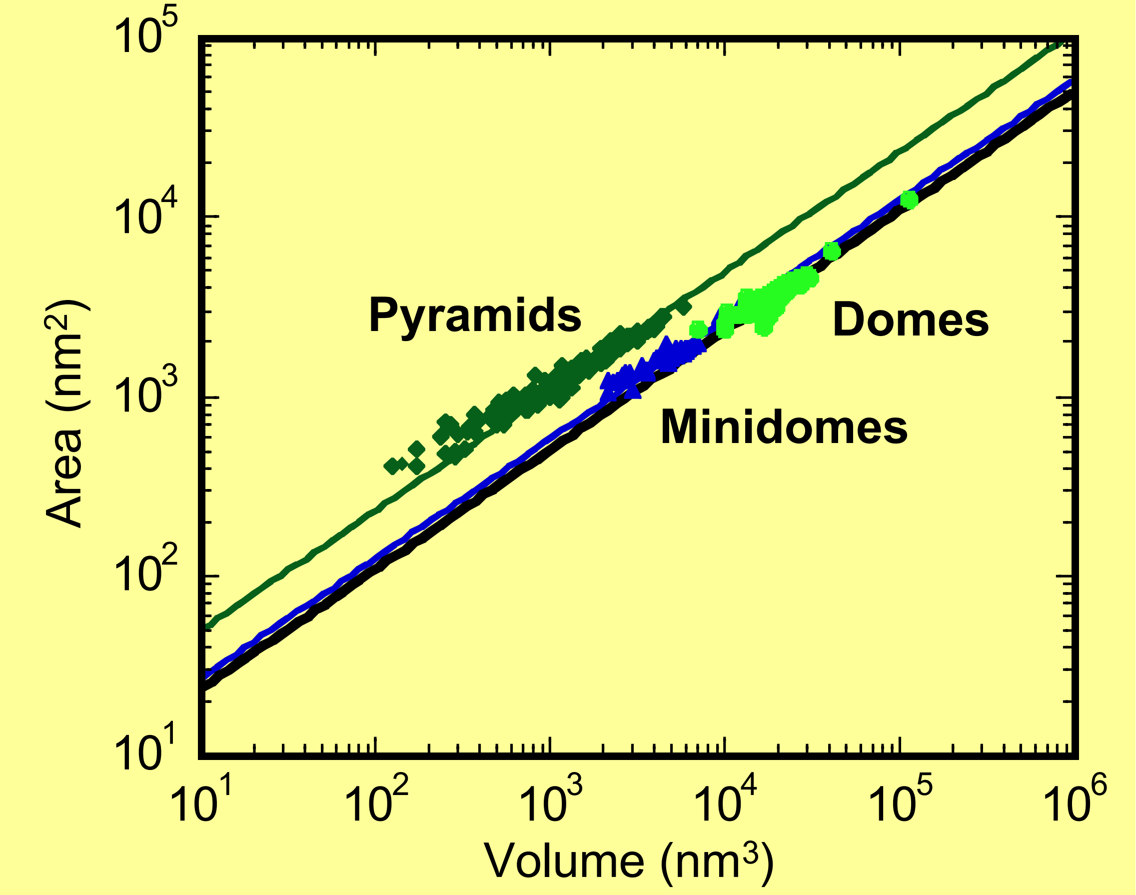
Island Shape Analysis

Undoped: Pyramids and Domes

Doped: Mini-domes

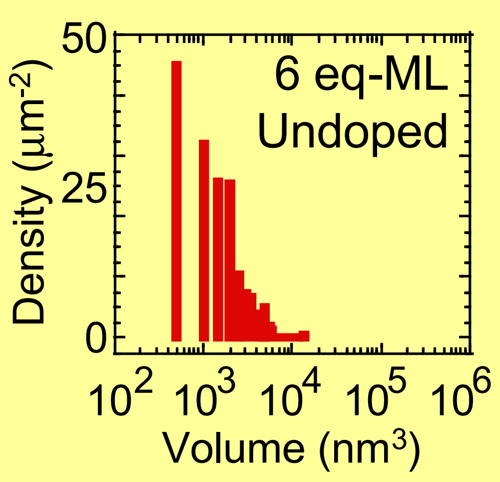
Points of one shape lie on line with slope = 2/3

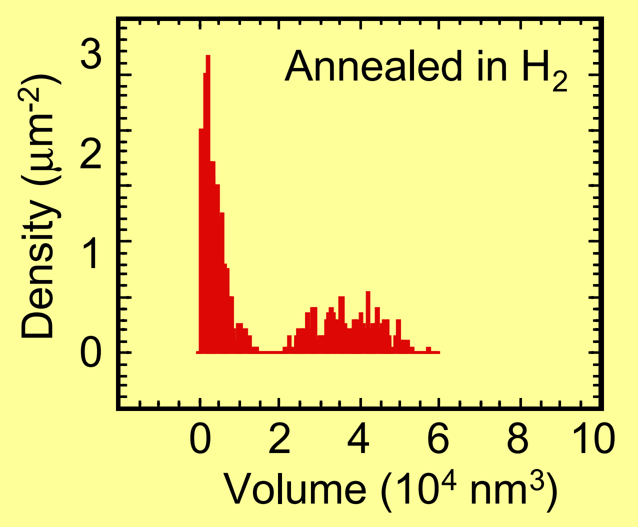
Intercept different for different shapes

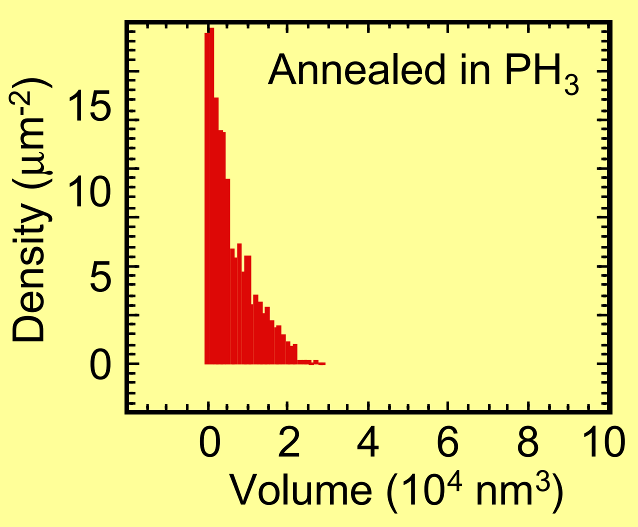


Phosphorus Also Changes Annealing Kinetics

6 eq-ML undoped Ge
Mainly pyramids







Effect of annealing

H_2: Islands coarsen - many convert to domes

PH_3: Coarsening retarded

Phosphorus-Doped Ge Islands

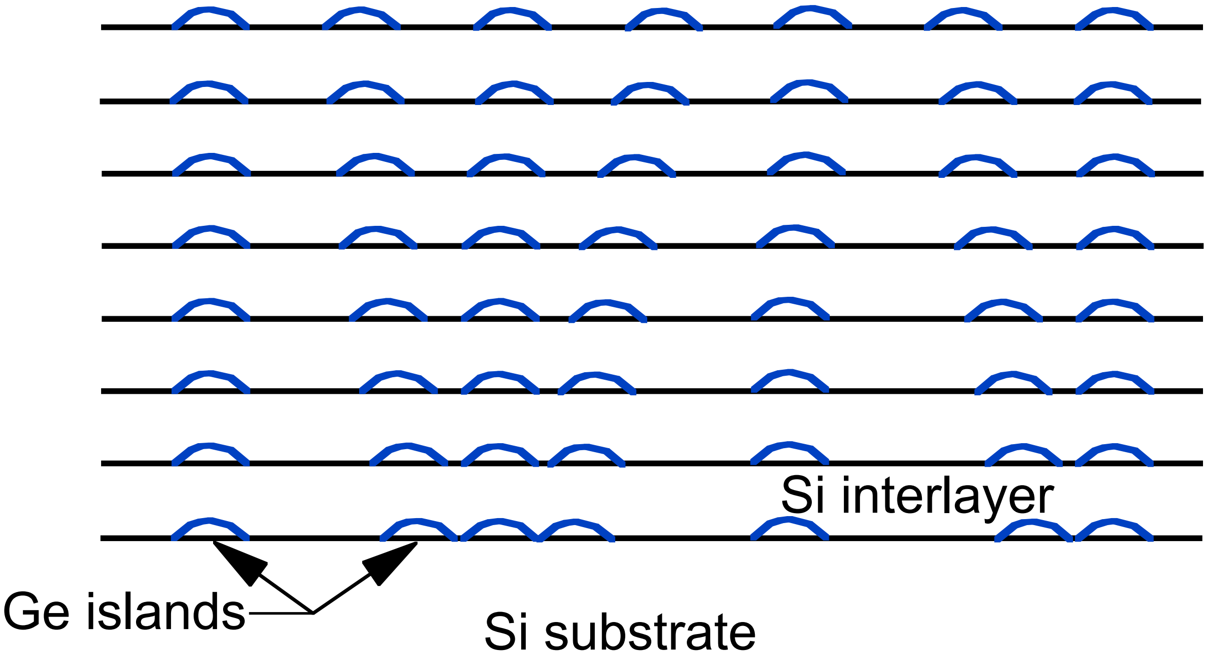
- Island shape influenced by surface energy
- Phosphorus…
    - Modifies energies and relative energies of different surface planes
    - Changes favored island shape
    - Retards coarsening
- Additional method for controlling island size, shape, and uniformity
- Slow buildup of high surface phosphorus concentration over 10s of monolayers

Manipulating Islands

Ordering and aligning

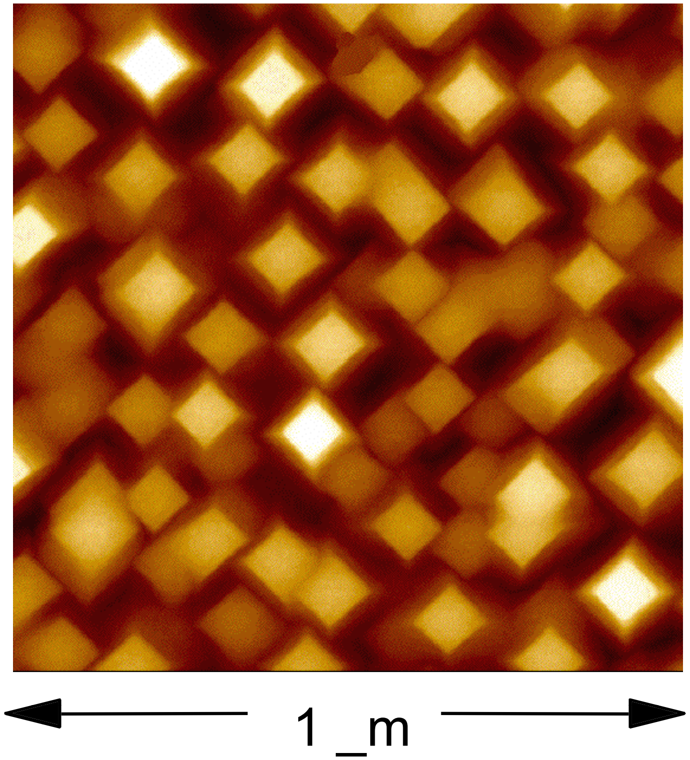
Ordering in Successive Layers

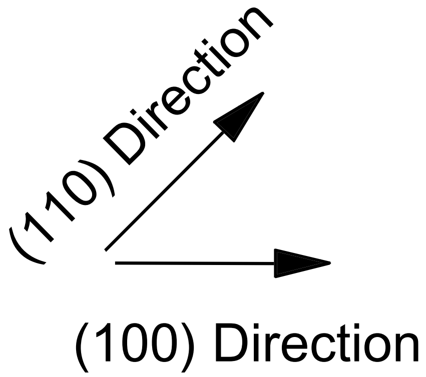
Cross Section



10 Layers of Si/Ge (Pyramids)
Nano Picasso

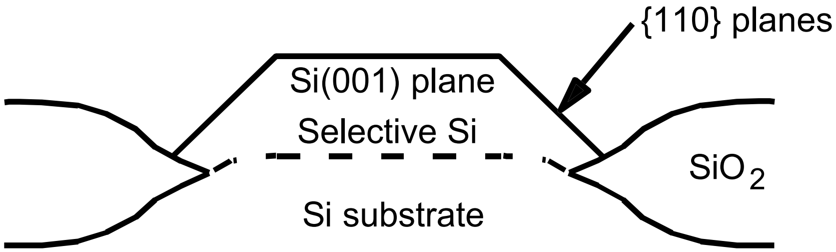
Top View





Height scale: 20 nm

Positioning Islands: Self-Assembled Ge Islands on Patterned Si substrate



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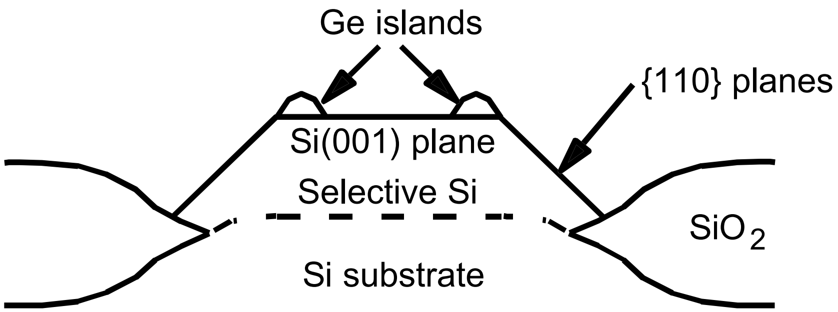
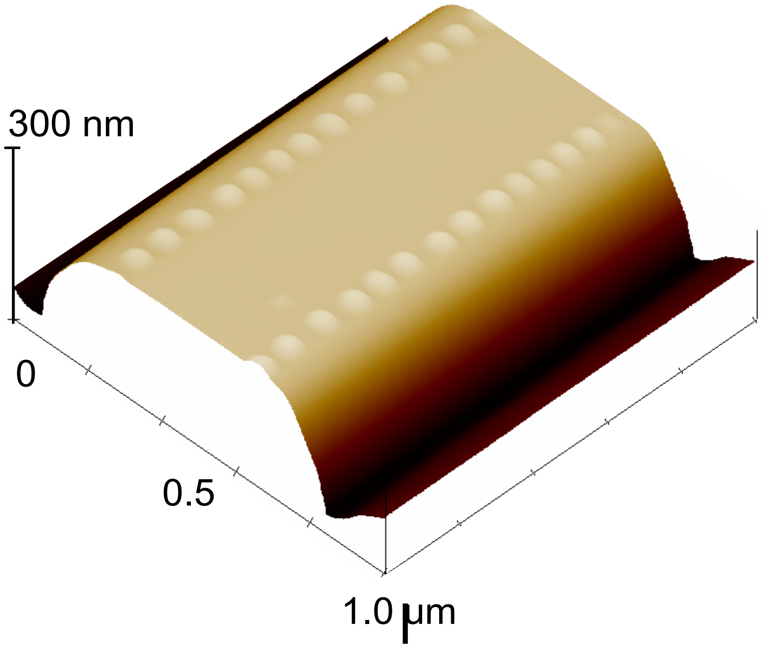
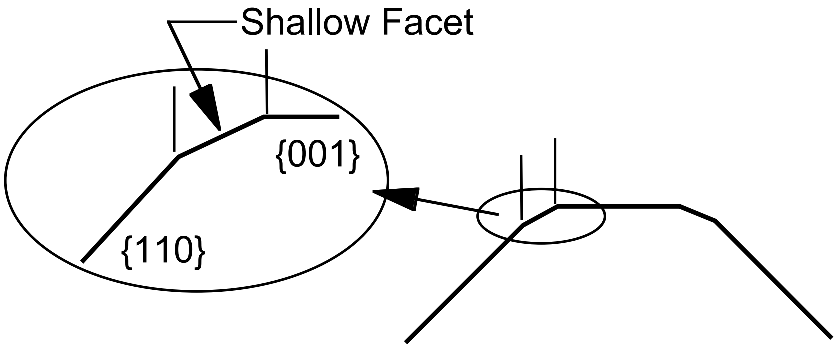




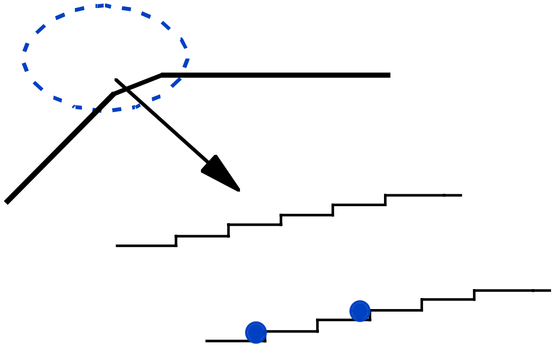
T.I. Kamins and R. Stanley Williams,
Appl. Phys. Lett. **71**, 1201 (1997)

What Causes Alignment?

Shallow facet



Facet provides steps for Ge nucleation



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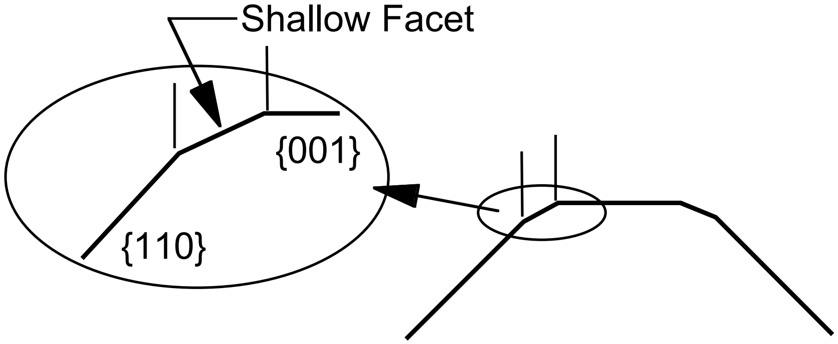

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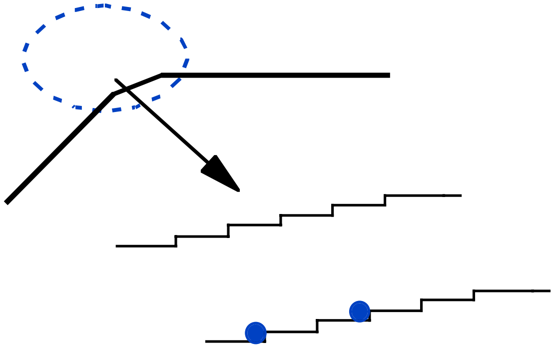
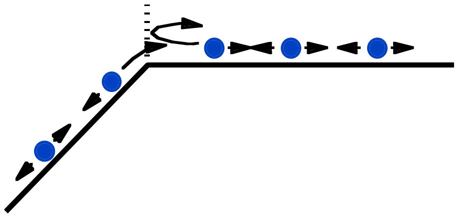


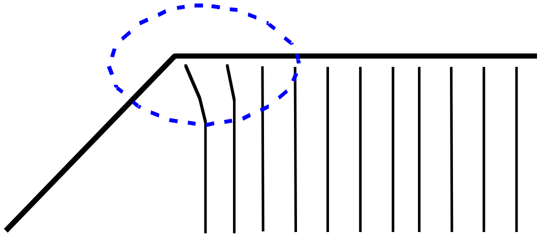
Surface Diffusion?

Anisotropic diffusion causes
Ge accumulation near edge

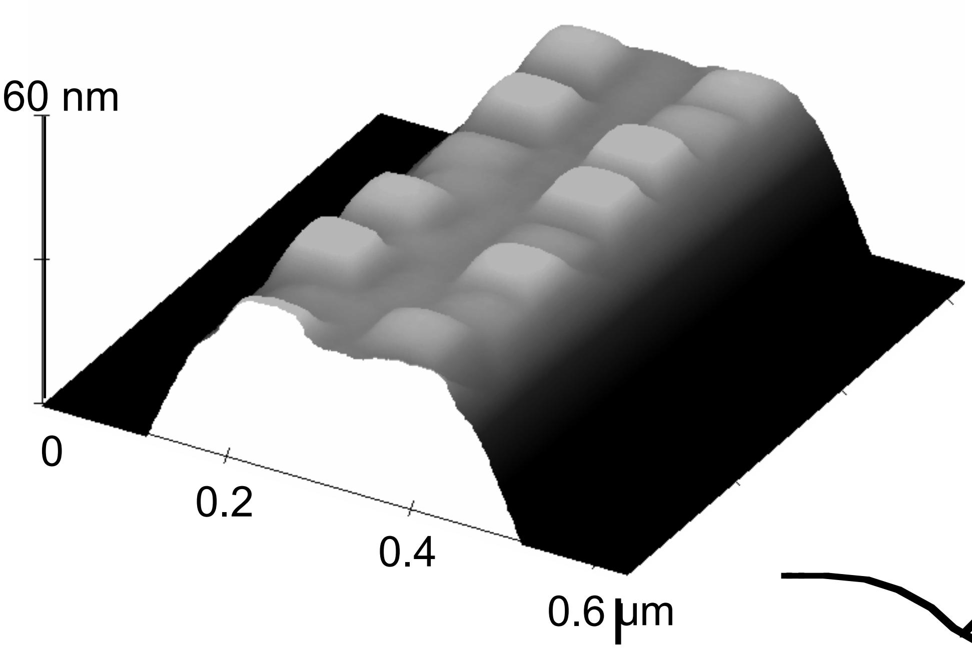


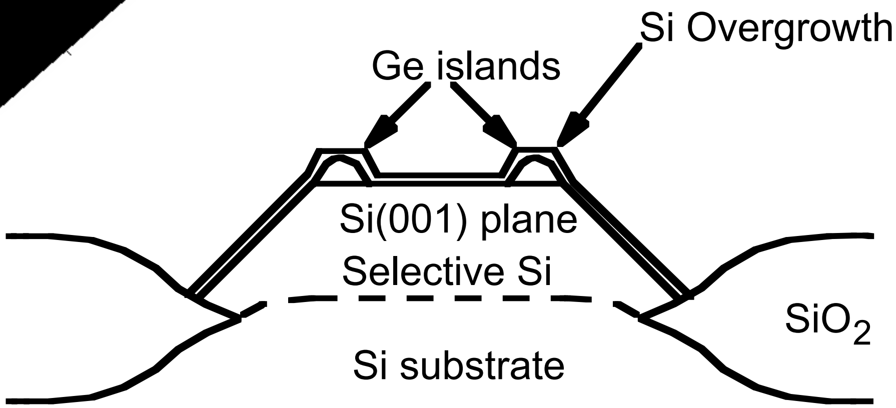
Strain?

Ge stretches Si lattice near edges
Relieves stress
Lowers energy barrier for nucleation



Si-Capped Ge Islands on Patterned Si Substrate





In-plane orientation of Ge islands and Si cap are different: Ge || [100], Si || [110] directions

Anisotropic Stress

Ge on Si:

Lattice mismatch same in x and y directions

⇒ equi-axed islands

Different lattice mismatch in different directions

⇒ anisotropic islands (ie, “wires”)

Anisotropic lattice mismatch:

ErSi2 [0001] || Si<110>: +6.5%

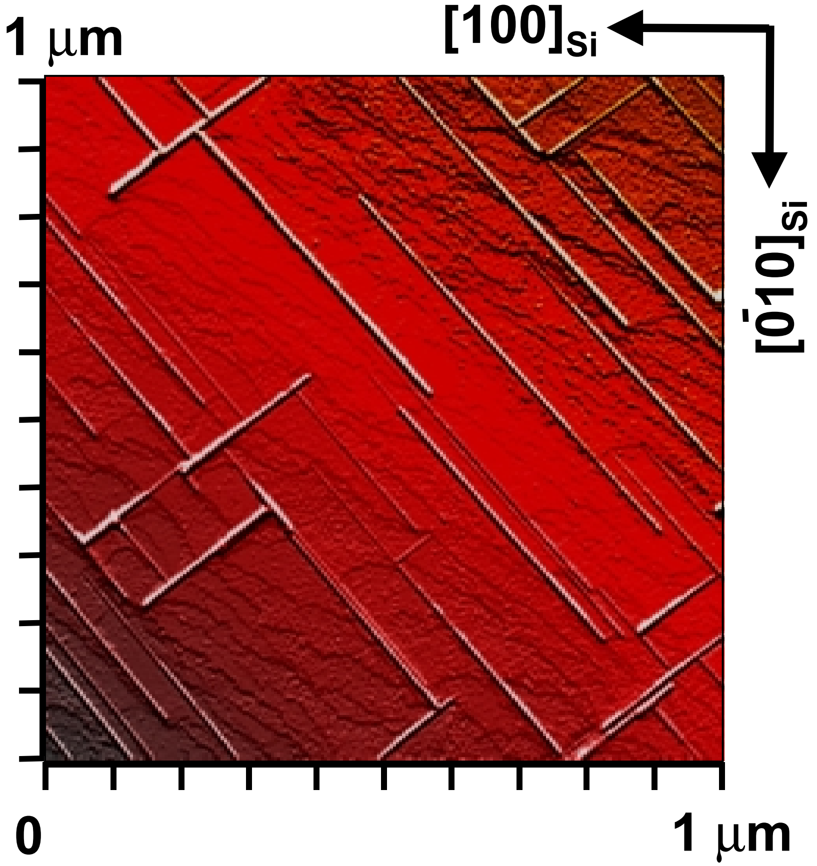
ErSi2 $[11\bar{2}0]$ || Si<110>: -1.3%

Constraint on growth in one direction

Elongated (wire) growth in perpendicular direction

Y. Chen, D. A. A. Ohlberg, G. Medeiros-Ribero,
Y. A. Chang, and R. Stanley Williams,
Applied Physics Letters **76**, 4004 (26 June 2000)

ErSi$_2$ on Si



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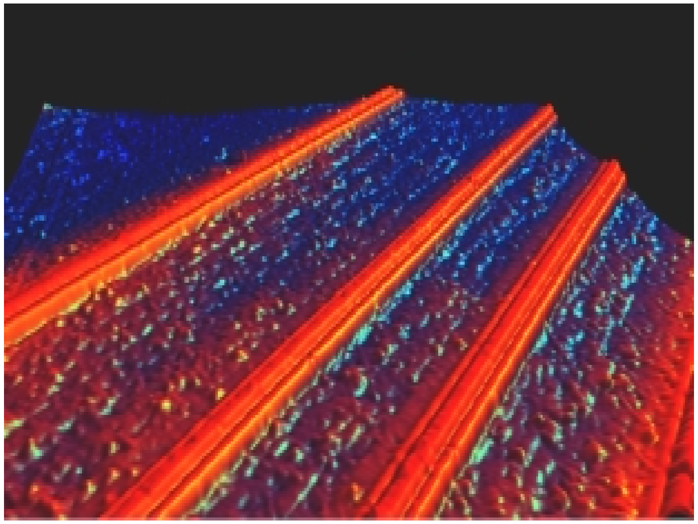
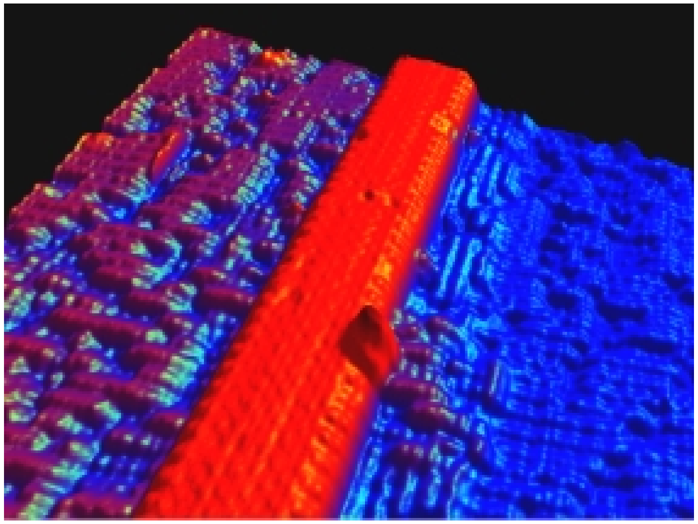
Self-Assembled Nanostructures

Anisotropic lattice strain forms 1D structure

$ErSi_2$ "wires" on Si(001)





Scanning tunneling micrographs

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Defect Tolerance

Self-assembled, self-ordered system will not be perfect
- Several percent defects

How to live with less-than-perfect parts in a system?
- Structurally simple architecture (*eg,* crossbar array)
  - Parallel straight wires
- Map defects
- Configure around defects
- (Can also be applied to conventional fabrication to reduce costs)

Normal computer:
- Design (configure), build, test

Defect-tolerant computer:
- Build, test (to locate defects), configure around defects

Summary

- Limits of scaling
  - Alternative devices
- Self-assembled nanostructures
  - Forming small structures
    - Putting them where we want them
  - **Strain from lattice mismatch**
    - **Zero-dimensional islands: Ge**, Ti
    - One-dimensional wires: $ErSi_2$
  - Catalytic wire growth
    - Ti-catalyzed Si nanowire growth
  - Patterned substrate to position features
- Defect-tolerant architecture