# HEWLETT-PACKARD JOURNAL

# A Low-Cost, Microprocessor-Based, 100-MHz Universal Counter

*A special integrated-circuit counter chip works with the microprocessor to give this reciprocal-taking counter a range of capabilities formerly found only at a much higher price. Flexible input amplifiers, a novel battery pack, and low radiated emissions are other features.*

**by Lewis W. Masters, Karl M. Blankenship, and Michael J. Ward**

MICROPROCESSORS AND LARGE-SCALE integration (LSI) have become powerful and indispensable tools for the designer of measurement instruments, allowing as they do a reoptimization of the conflicting goals of performance, features, and cost. Until now, these tools have made maximum impact at opposite ends of the instrument cost spectrum. Microprocessors have improved performance in high-end instruments ranging from voltmeters to spectrum analyzers, and LSI technology has provided simple multimeters and frequency counters at very low cost.

In HP's new 5315A/B Universal Counter, these two design tools have been combined to advance the state of the art in the middle range of counters by providing improved performance, more features, and reduced complexity at a much lower price than previous generations. Three ICs are critical to the performance of the 5315A/B: a commercial single-chip microcomputer, an integrated display driver chip, and most important, an HP-made custom LSI chip containing all of the data-acquisition functions needed by a universal counter. The implementation of this last IC, which we call the multiple-register counter, or MRC, is described in the article on page 12.

The 5315A/B is a moderately priced universal counter that accepts signals from dc to 100 MHz on both input channels. Its basic time interval resolution is 100 nanoseconds, but this may be improved on repetitive signals to less than a nanosecond through the use of averaging. The 5315A (Fig. 1) comes in a rugged plastic case that is suitable for bench use and can be equipped with an optional internal battery pack for portable and field applications. The 5315B is the same instrument housed in a standard HP metal package. The 5315B is useful for system applications or where superior EMI (electromagnetic interference) performance is required. Either instrument may be ordered with a temperature-compensated oscillator for applications where higher accuracy is necessary.

### A Computing Counter

The primary feature distinguishing the 5315A/B from earlier moderately priced counters is that it is a computing or reciprocal frequency counter. Simply put, the 5315A/B measures the period of the input signal and computes the corresponding frequency (frequency = 1/period) for display. This may seem


**Cover:** *Model 5315A Universal Counter is surrounded by microphotographs of the MRC (multiple-register counter) chip, a state-of-the art HP-developed bipolar integrated circuit designed to perform most universal counter functions under microprocessor control. The MRC is one of three major ICs in the 5315A.*

## In this Issue:



Printed in U.S.A.


**Fig. 1.** *Model 5315A Universal Counter measures frequency to 100 MHz and time intervals with 100-ns resolution. A reciprocal-taking two-channel instrument with a seven-digit display, it offers mid-range counter performance at a cost much lower than previous-generation counters. Shown here is the 5315A. The 5315B, the same instrument in a half-rack-width metal cabinet, offers exceptionally low radiated emissions.*

like unnecessary complexity, since a conventional direct-gating counter provides high resolution at communications frequencies. However, the conventional counter is restricted to 1-Hz resolution per second of gate time, so at low frequencies, it often provides unacceptable results. For example, it would take a 100-second gate time for a direct counter to provide a one-part-per-million accuracy check on a 32-kHz watch crystal. The high resolution of the computing technique enables the 5315A/B to display at least seven digits of answer per second of gate time, independent of the input frequency. Therefore, it would take only 0.1 second to measure 32 kHz, or for that matter 32 Hz, to one part per million.

### Universal Measurement Capability

Besides high-resolution frequency measurements, the 5315A/B can make many other kinds of single and dual-channel measurements. The period measurement capability of the counter is virtually identical to the frequency capability, since the only difference between the two is how they are displayed. Three types of two-channel time measurement functions are offered: time interval, time interval average, and time interval with delay. All three functions provide time measurement from an event at the A input to an event at the B input and provide at least 100-ns resolution. Time interval average allows greatly increased measurement resolution on many repetitive signals. Time interval with delay allows the user to vary the time between the start event and the time when the stop channel is enabled. This feature allows time measurements to be made on noisy signals or where signal anomalies prevent the standard function from operating properly (Fig. 2).

In the ratio mode, the ratio of the frequency in channel A to the frequency in channel B is displayed. Two types of totalizing functions are provided, one manually controlled by the operator and the other

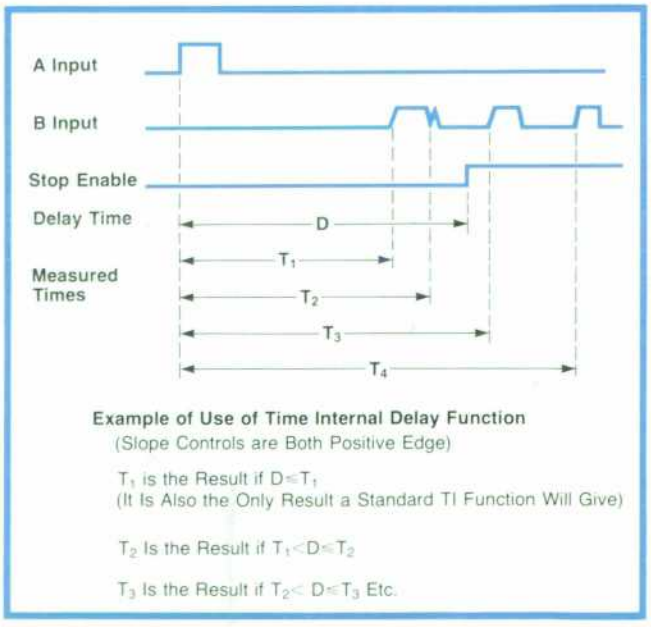



**Fig. 2.** *Time interval with delay is useful on noisy signals or signals with anomalies.*

controlled by electrical events applied to the second input. Several auxiliary functions are available, including the traditional counter check function, a display verification function, and a way to measure the gate and delay times. A position on the function selector (FREQ C) has been reserved for a frequency extention option to be introduced soon.

### Display Features

A number of steps were taken to enhance the readability of the display. First, yellow LEDs were selected because they are highly readable and easy on the eye. Second, the result is displayed in engineering format, with eight digits reserved for the mantissa and one for the exponent. Engineering format eliminates the confusing array of annunciators usually found on counters and replaces them with exponents of 0, ±3, ±6 and ±9.

The most-significant digit is always placed in the leftmost LED so that the operator knows where to look. Similarly, the decimal point may appear in only the three leftmost digits, eliminating correct but confusing displays such as 32128 kHz.

Most measurement functions will not produce a display overflow; only the eight most-significant digits are shown. Totalize and frequency, however, may contain useful data in the least-significant digits, so when more than eight digits of result are available, the most significant digits are overflowed. For instance, without overflow, the 5315A/B would be limited to 10-Hz resolution at 100 MHz, but with it, 0.1-Hz resolution is available.

The display area also contains annunciator LEDs for the optional battery pack and an error LED that turns on if the microcomputer finds an internal error during its start-up check.

### Continuously Variable Gate Time

The 5315A/B is the first counter to offer a continuously variable measurement time control. This feature is possible because a computing counter is not constrained to a fixed number of input events, such as 100, to yield a correct display. The microcomputer solves the equation: Frequency = (number of periods, N) ÷ (total time, T, for N periods). N and T can be any number greater than 1 and less than $10^{12}$.

The front-panel gate-time knob varies the time constant of a resistor-capacitor timer that determines the time from the start of a measurement until the stop is enabled. The next input event terminates the measurement. The exact measurement time is not important so long as it is known precisely enough. The counter measures this time to an accuracy of 100 nanoseconds.

A continuously variable control is useful on a counter because it gives the user a quick way to optimize resolution and update rate. With short gate times the display is updated rapidly, making it possible to follow changing signals. Long gate times provide more digits in the result. When the approximate measurement time must be known, selection of the GATE TIME function will display the current setting. The gate-time control sets approximate measurement time in frequency, period, time interval average, check and ratio functions. In time interval measurements with delay, the control varies the holdoff time before the stop is enabled, and in standard time interval measurements acts as a sample rate control. When the knob is rotated to the HOLD position, the counter makes one measurement at minimum gate time and then halts. A new measurement may be initiated by pressing the reset button.

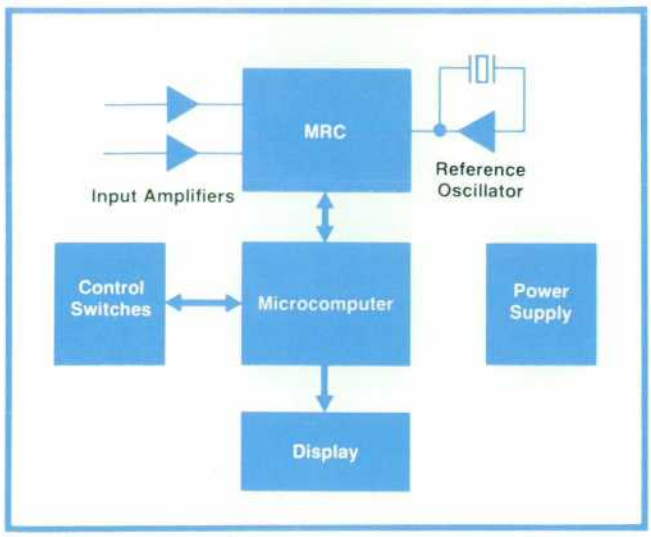



**Fig. 3.** *The 5315A/B block diagram is similar to that of a computer system. A commercial microcomputer controls a data acquisition block—a multiple-register counter chip—and the display.*

### Computer-Type Architecture

The block diagram of the 5315A/B should be quite familiar, since it is the same as that of a classical computer system (Fig. 3). There is a data-acquisition block (the MRC), a computation and control block (the microcomputer), and an output block (the display). LSI technology has reduced each of these three blocks to virtually a single IC. The MRC requires only a reference oscillator (time base) and a half-dozen components to do all the gating and counting required by a universal counter. The MRC was designed specifically as a microcomputer peripheral, so it interfaces directly, with a minimum of lines and no other components. The microcomputer, a 3870 with 2K bytes of on-board read-only memory (ROM), is likewise a model of simplicity, consisting of only a single IC and a few discrete components. At one stage

in the development of the 5315A/B, the display contained more components than any other block, but later an IC manufacturer was found who had the capability and desire to integrate a complete LED drive subsystem. The result, Intersil's ICM 7218A, is a microcomputer peripheral chip that requires no other components to drive eight standard-size LED digits. The simplicity of these three blocks is also mirrored in the rest of the 5315A/B. In all, only a dozen ICs were required to implement this counter, about 30% of the number required to build a predecessor of much lower capability.

The interaction of the various functional blocks to make a measurement is straightforward, with the microcomputer providing all instrument control via data, address, and command buses that use 16 of its general-purpose I/O ports. On power-up, the microcomputer goes through a brief check routine to verify its ROM, RAM, and I/O ports. It then checks to see that the MRC can make a simple measurement. If a fault is detected, a front-panel error LED is turned on and an error code displayed briefly. Next, the computer checks the front-panel pushbuttons to determine what function is selected. The appropriate setup data for that type of measurement is then sent to the MRC control register, an operation analogous to writing to a RAM (random-access memory). The microcomputer next resets the MRC's counting and gating circuits and enables the start of a measurement cycle.

From this point on, the computer has nothing to do until signaled by the MRC that service is needed. The MRC signals the computer whenever it has completed a measurement or one of the eight decade counter chains has overflowed. The computer can then access the MRC status register to determine the proper course of action. The computer must know when an overflow occurs because the counter chains are extended another four decades in the computer's memory. When the microcomputer detects the end of a measurement, it reads data from the two MRC counting registers, one BCD digit at a time.

Once the computer has the data, it processes it into a usable form, usually by dividing one 12-digit data word by the other. The result of this division, properly scaled, is usually the data that is displayed. First, however, the microcomputer manipulates the number to give a meaningful display. Even though the result of the division is a 12-digit number, very few measurements produce results with that resolution. Therefore, the number is usually truncated so that only statistically significant results are displayed. However, it is important to display as many digits as possible, so the truncation algorithm must be versatile and accurate. The microcomputer examines the original data from the MRC to determine which digits are significant, then shifts and manipulates the data so that it is most useful to the user when output to the display subsystem. The computer sends data to the display driver IC in much the same way that it would to a RAM. Once the data is in the display, the microcomputer is free to start a new measurement cycle.

### External Control

Although the microcomputer has a limited memory capacity, some memory was left over after the basic control and computation routines were completed, so a useful routine was written to fill the remaining program space. This routine allows a user, through an optional programmer box, to do mathematical manipulation of the data displayed by the counter. With this offset/normalize option, the counter can display the solution to the equation $x/m + b$, where x is the normal result and m and b are variables input by the user on thumbwheel switches. The data is input in scientific notation with eight digits plus sign for the mantissa and one digit plus sign for the exponent. When a negative answer is displayed, the leftmost LED digit becomes a minus sign, reducing display resolution to seven digits. Display range is from $999.\times10^{9}$ to less than $.1\times10^{-9}$. The offset/normalize option is useful in transducer measurement applications, where output is desired in such units as revolutions per minute or gallons per hour instead of events per second.

### Input Amplifiers

The input amplifier portion of the 5315A/B Counter takes the unknown signals, which can have a wide range of frequencies and amplitudes, and amplifies, conditions, and converts them into logic-level signals that can be counted by the MRC chip. The nominal sensitivity of the amplifiers is 10 mV from dc to 10 MHz, with a slow rolloff in frequency response above 10 MHz to a nominal sensitivity of 25 mV at 100 MHz. These specifications apply to both channels, A and B. The B-channel amplifier is matched to and is substantially identical to the A-channel amplifier, making possible such measurements as 90-MHz frequency ratios and time interval averaging to better than 5-ns accuracy.

Front-panel controls include ac/dc coupling and a $\times20$ attenuator for each channel, a 100-kHz low-pass filter on the A channel, a separate/common-A switch, individual slope select and trigger level controls, and a novel feature, a sensitivity control mode that is individually selectable for each channel. Trigger lights indicate whether the input signal is being captured by the counter, and in dc coupling, provide information about the relationship of the input signal level to the trigger level.

The amplifier is constructed and serviced as a sepa-

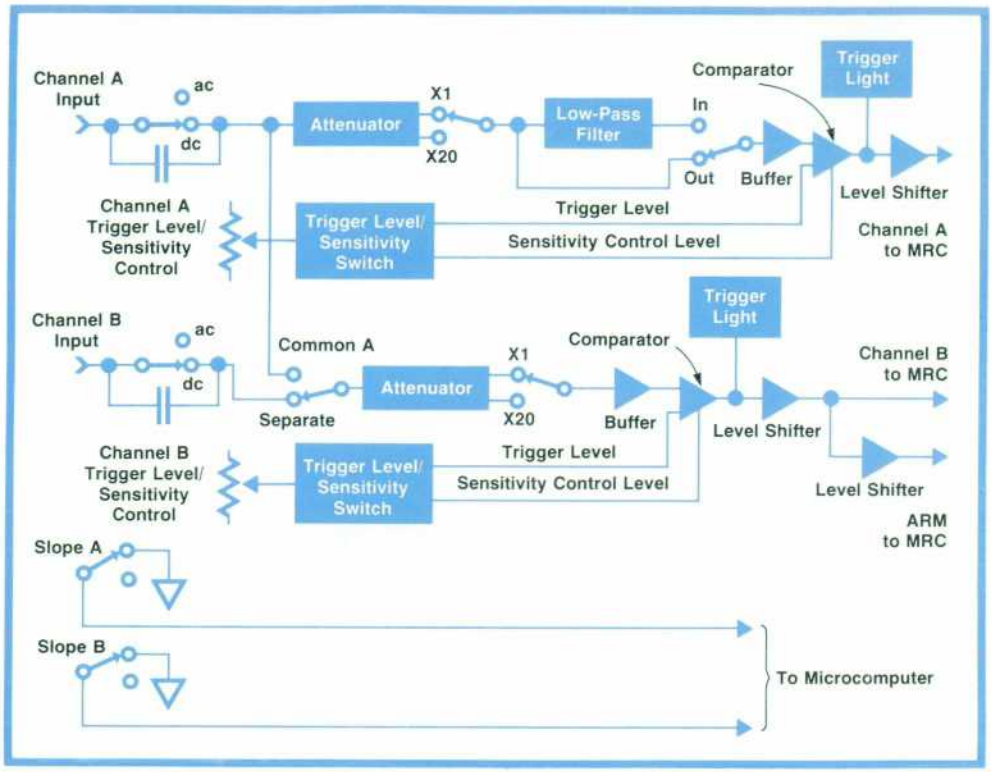



**Fig. 4.** *5315A/B input amplifier section.*

rate module. Amplifier modules are interchangeable: any amplifier will work with any 5315A/B main board. This feature improves flow in the manufacturing area and simplifies service.

The functional block diagram of the amplifier section of the 5315A/B (Fig. 4) is straightforward. A dual high-speed comparator provides most of the amplification. The dc trigger level is applied to the reference input of the comparator and the input signal is dc-coupled to the other input. The comparator output, at standard ECL levels, is shifted to the special levels required by the MRC.

The trigger level is controllable separately for each of the two channels. In trigger level mode, the trigger level potentiometer applies a variable voltage (+2 to −2 Vdc) to the reference input of the comparator. This voltage defines the threshold dc level at which the output of the comparator switches states.

### Sensitivity Mode

A new feature in this counter is the sensitivity mode of operation. This is selected by pushing the button next to the trigger level potentiometer. In this mode the trigger level presented to the comparator's reference input is set to ground potential, so that the comparator is now operating as a zero-crossing detector. The trigger level potentiometer does double duty, in this mode operating as a sensitivity control.

In sensitivity mode the trigger level potentiometer controls the value of the comparator's hysteresis and thereby controls the threshold switching voltages. This effectively controls the sensitivity of the amplifier; in this respect the potentiometer may be thought of as an amplifier gain control. When the trigger level control is fully clockwise, the sensitivity is maximum. Turning the knob counterclockwise increases the hysteresis and decreases the sensitivity. When the knob is turned fully counterclockwise, the amplifier is essentially turned off. In the trigger level mode, the sensitivity is automatically preset to maximum.

In general, the sensitivity mode works best for most frequency measurements and the trigger level mode for most time interval measurements. However, there are exceptions.

For low-frequency signals it is necessary to use dc coupling. In this case, the trigger level mode is generally used, even for frequency measurements. However, sine waves with no dc offset cause no trouble in dc-coupled sensitivity mode.

With signals larger than 100 mV rms and the counter in sensitivity mode, the sensitivity control may be set somewhat counterclockwise (reduced sensitivity) if it is suspected that the input signal has noise riding on it. This allows the input amplifier to ignore the smaller noise impulses while still triggering properly on the desired signal. This does not help, of course, if the noise amplitude is greater than that of the desired signal. In this case, if the input signal is below 100 kHz and the interfering noise is high-frequency, using the A-channel filter will help suppress the miscounts due to noise. In other cases it may

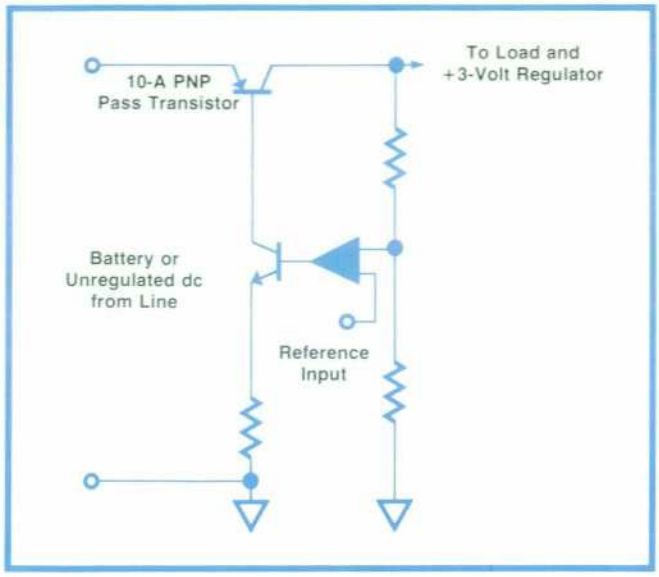



**Fig. 5.** *+5V regulator uses a PNP pass transistor instead of the usual NPN type. Dropout voltage is only 200 mV instead of the usual 2V, making it possible for the 6V battery pack to supply the +5V and +3V regulators directly, without dc-dc conversion.*

be necessary to filter the input signal before it is applied to the 5315A/B inputs.

In measurements of impulses or pulse trains, the trigger level mode is usually best. This mode allows the user to select where on the pulse waveform the counter will trigger, and to choose triggering above or below noise or ringing at edge transitions. Alternatively, the user may choose to trigger during the ringing, to characterize it. If very large signals are involved, the ×20 attenuator can be switched in.

### Power Supply

The 5315A can be operated either from the ac power line or from an optional 6-volt battery pack. The 5315B operates from the ac line only.

For ac line operation, 100/120/220/240 volts at 48-66 Hz is applied to the ac portion of the power system, consisting of transformer, rectifier bridge, and filter capacitors. This section produces the positive and negative unregulated dc voltages. The unregulated dc voltages are routed via the power switch to the regulator section of the circuit, which provides the +5V, +3V, and −5.2V supply voltages necessary to run the counter. All three regulators are adjustable.

The adjustability of the regulators has certain advantages in the production of a modular instrument such as the 5315A/B. Being able to set each voltage accurately allows the design of certain modules to be optimized with respect to the supply voltages. This means that the functional modules can be tested while separate from the mainframe, with a high level of confidence that subsequent mating of the modules with the mainframe will yield optimum performance without additional testing and adjustments.

The design of the +5V regulator makes it possible to use only a 6V battery in the battery pack, thereby reducing the size, weight and cost of the battery pack significantly compared to an 8V battery, the next available size. The +5V regulator is a discrete series regulator with an unusual feature. It employs a high-current PNP pass transistor instead of the usual NPN type (Fig. 5). This change offers significant advantages when operating from the battery pack, because it allows operation down to an input-output voltage differential (drop-out voltage) equal to the $V_{ce}$(sat) of the transistor, or less than 0.5V. By comparison, the dropout voltage of a typical three-terminal regulator is about 2V.

The $V_{ce}$(sat) of a transistor is minimized when the transistor is operated at a current level much lower than its rated capability. The transistor selected for the +5V regulator allows the circuit to regulate down to an input-output voltage differential of approximately 200 mV. This means that a 6V battery can be used to supply the +5V and +3V regulator chain directly and dc-dc conversion is necessary only to supply the negative supply voltage. Because most of the power in the instrument is on the +5V and +3V buses, the system is very efficient. In battery operation, the +5V regulator is over 75% efficient. Had a three-terminal regulator and an 8V battery been used, the efficiency would have been 15-20% lower.

### Battery Pack

The optional 5315A battery pack consists of the 6-volt rechargeable battery and the circuitry necessary to charge and discharge it. It also incorporates a dc-dc converter (inverter), which supplies the negative voltage for the mainframe during battery operation. The battery pack is designed to provide adequate power to run the instrument and yield optimum performance in applications ranging from standby operation to once-a-day cycling. Special attention is also given to maximizing battery life through features that minimize the effect of abusive use and provide useful information to the user.

The battery selected for the 5315A consists of three series-connected, 2V, five-ampere-hour Gates rechargeable sealed lead-acid cells. Lead-acid cells offer high cell voltage, low cost, long shelf life, and no discharge memory.

Current-limited constant-voltage charging and constant-current charging are two common techniques for charging lead-acid batteries. Neither of these techniques offered a solution to the charging requirements of the 5315A battery pack. To recharge a battery of this capacity in a time period suitable for once-a-day cycling using the current-limited constant-voltage technique requires either a very

# Lowest-Cost HP Universal Counter Developed Using LSI and Manufacturing Innovations

by Michael D. Wilson and David M. George

Recent advances in LSI technology have produced a universal counting IC with the oscillator circuit and display driver incorporated into the design. Previously, this much circuitry required one or more printed circuit boards, packed with small and medium-scale TTL integrated circuits.

This new IC, the Intersil ICM 7226A, is used in a new low-cost HP universal counter, Model 5314A (Fig. 1). The 5314A is a 100-MHz universal counter that measures frequency, period average, time interval, and ratio in conventional fashion. It also has totalize and check functions.

**Fig. 1.** *Model 5314A is a low-cost two-channel 100-MHz universal counter that measures frequency, period average, time interval and ratio.*

The 5314A is the lowest-priced universal counter manufactured by HP. To achieve a low price, the instrument and power supply (the only boards in the standard 5314A) are loaded and tested as a single printed circuit board (Fig. 2). The only adjustment required is the tuning of the 10-MHz reference oscillator, and this can be done from the front panel of the standard instrument. The front board and metal front panel are held in place by plastic inserts molded into the package, resulting in an instrument that is easy to assemble and requires no expensive hardware.

Low cost was achieved while retaining performance by designing both technically efficient circuits and an equally efficient manufacturing plan. The simple notion of building the complete instrument on a single printed circuit board has resulted in cost savings in every step of the manufacturing process. The single blank board is cheaper than two separate boards, the loading of parts is quicker, secondary operations are eliminated, and testing is simplified. In general, one part passing through the manufacturing system is more efficient than two smaller parts. Extra emphasis was placed on the physical board layout to minimize the possibility of misloading parts. With a low-cost instrument, one cannot afford to spend much time correcting errors. Therefore, many parts are automatically inserted under computer control. Both custom and standard resistor packs are used and special provisions made so they cannot be loaded incorrectly.

Since testing can be very time-consuming, it was essential

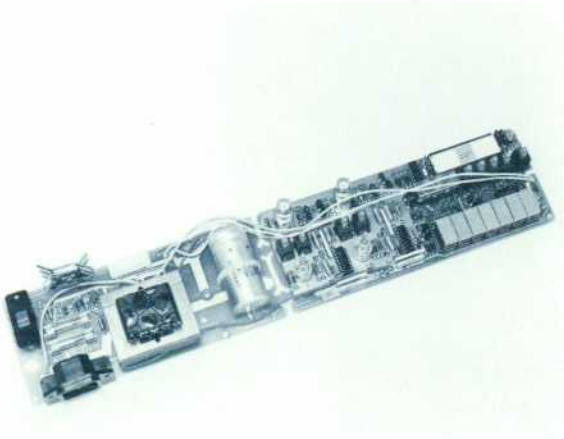


**Fig. 2.** *The only two boards in the 5314A are made, loaded, and tested as a single unit, thereby lowering manufacturing costs. The boards are separated before being installed in an instrument.*

that the 5314A take advantage of the most efficient testing methods available. The instrument is built on a single flat printed circuit board, making it possible to test it quickly with a vacuum fixture and an HP 3060A Board Test System. Accurate diagnostics for units that might have a problem eliminate tedious troubleshooting.

The 5314A uses yellow seven-segment LED displays instead of red. Yellow has better contrast at distances greater than eight feet, and unlike red, is visible to people with certain types of color blindness. Custom resistor packs were designed to obtain short electrical paths, significantly improving high-frequency performance while simultaneously lowering parts count. This helped to provide flat sensitivity of 25 mV to 100 MHz.

ECL line receivers are used for amplification because of their low cost and high gain at high frequencies (100 MHz). This allows the internal power supply design to be simplified because only +5 volts is required. Trigger levels and slope controls can be set from the front panel, enabling the counter to function correctly with all waveforms. A separate/common-A switch allows timing measurements to be made using only Channel A or both channels. For frequency measurements the counting chain will direct count to 10 MHz, and an ECL prescaler can be switched in to allow counting of frequencies to 100 MHz. To conserve power, the prescaler is disconnected when not in use, reducing power consumption by more than 15%.

Two options are available: a temperature-compensated crystal oscillator (TCXO) and a battery pack. The battery is automatically switched in and will power the instrument for about eight hours any time ac power is not present. The battery pack and charging scheme used in the 5314A are similar to (but simpler than) those of the 5315A Universal Counter, as described in the accompanying article.

A comparison of the 5314A with a predecessor, the 5300B/5302A, shows that the 5314A actually has superior capability in frequency response, sensitivity, and timing resolution, yet sells

for less than half the price. Not only does the 5314A provide good performance, it should be very low in maintenance requirements due to its high estimated mean time between failures (MTBF ≈ 40,000 hr) and easy access to the printed circuit boards. No extender boards or special cables are required.

A special power transformer conforms to IEC and VDE (Verband Deutcher Electrotechniker) safety standards. The standard 5314A has exceptionally low electromagnetic emissions. Extensive environmental and life testing insure that this instrument will provide good measuring capability in a wide variety of applications.

**Acknowledgments**

Without the involvement of many people this project would not have been possible. Both Jim Horner and Ian Band provided valuable criticism and encouragement to keep the project on target for a timely introduction while meeting the technical goals. Valuable mechanical contributions were provided by Eric Havstad, Ashok Phadke and Mike Detro. These people developed several previously untried ideas, many of which were incorporated into the final design. Bob Bliven provided many good ideas on the front-panel layout in spite of countless changes. Lew Masters, with his previous experience in low-cost counters, was helpful in product definition. Ivan Andres also provided good support and many good ideas for this project. Numerous production people provided useful information to make the design more producible.

**David M. George**

David George received his BSEE degree from the University of Utah in 1976 and his MSEE from Stanford University in 1977. Joining HP in 1977, he took the 5314A Universal Counter from initial design through its release to production. David was born in Waco, Texas and grew up in Ogden, Utah. He is single, lives in Campbell, California, and enjoys skiing, skin diving, and hiking.

**Michael D. Wilson**

Born in Monterey Park, California, Mike Wilson is a 1972 BSEE and 1973 Master of Engineering graduate of California State Polytechnic University at San Luis Obispo. Mike joined HP shortly after graduation in 1973 and has worked as design engineer on the 5328A Universal Counter and as project leader on two 5328A options and the 5314A Universal Counter. A member of IEEE, he is currently production engineering supervisor for logic test and precision frequency sources. Mike is married, has a 19-month-old daughter and lives in Santa Clara, California. In the summer months, he enjoys catamaran racing and playing softball, while his winter months are spent skiing and playing volleyball.

high current level or a very high float voltage level. The required current level exceeded the power limitations of both the power transformer and the instrument package. The high float voltage would severely reduce the life of the battery in standby applications. While the constant-current technique would provide recharge times suitable for once-a-day cycling at a moderate current level, problems exist in sensing end-of-charge reliably at that current level. This could result in reduced battery life due to overcharging and/or less than optimum performance in standby applications.

The charging circuit used in the 5315A battery pack takes advantage of two characteristics of the Gates lead-acid cell. When charged at a constant current equal to one-tenth of the rated capacity, the cell voltage reaches a particular value after 90% of the charge previously taken from the cell is returned.* Also, in an overcharge state, application of a constant current causes the cell voltage to float near a particular level. Using these two characteristics, it was possible to design a charger capable of recharging a fully discharged battery in 16 hours, reliably sensing end of charge, and providing a safe float voltage for standby applications. It accomplishes this at moderate power and good efficiency. The charging technique is called "two-step constant-current state-of-charge sampled," or in fewer words, hysteresis charging.

The circuit consists of a parallel arrangement of high and low-current regulators that supply charge current to the battery, and a voltage comparator circuit with hysteresis that monitors the battery voltage and controls the operation of the high-current regulator. The charging cycle involves three stages of operation (see Fig. 6). The battery is initially supplied with a constant current of 500 mA from both current regulators (high current = 490 mA; low current = 10 mA). The upper threshold of the comparator hysteresis window coincides with the battery voltage corresponding to the 90% charge-returned point. When the battery voltage reaches this level, the comparator disables the high-current state, and the battery voltage starts to drop. The lower threshold of the comparator is set below the overcharge float voltage level corresponding to the 10 mA constant current. When the battery voltage reaches this lower threshold, the comparator enables the high-current regulator and the charge current returns to 500 mA. The battery voltage again rises to the upper threshold

*The 90% figure does not take the charge acceptance of the battery into account. If the charge were terminated at this point and the battery subsequently discharged, approximately 72% of the rated capacity would be available.

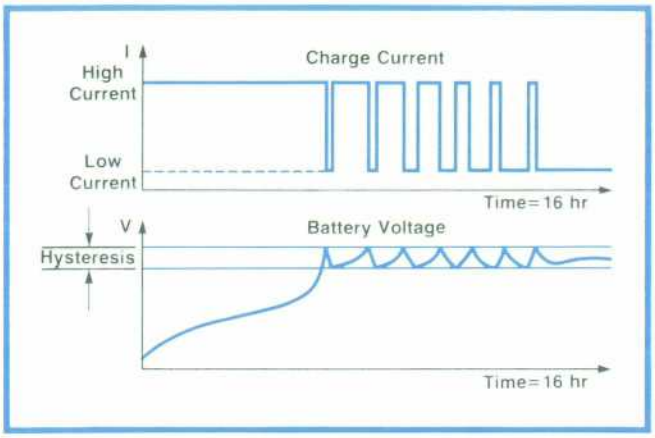



**Fig. 6.** *Three-stage hysteresis charging cycle for the lead-acid batteries.*

of the comparator and the process is repeated. This second stage of operation, with the battery charge current switching between 500 mA and 10 mA, continues until the battery voltage fails to reach the lower threshold of the comparator in the 10-mA state. At this point the battery is 95-97% charged. In the final stage of the cycle, the battery is maintained at the 10 mA current level and the remaining 3-5% of charge is returned to the battery. At full charge, the 10-mA constant current causes a battery voltage of approximately 2.4 volts/cell (7.2 volts). The battery can be safely maintained at this level for standby applications.

An additional benefit of the hysteresis charger is that normal operation of the circuit provides useful charge status information. An LED in the display section of the instrument monitors the activity of the charge circuit comparator, indicating the three stages of the charge cycle. During the first stage of the cycle, the LED is off to indicate that less than 70% of the discharged capacity has been returned and the charger is in the high-current state. During the second stage of operation, the LED flashes on and off to indicate the low and high-current states, respectively. This stage occurs after approximately 70% of the previously discharged capacity has been returned (charge acceptance accounted for). During this stage, the ratio of the time the charger spends in the high-current state to the time it spends in the low-current state depends on the absolute state of charge of the battery. This means that in addition to information on the amount of charge returned, indicated by the flashing LED, the ratio of the LED's on time to its off time gives an indication of the absolute state of charge.

In the third stage, the LED is on continuously, indicating that the battery is at least 95-97% charged and the charger is in the low-current state.

A temperature compensation feature of the charger circuit provides proper charging and protection for the battery at high and low temperatures. This is accomplished by automatically adjusting the level and size of the charge comparator hysteresis window as a function of temperature.

In battery operation the 5315A battery pack pro-


**Lewis W. Masters**

Lew Masters received his BSME degree in 1966 from the University of Maryland and his MSEE degree in 1969 from the University of California at Santa Barbara. An HP employee since 1970, Lew has designed several modules for the 5300A Counter Mainframe and was project leader for the 5381A/82A/83A Frequency Counters and the 5315A Universal Counter. Before coming to HP, he was in aerospace mechanical design. Raised in Washington, D.C., Lew is married and lives in Los Altos, California. He enjoys building furniture and remodeling his home in his spare time.

**Karl M. Blankenship**

Karl Blankenship received his BSEE degree from Stanford University in 1973 and joined HP the same year. Before taking on the power system design for the 5315A/B Universal Counter, he was responsible for the design of several circuits and options for the 5328A Universal Counter. Born in Los Angeles, Karl is married, has a son, and lives in San Jose, California. He enjoys bowling, basketball, and jazz, writes short stories and poetry, and spends a lot of time on family activities, especially supporting his son's budding gymnastics talent.

**Michael J. Ward**

Mike Ward designed the input amplifiers and associated circuits for the 5315A/B Universal Counter. With HP since 1973, he was involved in the design of several boards and products for HP's laser interferometer systems before switching to the counter lab. Mike was born in Worcester, Massachusetts. He received his BSEE degree in 1966 and his MSEE in 1968 from Massachusetts Institute of Technology, and did RF and microwave design for an aerospace company before coming to HP. He's a member of IEEE. In his spare time, he edits and publishes a small magazine about science fiction. He's also a fan of railway and transit systems and of old-time jazz. Mike is single and lives in Sunnyvale, California.

vides automatic shutdown and discharge status annunciation. Automatic shutdown is controlled by the low-battery detector circuit. This circuit consists of a voltage comparator with hysteresis that monitors the battery voltage during discharge. When the voltage falls below the low threshold of the comparator, the change of state of the comparator output is sensed by the dc-dc converter and regulator section of the main power supply. As a result, the operation of these circuits is disabled and the current drain on the battery is reduced to approximately 10 mA. At this point, approximately 80% of the battery's rated capacity has been used, allowing for a reserve capacity of 20%. The instrument can remain in this state for 4-5 days without damaging the battery.

An LED in the display section of the instrument and circuitry that monitors the activity of the low-battery detector provide useful annunciation during battery operation. The LED is on continuously whenever the instrument is operating from the battery and the battery voltage is above the auto shutdown point. Auto shutdown is indicated when the same LED flashes at a slow rate. This reduces the possibility of unintentionally discharging the battery and informs the user when recharge is necessary.


## Acknowledgments

The project team would like to thank a few of the many individuals who helped make the 5315A/B project successful. Carl Spalding contributed the product design with assistance from Bill Anson and Eric Havstad. Jim Feagin contributed many ideas on how to make the instrument testable and producible. Russ Aleshi and Bill Ruhl provided the automatic test programs, while Bob Boss and Jim Conforti guided the instrument through pilot run. Finally, Jim Horner gave us a clear goal and provided the support necessary to achieve it.


## ABRIDGED SPECIFICATIONS

### HP Model 5315A/B Universal Counter

**INPUT CHARACTERISTICS:** (Channel A and Channel B)
RANGE:
Dc coupled: 0 to 100 MHz.
Ac coupled: 30 Hz to 100 MHz.
SENSITIVITY:
10 mV rms sine wave to 10 MHz.
25 mV rms sine wave to 100 MHz.
75 mV peak-to-peak pulse at minimum pulse width of 5 ns. Sensitivity can be varied continuously up to 500 mV rms NOMINAL by adjusting sensitivity control. In sensitivity mode, trigger level is automatically set to 0V NOMINAL.
COUPLING: ac or dc switchable.
IMPEDANCE:
1 MΩ NOMINAL shunted by less than 40 pF.
500 kΩ NOMINAL shunted by less than 70 pF (COMMON A).
ATTENUATOR: ×1 or ×20 NOMINAL.
TRIGGER LEVEL: Variable between +2V and −2V.
SLOPE: Independent selection of + or − slope.
CHANNEL INPUT: SEPARATE or COMMON A.

**FREQUENCY:**
RANGE: 0.1 Hz to 100 MHz.
LSD* DISPLAYED: 10 Hz to 1 nHz depending upon gate time and input signal. At least 7 digits displayed per second of gate time.

**PERIOD:**
RANGE: 10 ns to $10^5$ s.
LSD* DISPLAYED: 100 ns to 1 fs depending upon gate time and input signal. At least 7 digits displayed per second of gate time.

**TIME INTERVAL:**
RANGE: 100 ns to $10^5$ s.
LSD* DISPLAYED: 100 ns.

**TIME INTERVAL AVERAGE:**
RANGE: 0 ns to $10^5$ s.
LSD* DISPLAYED: 100 ns to 10 ps depending upon gate time and input signal.
MINIMUM DEAD TIME (stop to start): 200 ns.

**TIME INTERVAL HOLDOFF (Delay):** Front panel gate time knob inserts a variable delay of NOMINALLY 500 μs to 20 ms between START (Channel A) and enabling of STOP (Channel B). Electrical inputs during delay time are ignored. Delay time may be digitally measured by simultaneously pressing T.I. Averaging, T.I. Delay, and blue key. Other specifications of T.I. Holdoff are identical to Time Interval.

**RATIO:**
RANGE: 0.1 Hz to 100 MHz, both channels.
LSD:
$$\frac{2.5 \times \text{Period A}}{\text{Gate Time}} = \text{Ratio} \quad \text{(rounded to nearest decade)}$$

**TOTALIZE:**
MANUAL: Range: 0 to 100 MHz.
A GATED BY B: Totalizes input A between two events of B. Instrument must be reset to make new measurement. Gate opens on A slope, closes on B slope. Range: 0 to 100 MHz.

**TIME BASE:**
FREQUENCY: 10 MHz.
AGING RATE: <3 parts in $10^7$/mo.
TEMPERATURE: ≤±5 parts in $10^6$, 0 to 50°C.

**GENERAL:**
CHECK: Counts internal 10 MHz reference frequency over gate time range NOMINALLY 500 μs to 20 ms.
DISPLAY: 8-digit amber LED display, with engineering units annunciator.
GATE TIME: Continuously variable, NOMINALLY from 50 ms to 10 s or 1 period of the input, whichever is longer.
SAMPLE RATE: Up to 5 readings per second NOMINAL except in time interval mode, where it is continuously variable NOMINALLY from 250 ms to 10 s via Gate Time control.
OPERATING TEMPERATURE: 0°C to 50°C.
POWER REQUIREMENTS: 100, 115, 210, 230V (+5%, −10%) 48-66 Hz; 10 VA max.
WEIGHT: 2.9 kg (6 lb 5 oz).
DIMENSIONS: 238 mm W × 98 mm H × 276 mm L (9⅜ × 3⅞ × 10⅞ in).

**OPTIONS:**
OPTION 001: High Stability Time Base (TCXO).
FREQUENCY: 10 MHz.
AGING RATE: <1 part in $10^7$/mo.
TEMPERATURE: <1 part in $10^6$, 0° to 40°C.
OPTION 002: Battery.
TYPE: Rechargeable lead-acid (sealed).
CAPACITY: TYPICALLY 4 hours of continuous operation at 25°C.
RECHARGING TIME: TYPICALLY 16 hours to 98% of full charge, instrument nonoperating. Charging circuitry included with Option. Batteries not charged during instrument operation.
LOW VOLTAGE INDICATOR: Instrument turns itself off automatically when low battery condition exists. DISCHARGE LED flashes slowly when this happens. DISCHARGE LED is on whenever battery is supplying power to instrument.
CHARGE LED indicates state of charge of battery during charging only and is on whenever battery is charged to 95% NOMINAL of capacity.
CHARGE LED flashes when 90% NOMINAL of charge taken out is replaced. Charge LED is off if charge is less than 70% NOMINAL of capacity.
LINE FAILURE PROTECTION: Instrument automatically switches to battery in case of line failure.
WEIGHT: Option 002 adds 1.4 kg (3 lbs.) to weight of instrument.

**5315B:**
Rack and stack metal case; ac line power only. Specifications same as 5315A except as follows:
OSCILLATOR OUTPUT: 10 MHz, 50 mV p-p into 500Ω load.
EXTERNAL FREQUENCY STANDARD: 10 MHz, 1V rms into 500Ω.
DIMENSIONS: 215 mm W × 81 mm H × 279 mm L (8⅜ × 3⅛ × 10⅞ in.)
WEIGHT: 4 kg (8 lb 13 oz).

**PRICES IN U.S.A.:**
5315A 100 MHz 100 ns Universal Counter, $800.
5315B 100 MHz 100 ns Universal Counter in Metal Rack/Stack Package, $950.
OPTIONS:
001 High Stability Time Base, $100.
002 Battery (available with 5315A only), $225.

***LEAST SIGNIFICANT DIGIT (LSD) DISPLAYED (5315A/B):**
FREQUENCY:

| | |
|---|---|
| $\frac{2.5 \times 10^{-7}}{\text{Gate Time}} \times \text{FREQ}$ | FREQ <10 MHz |
| $\frac{2.5}{\text{Gate Time}}$ | FREQ ≥10 MHz |

PERIOD:

| | |
|---|---|
| $\frac{2.5 \times 10^{-7}}{\text{Gate Time}} \times \text{PER}$ | PER <100 ns |
| $\frac{2.5}{\text{Gate Time}} \times \text{PER}^2$ | PER <100 ns |

All above calculations should be rounded to nearest decade (i.e., 0.5 Hz will become 1 Hz and 0.4 ns will be 0.1 ns).

TIME INTERVAL AVERAGE:

| | LSD |
|---|---|
| 1 to 25 intervals | 100 ns |
| 25 to 2500 intervals | 10 ns |
| 2500 to 250,000 intervals | 1 ns |
| 250,000 to 25,000,000 intervals | 100 ps |
| >25,000,000 intervals | 10 ps |

### HP Model 5314A Universal Counter

**INPUT CHARACTERISTICS:**
RANGE: Channel A: 10 Hz to 100 MHz.
Channel B: 10 Hz to 2.5 MHz.
SENSITIVITY:
Channel A: 25 mV rms to 100 MHz.
75 mV peak-to-peak minimum pulse width of 5 ns.
Channel B: 25 mV rms to 2.5 MHz.
75 mV peak-to-peak minimum pulse width of 200 ns.
COUPLING: ac.
IMPEDANCE: 1 MΩ NOMINAL, shunted by less than 30 pF.
ATTENUATOR: ×1 or ×20 NOMINAL (A Channel only).
TRIGGER LEVEL: Continuously variable ±350 mV times attenuator setting around average value of signal.
SLOPE: Independent selection of + or − slope.
CHANNEL INPUT: Selectable SEPARATE or COMMON A.

**FREQUENCY:**
RANGE: 10 Hz to 10 MHz direct count.
10 Hz to 100 MHz prescaled by 10.
LSD DISPLAYED: Direct count 0.1 Hz, 1 Hz, 10 Hz switch selectable.
Prescaled 10 Hz, 100 Hz, 1 kHz switch selectable.

**PERIOD:**
RANGE: 10 Hz to 2.5 MHz.
LSD DISPLAYED: $\frac{100 \text{ ns}}{N}$ for N = 1 to 1000 in decade steps of N.

**TIME INTERVAL:**
RANGE: 250 ns to 1 s.
LSD DISPLAYED: 100 ns.

**RATIO (A to B):**
RANGE: 10 Hz to 10 MHz Channel A.
10 Hz to 2.5 MHz Channel B.
LSD DISPLAYED: 1/N in decade steps of N for N = 1 to 1000.

**TOTALIZE:**
RANGE: 10 Hz to 10 MHz.
Totalize controlled by front panel switch.

**GENERAL:**
CHECK: Counts internal 10 MHz oscillator.
DISPLAY: 7-digit amber LED display with gate and overflow indication.
MAXIMUM SAMPLE RATE: 5 readings per second.
OPERATING TEMPERATURE: 0° to 50°C.
POWER REQUIREMENT: 115; +10%, −25%; 230V, −17%, +9%; 48-66 Hz; 10 VA maximum.
WEIGHT: 2.0 kg (4.4 lbs.).
DIMENSION: 238 mm W × 98 mm H × 276 mm L (9⅜ × 3⅞ × 10⅞ in.)

**TIME BASE:**
FREQUENCY: 10 MHz.
AGING RATE: <3 parts in $10^7$ per month.
TEMPERATURE: <1 part in $10^6$, 0 to 50°C.

**OPTIONS:**
OPTION 001: High Stability Time Base (TCXO).
FREQUENCY: 10 MHz.
AGING RATE: <1 part in $10^7$ per month.
TEMPERATURE: <1 part in $10^6$, 0 to 40°C.
OPTION 002: Battery.
TYPE: Rechargeable lead-acid (sealed).
CAPACITY: TYPICALLY 8 hours of continuous operation at 25°C.
RECHARGING TIME: TYPICALLY 16 hours to 98% of full charge, instrument nonoperating. Charging circuitry included with option. Batteries not charged during instrument operation.
BATTERY VOLTAGE SENSOR: Automatically shuts instrument off when low battery condition exists.
LINE FAILURE PROTECTION: Instrument automatically switched to batteries in case of line failure.
WEIGHT: Option 002 adds 1.5 kg (3.3 lbs.) to weight of instrument.

**PRICES IN U.S.A.:**
5314A 100 MHz 100 ns Universal Counter, $375.
OPTIONS:
001 High Stability Time Base, $100.
002 Battery, $95.

**MANUFACTURING DIVISION:** SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050

# A High-Performance Bipolar LSI Counter Chip Using EFL and I²L circuits

*This state-of-the-art multiple-register counter chip contains all of the circuits needed for a 100-MHz universal counter except for the display, input amplifiers, power supply, and controller (microprocessor).*

**by Bosco W. Wong and William D. Jackson**

MICROPROCESSORS HAVE BROADENED performance capability in many new counter products. Intricate computing abilities are now readily obtainable in commercially available microprocessor chip sets. However, microprocessors alone cannot carry out complex counting functions. In addition to the processor unit, various circuit elements, both digital and analog, are required to accept, store, and regenerate data for different phases and different types of measuring functions.

As a group, these circuit elements cover a wide range of performance requirements. To optimize their performance, we felt that it was highly desirable if not totally essential to implement them in a special integrated circuit chip. For this reason, a custom bipolar LSI chip known as the multiple-register counter (MRC) has been developed for the new generation of microprocessor-controlled counter products. Except for the controller (microprocessor), the display circuitry, the signal input amplifiers, and the instrument power supply, all of the circuits required to perform all necessary counting functions are included in the MRC chip.

The decision to implement the MRC chip in the bipolar LSI process is mainly based on three factors. First, the process can accommodate mixed logic families with divergent performance characteristics, namely emitter function logic (EFL) and integrated injection logic (I²L). Second, the process can accommodate miscellaneous circuit configurations, both digital and analog. Third, the dual-layer metallization feature of the process provides an efficient means of solving the complex high-density logic interconnection problem.

### A Data-Acquisition Chip

The MRC chip has been specifically designed for universal counter use. The chip performs all the data-acquisition functions of a universal counter or timer when controlled by a microprocessor. For instrument performance flexibility and chip design simplicity, data computation features have not been included in the MRC. Instead, the processor performs all necessary calculations, with measurement data furnished by the MRC chip.

The MRC is designed not for a single counter but rather for a number of different counter products with a variety of performance requirements. Thus, its performance capability is broad and flexible. Depending on the type of processor and/or accessory circuits used, the MRC can provide a wide range of measurement capability, including different modes of frequency, period, time interval, ratio, totalizing, and other measurements.

### Multiple-Register Structure

The name multiple-register counter is derived from the chip's logic organization, a parallel multi-register structure. Fig. 1 is the basic functional block diagram of the MRC. The four registers—the E (event), T (timing reference), C (control) and S (status) registers—operate in parallel for I/O access.

The E and T registers are chains of eight decades each, with the front-end (first) decades capable of counting signals over 100 MHz. Because of the division factor of $10^8$ resulting from the eight-decade serial arrangement, the signal frequency coming out of the tail-end (last) decades is only 1 Hz for a 100-MHz input frequency. To optimize speed, power, and device density, it is obvious that different types of circuits should be used for different segments of the chains. Accordingly, the first two decades of the E and T registers are implemented as EFL circuits to meet the speed requirements, while the remaining six decades are I²L circuits for high device packing density and low power consumption.

Signal counting takes place in these two registers when gated by the sequencer block. An overflow flip-flop is provided for each of the two registers to extend the effective length of the counting chains.

The 20-bit control register serves as a storage buffer for program instructions received from the processor through the I/O block. As the name implies, it controls the general operation of the MRC chip. Specifically,

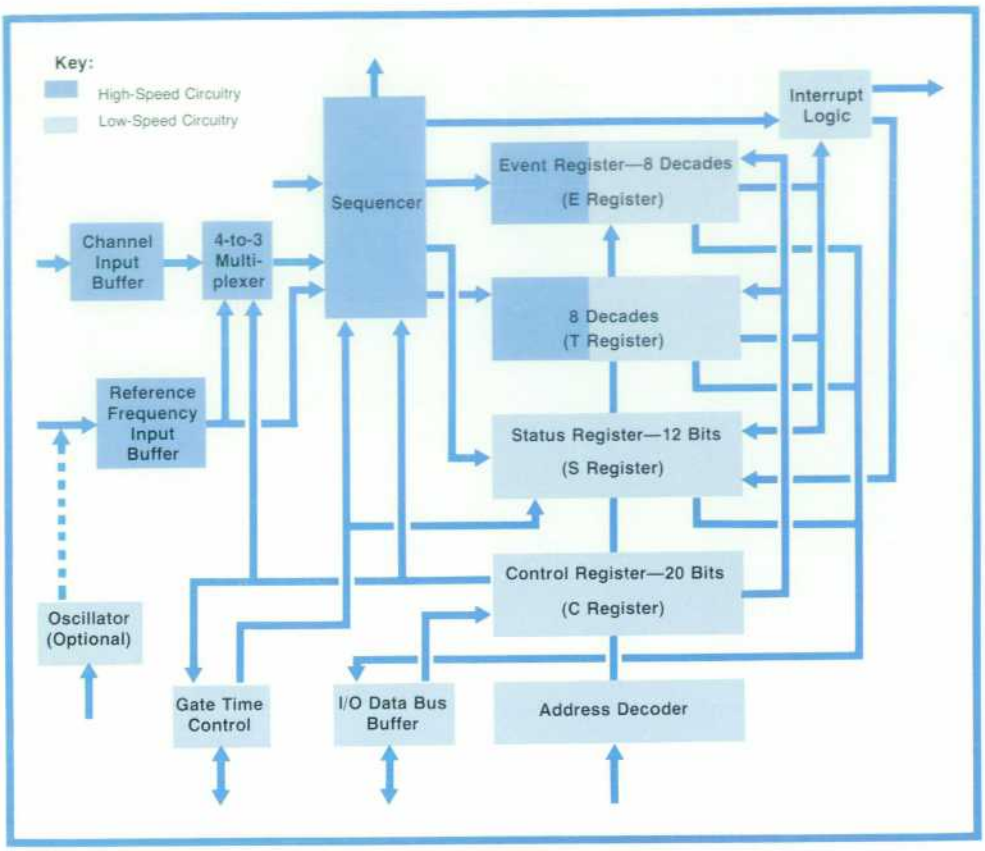



**Fig. 1.** *Multiple-register counter (MRC) chip functional block diagram.*

the jobs of the C register are to define the particular mode of the measuring functions, to set up proper synchronization and timing of the sequencer block, and to carry out the reset routine before a measurement is initiated.

Operational status of the MRC, including measurement cycle arming and gating, overflow of the two counting (E and T) registers, measurement interrupt and time-out, and so on, is recorded in the 12-bit status register and is available to the processor when properly addressed.

To minimize package pin count, the four-bit I/O bus is bidirectional (see Fig. 1). The bus is shared by the four registers. Through the address decoder block, any of the four registers can be selected. The C register uses the bus for the data input function (i.e., the write function), and the E, T and S registers use the bus for the data output function (i.e., the read function). Once a read or write function has been requested and a particular register has been selected, individual decades (in the case of the E and T registers), or individual words (in the case of the C and S registers), are accessed sequentially by scanning the 3-to-8 nibble-select logic within the address decoder block.

### Sophisticated Gating Functions

Of all of the functional blocks in the MRC, the sequencer logic block is most critical to the complex counting capability of the chip. In the sequencer block, two key elements that enable the MRC to excel in performance are a sophisticated gating synchronization technique and the realization of this technique with EFL and other circuits in a super-speed bipolar LSI process.

The gating technique involves three stages of successive synchronization: arming synchronization, synchronization for E-register gating, and synchronization for T-register gating. This scheme provides maximum measurement resolution in the sense that measurement error is limited to $\pm 1$ count of either the input frequency or the reference oscillator frequency, whichever is higher.

The bipolar LSI process features dual-layer metallization, which reduces on-chip parasitics, and an $f_T$ of 1 GHz for fast device switching.

Complementing the sequencer logic block are the high-speed three-channel input buffer and the high-speed 4-to-3 multiplexer. Signals to be measured are received through the channel inputs. They are then directed into the E and/or T counting registers via the multiplexer and the sequencer. The multiplexer block is responsible for proper signal routing based on the selected measuring function, while the sequencer logic block is responsible for gating synchronization.

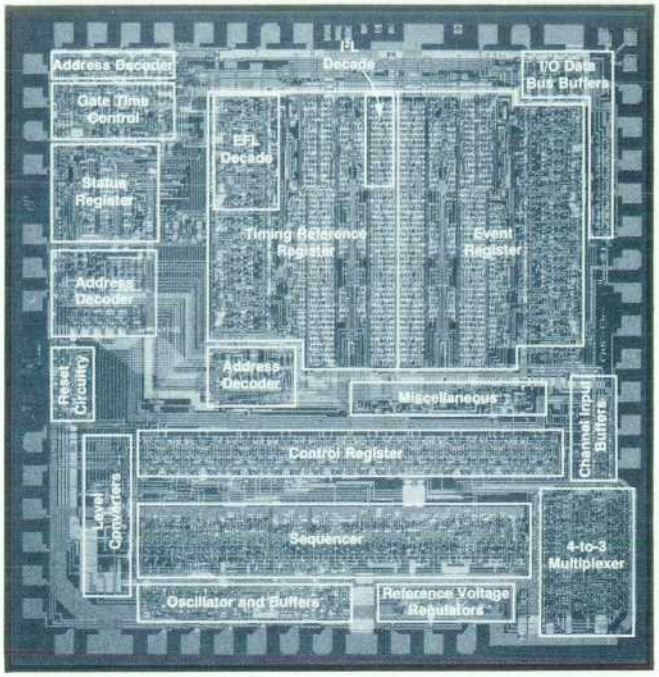



**Fig. 2.** *MRC chip layout. EFL circuits are used where high speed is needed. I²L is used for low power consumption and high density.*

### Circuit and Mask Design Requirements

The diverse circuit performance requirements, including wide deviations of device speed, variable packing density, mixing of logic families, on-chip interplay among various types of digital and analog circuits, and narrow noise margins (because of the low supply voltage used), have made implementation of the MRC more than a trivial task. Aside from coming up with an adequate assortment of digital and analog circuit elements to realize various circuit functions, considerable engineering effort has also been given to planning and design of the mask topology.

Special care has been taken to minimize cross-coupling between adjacent high-speed input signals, to provide adequate ground connections (or taps) to minimize IR drop for the ground-potential-sensitive I²L circuit blocks (see box, page 17), to alleviate heat-gradient problems resulting from uneven power consumption of different types of circuits in different locations of the chip, to ensure adequate noise margin by generating on-chip temperature-compensated reference voltages for the EFL circuits, and to provide additional test probe pads to reduce the normally lengthy time required for testing multidecade chains.

Fig. 2 is a photomicrograph of the MRC chip. To show the difference in device density, the cell layouts of an EFL decade and an I²L decade are marked.

### Assortment of Circuits

Aside from conventional logic elements, such as multi-input logic gates, flip-flops, decades, and so on, which are implemented extensively in EFL or I²L throughout the chip, a variety of other special-function circuits, both digital and analog, are used in the MRC. The digital circuits include miscellaneous types of input-output buffers, high-speed and low-speed multiplexers, different types of delay circuits for timing use, special purpose complementary clock drivers, matrix decoders, EFL to I²L level converters, and vice versa. The analog circuits include precision voltage regulators, Schmitt triggers, oscillators, differential amplifiers, and voltage level detectors.

A few of the MRC circuits are unusual enough to warrant further discussion. These include the timing delay circuit, matrix decoder, and level converters.

### I²L Delay Circuit

The timing delay circuit is implemented in low-current I²L gates. In the past, IC designers have had difficulty implementing well-controlled long-delay

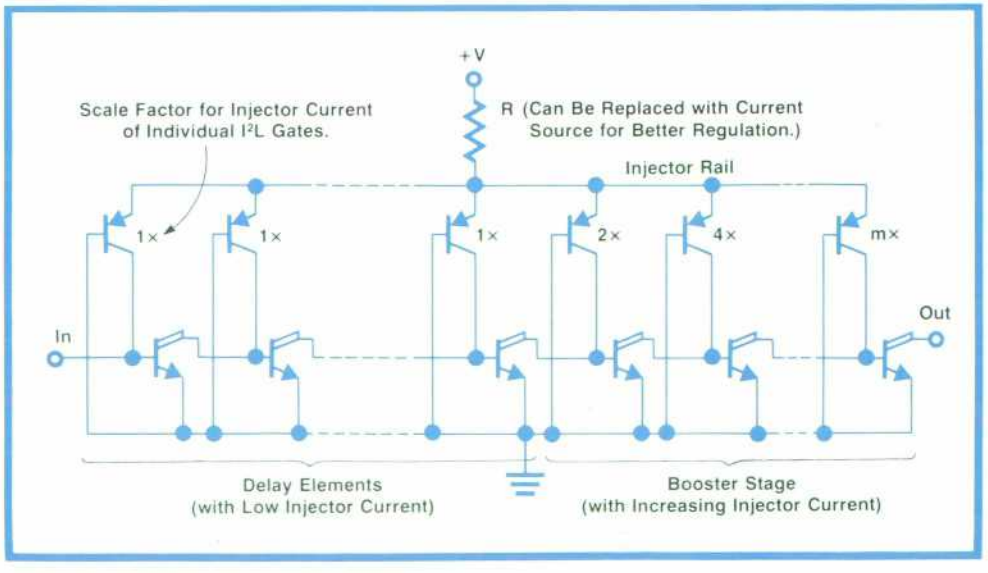



**Fig. 3.** *I²L delay circuit provides delays in the millisecond range.*

circuit elements with conventional bipolar circuit techniques. The difficulty is mainly due to two factors, namely the relatively fast transit time of conventional bipolar transistors and the impracticality of making large-value on-chip capacitors and resistors. It takes a moderately complex circuit and tight process control to generate a signal delay of up to a few microseconds. Longer delays usually require off-chip RC trimming.

By taking advantage of the intrinsically slower propagation delay of I²L transistors and by appropriately controlling the magnitude of the injector current in the I²L gates, the MRC delay circuit, implemented in special serially connected I²L gates, provides delay times not only of microseconds but of milliseconds. Fig. 3 shows the relatively simple circuit. The delay is strictly a function of the number of series I²L gates used and the magnitude of the injector current into each individual gate.

For long delay requirements, the injector current should be held to a minimum for the bulk of the delay string. However, for adequate drive to other circuit blocks, the final section of the delay string should have increased injector current, as shown in Fig. 3. If the delay circuit is properly designed, the delay time will be within ±20% of target value. Further accuracy

## Emitter Function Logic

**by Bosco W. Wong**

Emitter function logic (EFL), is a relatively new type of logic circuit that is particularly useful for LSI implementation whenever high switching speed is required. Developed by Z.E. Skokan of Hewlett-Packard Laboratories, EFL is designed to capitalize on two logic circuit features, namely the multi-emitter structure normally found in TTL, and the nonsaturating current mode operation used in ECL. To minimize propagation delay, EFL uses noninverting gates. Its intrinsic gate delay is considerably less than that of other common logic families, such as TTL, which use inverting gates.

EFL bears some degree of resemblance to the popular ECL family. However, EFL exceeds ECL in cell density and in other aspects of performance. While both EFL and ECL use the nonsaturated operating region of switching transistors for fast switching performance, EFL requires a reduced total bias voltage of only 3V, compared with the typical 5.2V of ECL. Also, an efficient circuit partition technique known as functional integration, employed exclusively in EFL, greatly reduces the overall complexity of the circuit compared with ECL.

The most prominent feature of EFL is the functional integration capability. Boolean functions can be directly implemented in EFL gates without resorting to the conventional transformation procedure. This means that Boolean equations need not be converted into formatted structures like NAND and NOR expressions before circuit implementation. Essentially, each basic EFL gate, with appropriate variations, can be used to realize different sets of multiple logic functions, such as sum-of-products or product-of-sums expressions.

To illustrate the functional integration aspect of EFL gates, Fig. 1 shows two EFL gate elements, each representing a different Boolean expression. The first gate (Fig. 1a) represents a simple two-input AND function involving only one Boolean gate. The second EFL gate (Fig. 1b) represents a product-of-sums expression equivalent to four Boolean gates. A brief comparison of the two EFL gate elements reveals that while the component counts for both elements are almost the same (i.e., four transistors and two resistors in one element and five transistors and one resistor in the other), the Boolean gate counts for the two EFL gate elements are quite different (i.e., by a 1:4 ratio). It is important that EFL designers be aware of this flexible capability of EFL and take care to maximize their use of it.

**Acknowledgment**

The author would like to thank Z.E. Skokan for his many phases of technical support in EFL.

**Reference**

1. Z. Skokan, "Emitter-Function-Logic Logic Family for LSI," IEEE Journal of Solid-State Circuits, October 1973.

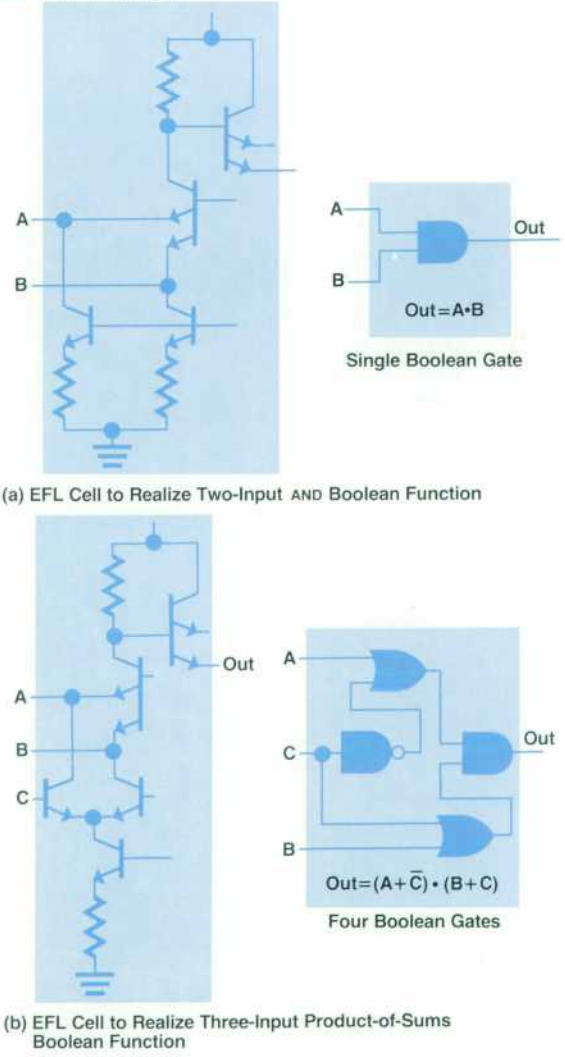



**Fig. 1.** *Two different EFL cells illustrate the flexibility of the functional integration feature of EFL.*

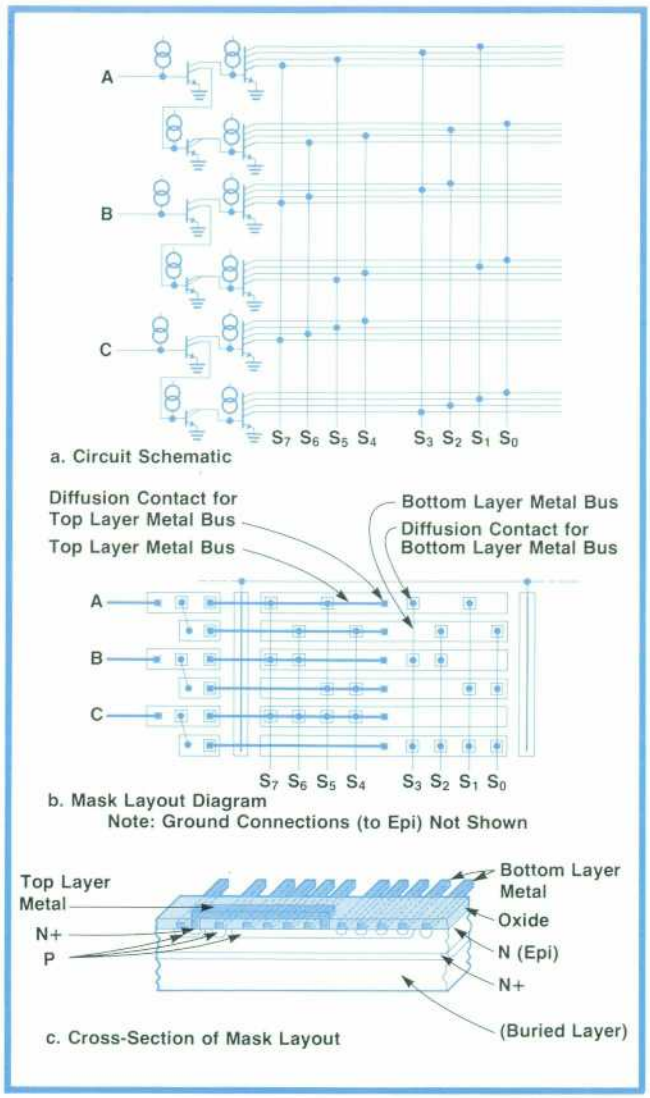



**Fig. 4.** *3-to-8 address decoder uses a double-injector scheme, with injector rails flanking both ends of the long inverse NPN transistors. Note the dense packing of the I²L gates and the convenience of dual-layer metallization for interconnections.*

can be achieved by replacing the resistor R with a well-regulated current source.

### Matrix Decoder

Fig. 4 shows the 3-to-8 address decoder, another circuit conveniently implemented in I²L. However, the design of this decoder differs slightly from the conventional way of using I²L (see Fig. 4b). Because of the array layout, the multicollector inverse NPN transistors are longer than those of regular I²L gates. To assure proper current drive for the worst-positioned collectors, which are the ones farthest from the injector rail, a double-injector scheme has been used, with injector rails flanking both ends of the long inverse NPN transistors.

The mask layout sketch and cross-section for the matrix decoder, Figs. 4b and 4c, also reveal two mask-topology features, the dense packing layout of the I²L gates and the convenience of logic hook-up using dual-layer metallization.

### EFL-to-I²L Converter Circuits

Since I²L gates operate at moderately slow speeds, the interface between EFL and I²L gates is reasonably simple. Fig. 5 shows two different voltage conversion schemes, one from EFL levels to I²L and the other from I²L to EFL.

In the EFL to I²L converter, the output transistor is a multicollector inverse NPN transistor, that is, a typical I²L gate without an injector. Since switching speed is not a prime requirement, lateral PNP transistors have been conveniently used in both converters.

### System Interface

Since the MRC is designed for a number of different counter products with a wide range of performance specifications, interface flexibility has been emphasized in the architectural design. The performance capability of the MRC depends largely on the type of controller. A prescale option has been provided for higher front-end counting frequencies and extended resolution. All input-output pins, except for the analog areas, are either TTL or ECL compatible.

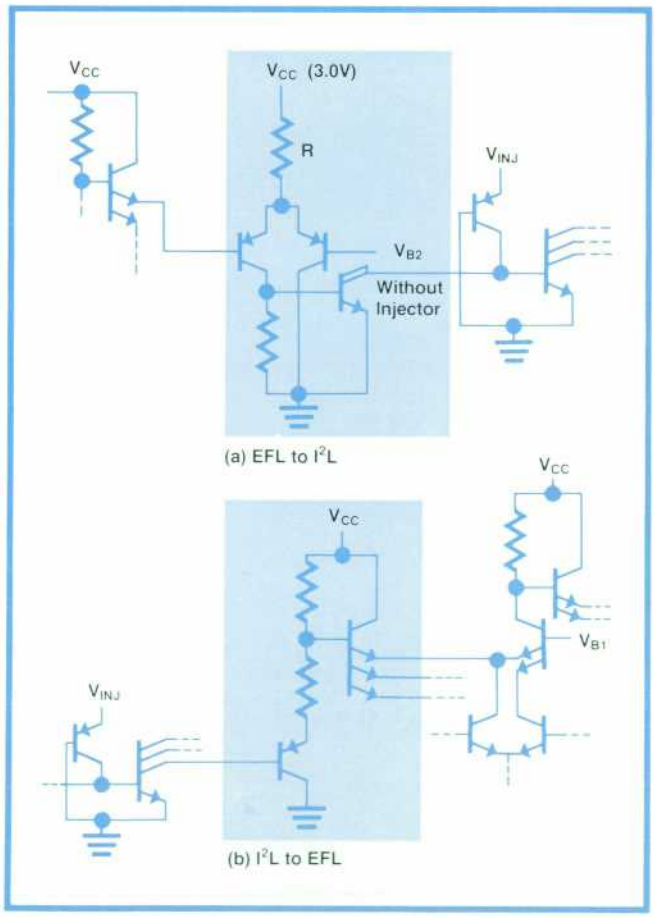



**Fig. 5.** *Voltage level converters used on the MRC chip.*

## Integrated Injection Logic

**by Bosco W. Wong**

A youngster among bipolar LSI circuit families, integrated injection logic ($I^2L$) has been looked upon by some LSI designers and users as a challenge to MOS in terms of device density and device performance. One fact that can hardly be denied is that $I^2L$ fills a desperate need for better device packing capability in bipolar LSI design.

The $I^2L$ gate has a rather simple structure. As shown in Fig. 1, it consists of a lateral PNP transistor as a current source and a multicollector inverse NPN transistor as an inverter.* The current source performs the function of a pullup resistor, but in most cases requires much less chip area. Also, the use of the PNP transistor as a current source makes it possible to have reasonable control of the magnitude of the injected current.

In the typical chip layout, the two transistors are merged into one nonisolated cell. Furthermore, it is possible to lay out a chip so that no isolation is required among different $I^2L$ gates. Hence device density can be very high. The need for isolation is minimized by taking advantage of certain properties of inverse NPN and lateral PNP transistors (see footnote).

The three attractive features of $I^2L$ are high packing density (~200 to 300 gates per $mm^2$), low power-speed product (typically sub-pJ), and on-chip compatibility with other popular bipolar LSI families and analog circuits. These have prompted the use of $I^2L$ circuit technology in a variety of bipolar LSI designs in the last few years.

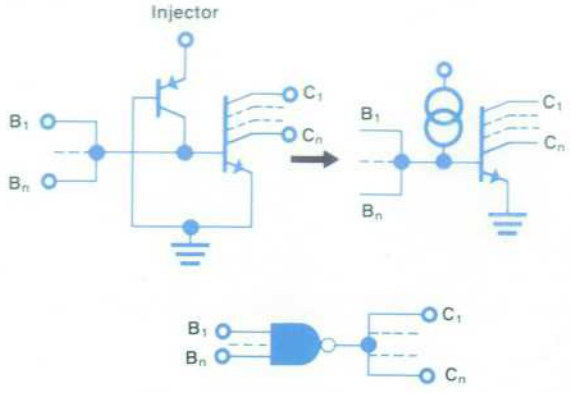



**Fig. 1.** *Typical $I^2L$ gate.*

The disadvantages of $I^2L$ fall into two areas. These are the limited fan-out capability of $I^2L$ gates and a low tolerance for IR drop along lengthy voltage lines or injector rails. In view of the limitations, $I^2L$ is better suited for the implementation of low-power serial logic, such as decade chains, serial registers, and delay lines, than for random logic functions. For random logic, $I^2L$ generally involves heavy parallel signal buses to connect circuit elements located in different areas of the chip.

*In a normal vertical NPN transistor the collector is in the N-doped epitaxial layer grown on the silicon wafer. The base is a P diffusion in this layer, and the emitter is an N diffusion inside the P area. Since the collectors of different transistors are not normally at the same potential, isolation is required between transistors. In an inverse NPN transistor the emitter is in the epitaxial layer, making this isolation unnecessary, since emitters are often tied together in conventional circuit design.

A lateral PNP transistor consists of two nearby P diffusions in the epitaxial layer, so that the emitter, base, and collector areas are side by side instead of one on top of the other. In $I^2L$, one of the P diffusions, the injector rail, forms the emitters of all of the PNP transistors, so these transistors need no isolation.

**Reference**

1. K. Hart and A. Slob, "Integrated Injection Logic: A New Approach to LSI," IEEE Journal of Solid State Circuits, October 1972.

Also, a chip enable-inhibit control input is available for convenient system multiplexing.

**Acknowledgments**

The MRC chip is a product of a solid team effort within HP's Santa Clara Division. Numerous people both in the IC department and in the engineering lab have made contributions to different phases of the development project. The authors would like to share the satisfaction derived from the successful MRC with Mike Catalano, who as a member of the design team for a period of time, was responsible for some of the novel design techniques. Special thanks should also go to Kay Bushey, Kazuko Kikuta, Percy Smith, Jay Thomas, Barry Welsh, Jim Grace, Ed Hilton, Larry Triplett and Dale Nieman.

**Bosco W. Wong**

Bosco Wong received his BSEE degree in 1967 and his MSEE in 1973 from California State University at San Jose. After four years with a major semiconductor company, mostly doing MOS RAM design, he joined HP in 1971. He's designed bipolar ICs for HP handheld calculators and served as project leader for $I^2L$ development work and for the MRC chip design. He's also co-authored a pair of papers on $I^2L$. Bosco was born in China and grew up in Hong Kong. He's married, has two sons, and now lives in Sunnyvale, California. His hobbies are table tennis, social dancing, and gourmet food.

**William D. Jackson**

Bill Jackson received his BSEE degree from the University of Arizona in 1970 and his MSEE from the University of Santa Clara in 1976. With HP since 1970, he's helped design the 5328A Universal Counter, the 10544A Oscillator, and the MRC chip. He's named as inventor on a patent on three-state trigger lights for counters. Born in Tuscon, Arizona, Bill is married and lives in Cupertino, California. He enjoys tennis, music, and travel.

# A Synthesized Signal Source with Function Generator Capabilities

*This fully programmable signal source spans 13 decades in frequency (1 μHz to 21 MHz) with synthesizer accuracy, and produces sine waves, square waves, triangles, and ramps with synthesizer stability and swept-frequency convenience.*

**by Dan D. Danielson and Stanley E. Froseth**

TWO TYPES OF SIGNAL SOURCES are finding increasingly wide use in today's world. One is the frequency synthesizer. Because of its programmability, the synthesizer finds many uses in automatic test equipment and, because of its inherent accuracy and high resolution, it also finds use as a local oscillator for receivers and as a precision tunable source for exacting tests, such as measuring crystal responses.

The other type, the function generator, is valued for its versatility, its capability for generating very low frequencies, its variety of waveform outputs, and its low cost. Among the applications of function generators are the step-response testing of loudspeakers and other electromechanical devices, filter transient response testing, amplifier and detector linearity testing, logic testing, control and timing, and tests involving materials, geophysics, and biomedicine.

The versatility of a function generator has now been combined with the accuracy, resolution, and programmability of a synthesizer in the HP Model 3325A Synthesizer/Function Generator (Fig. 1). As a frequency synthesizer, this instrument has a resolution of 11 digits and its sine-wave output covers an exceptionally wide range of frequencies, from 1 μHz to 21 MHz—over 13 decades. Unlike other synthesizers, the phase of the output can be adjusted over a ±720° range with respect to an internal reference. Also, it can sweep the entire frequency range or any part of it with a phase-continuous sweep (no transients between frequency steps). In terms of synthesizer performance, it has low sine-wave distortion (−65 dBc) at audio frequencies.

As a function generator, the Model 3325A is noteworthy because of its frequency accuracy, waveform precision (triangles and ramps with linearities within ±0.05%), low-frequency capability (to $10^{-6}$ Hz), and programmability. Output amplitude is adjustable up to 10 volts into 50Ω and the output can be offset up to ±4.5 Vdc. The offset can also be used by itself to provide a dc level up to ±5 V. Provisions are also included for phase modulating any output function and for amplitude modulating the sine-wave output. An optional output amplifier increases the output amplitude and offset by a factor of four (into 500Ω) up to 1 MHz.

Several convenience features in the new instrument include front- and rear-panel sync outputs, a rear-panel 20-60-MHz high frequency output pro-


**Fig. 1.** *Model 3325A Synthesizer/Function Generator produces waveforms with frequencies as low as 1 μHz and as high as 21 MHz for sine waves (to 11 MHz for square waves and 11 kHz for triangles and ramps) with synthesizer accuracy. Output amplitude over the full frequency range is 1 mV to 10 V p-p into 50Ω or, with an option, to 40V p-p into 500Ω over a frequency range of 1 μHz to 1 MHz. All necessary functions can be controlled through the HP interface bus as well as the front panel.*

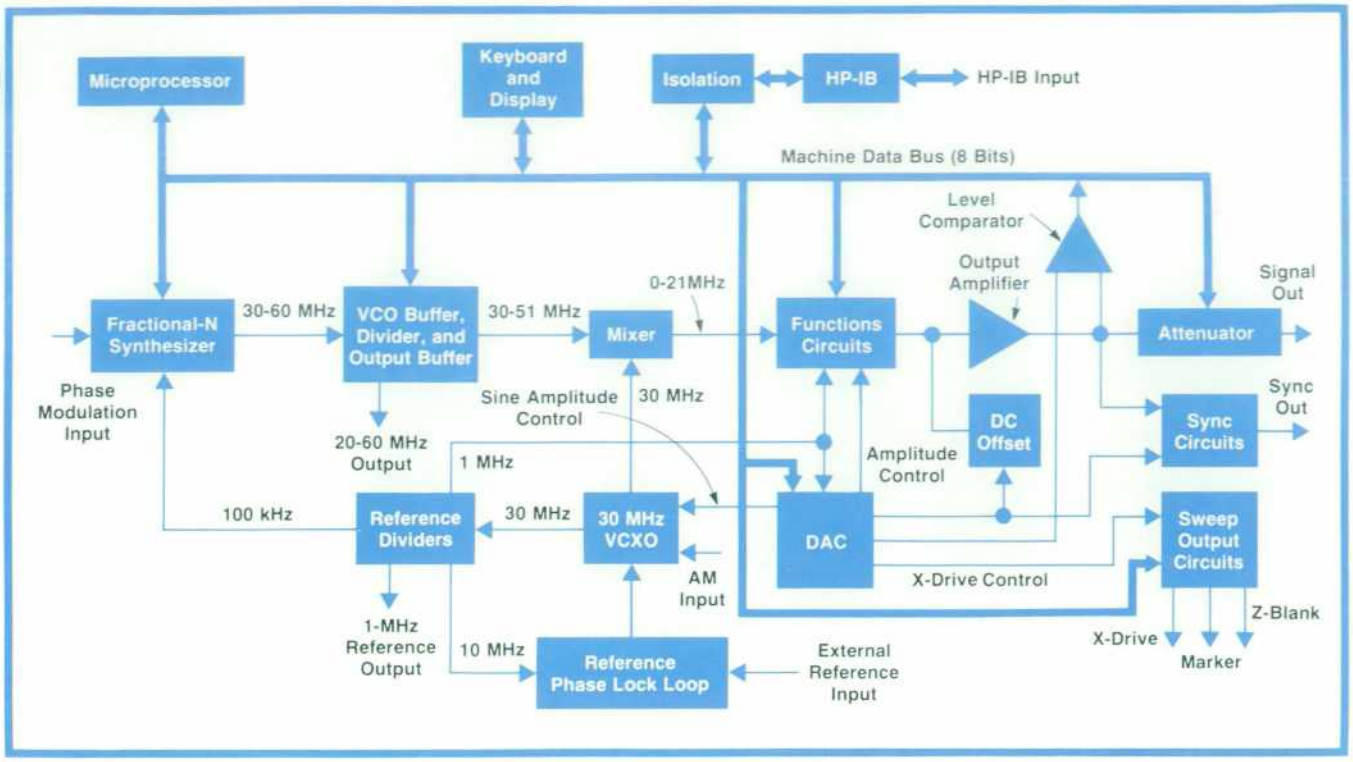



**Fig. 2.** *Block diagram of the Model 3325A Synthesizer/Function Generator. All operations are controlled by the microprocessor in response to commands entered through the front panel or by way of the HP-IB interface.*

grammable from the front panel, and a 1-MHz reference output. The instrument can be phase-locked to any subharmonic of 10 MHz between 1 and 10 MHz and a high-stability oven-controlled reference oscillator is available as an option.

All the functions within this instrument are controlled by a microprocessor, a custom-made 8-bit processor using 16K bytes of read-only memory. This enables a broadened control capability, such as the ability to store and recall up to 10 sets of complete instrument settings, the ability to "tune" the output frequency by incrementing any display digit with up-down step keys as well as by entering a desired frequency with the numerical keypad, and extensive error checking that insures that the selected signal parameters are allowed for the functions chosen. Also, the microprocessor enables the output amplitude to be selected directly in the desired units ($V_{p\text{-}p}$, $V_{rms}$, or dBm/50Ω). Extensive self-test capabilities are also included.

The instrument is also fully programmable through the HP interface bus.* It is thus readily incorporated into HP-IB-linked automatic test systems.

### Instrument Organization

Fig. 2 diagrams how the Model 3325A is organized. The synthesizer section, which uses the single-loop, fractional-N technique, generates an output frequency in a range of 30-51 MHz that is mixed with a 30-MHz crystal-controlled reference to produce an output in a range of 0 to 21 MHz. The 30-MHz reference is also divided down to 100 kHz to serve as the reference for the synthesizer. The mixer output is amplified and then used directly as the sine-wave output or it is used to generate the square, triangle, or ramp functions.

The output level is set by a programmable 10 dB/step attenuator and amplifiers with programmable gain. Analog levels within the instrument are controlled by a multiple output D-to-A converter, to be described later. A peak comparator at the output of the final amplifier is used during an automatic routine to calibrate the output amplitude.

All operations are controlled by the microprocessor, which enhances the versatility and "friendliness" of the instrument. Operating conditions are entered by way of the front-panel keyboard or through the HP-IB interface.

### Fractional-N frequency Synthesis

Fractional-N frequency synthesis is a technique for locking a voltage-controlled oscillator (VCO) to a fractional harmonic of a reference. That is, the oscillator frequency is equal to the number N.F times the reference frequency, where N and F are positive integers.

*The HP interface bus (HP-IB) is Hewlett-Packard's implementation of IEEE Standard 488-1975 and ANSI Standard MC1.1.

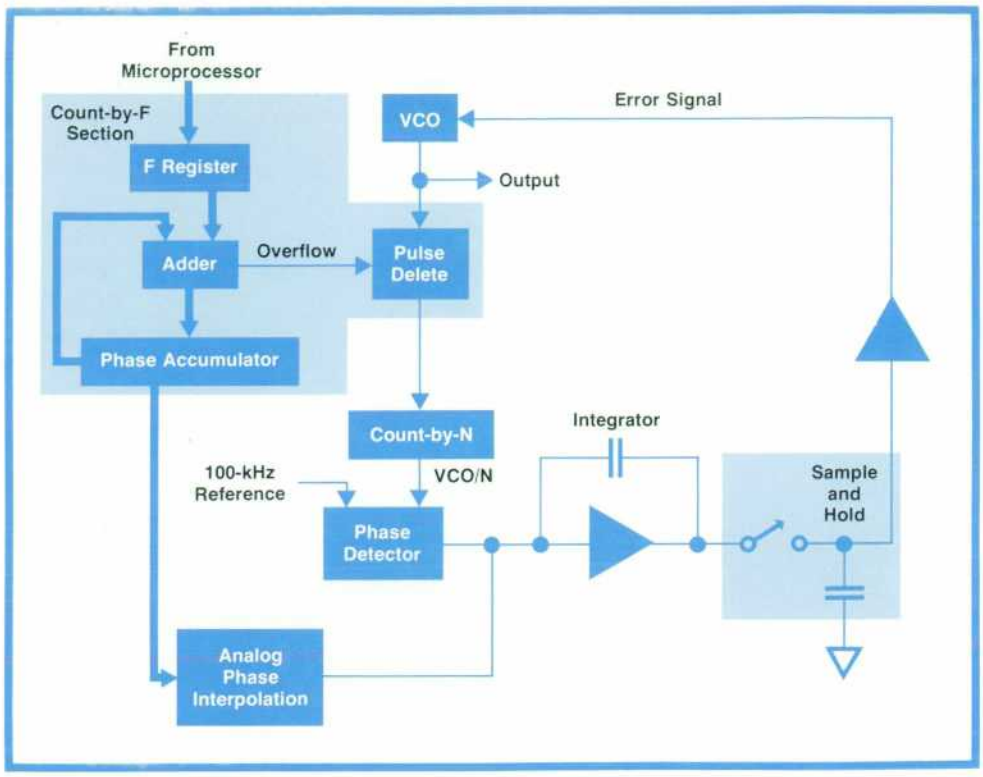



**Fig. 3.** *Simplified block diagram of the fractional-N frequency synthesizer used in Model 3325A. The basic circuit is a conventional count-by-N phase-locked VCO. The count-by-F section implements the fractional division.*

In the Model 3325A, the VCO frequency in the synthesizer is N.F×100 kHz where N is between 300 and 600 and F can be any integer 12 digits long.

A simplified block diagram of the fractional-N frequency synthesizer is shown in Fig. 3. The components of a basic count-by-N phase-lock loop are present. That is, a pulse is sent to the phase detector for every N VCO pulses counted and the phase of this pulse is compared to a 100-kHz reference to derive a phase-error signal for controlling the VCO frequency. Hence, the VCO frequency is N times the reference.

Added to these basic blocks is the count-by-0.F section. The fractional part, F, of the frequency is entered into the F register in BCD form and stored there. Once during each cycle of the 100-kHz reference, the contents of the F register are added to the contents of the phase accumulator. Whenever this addition causes the adder to overflow, one cycle of the VCO output is deleted from the count-by-N input so effectively, N+1 VCO pulses are counted for that particular reference cycle.

As an example, suppose that 0.1 is added to the phase accumulator every reference cycle. The adder then overflows every 10 reference cycles so in one out of 10 reference cycles, N+1 VCO pulses effectively are counted. Thus, when averaged over 10 cycles, N.1 VCO pulses are counted per 100-kHz-reference cycle, so the VCO frequency is N.1×100 kHz.

Note that even when the adder overflows, its contents are transferred to the phase accumulator and so are included in the total during the next reference cycle. For example, if 0.33 were added to the accumulator contents each reference cycle, starting from 0 the adder would overflow in the fourth reference cycle, leaving 0.32 in the accumulator, and then overflow again after three more reference cycles. Averaged over many cycles, the VCO frequency would be N.33×100 kHz.

A salient feature of this technique is that the number of digits synthesized is determined by the number of digits in the F register, which is limited only by hardware considerations. In the 3325A, the frequency resolution is 15 digits, with 11 digits displayed on the front panel.

### Phase Control

The basic count-by-N.F scheme just described requires certain refinements to become a viable technique. For example, cycle removals cause the phase detector to detect a 360° phase error every time a pulse is deleted. To prevent the resulting large transient in the phase-error signal from disturbing the VCO loop, the analog phase interpolation (API) block was added to the circuitry. It anticipates a pulse deletion and makes corrections to the integrator output so large error signals are not transmitted to the VCO (see Fig. 4).

A more detailed diagram of this part of the synthesizer is shown in Fig. 5. The first event that occurs every reference cycle is that the VCO/N pulse from the count-by-N circuit turns on the phase detector current, causing the integrator to ramp up. The next

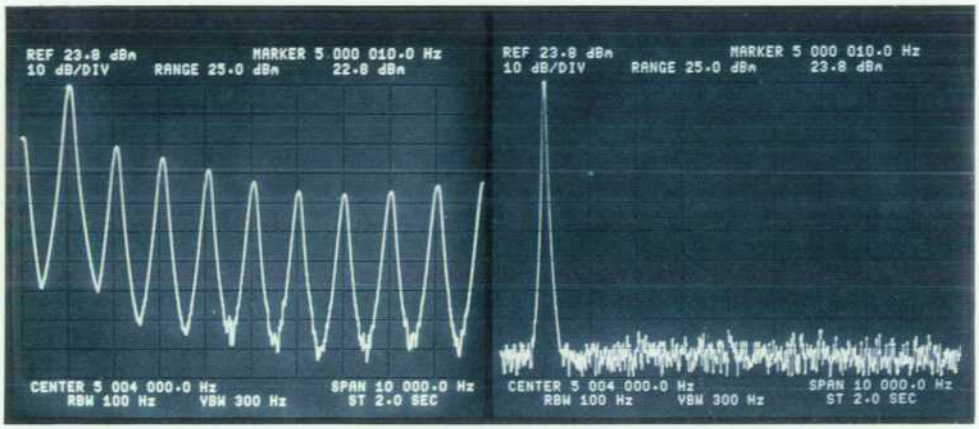



**Fig. 4.** *Spectrum displays show the effect of analog phase interpolation (API). Spurious output frequencies are evident in the photo at left, which shows the spectrum of a 5.001-MHz sine-wave output without the use of API. Photo at right shows the spectrum of the same output with API.*

100-kHz reference pulse turns it off. Thus, the level of the integrator output after the ramp up is proportional to the phase difference between VCO/N and the 100-kHz reference. This level is retained by the sample-and-hold circuit and passed to the VCO. Following the sampling, the bias signal turns on the bias current which ramps the integrator down to the starting level.

When the desired output frequency is not an integral multiple of the reference frequency, the VCO/N pulse gains a fractional part of a cycle with respect to the reference each time it occurs. Thus, until a pulse deletion occurs, the phase detector pulse becomes wider and the integrator ramps up further during each succeeding reference cycle. It is therefore necessary to ramp down further each time so the integrator ramp up will always end at the same level.

The necessary change in ramp-down current is controlled by the API switches which are in turn controlled by the phase accumulator. At the end of each reference cycle, the number stored in the accumulator corresponds to the difference in phase between the VCO/N pulse and the reference. Each of the top five decimal digits of this number controls one of the five API bias switches, and turns on the switch for a period inversely proportional to the numerical value of the digit. The bias current is thus adjusted according to the phase difference.

Since the number in the phase accumulator controls the phase of the VCO through the action of the API currents, the VCO phase can be changed arbitrarily by changing this number. Hence, by adding an increment to the F register for one reference cycle and

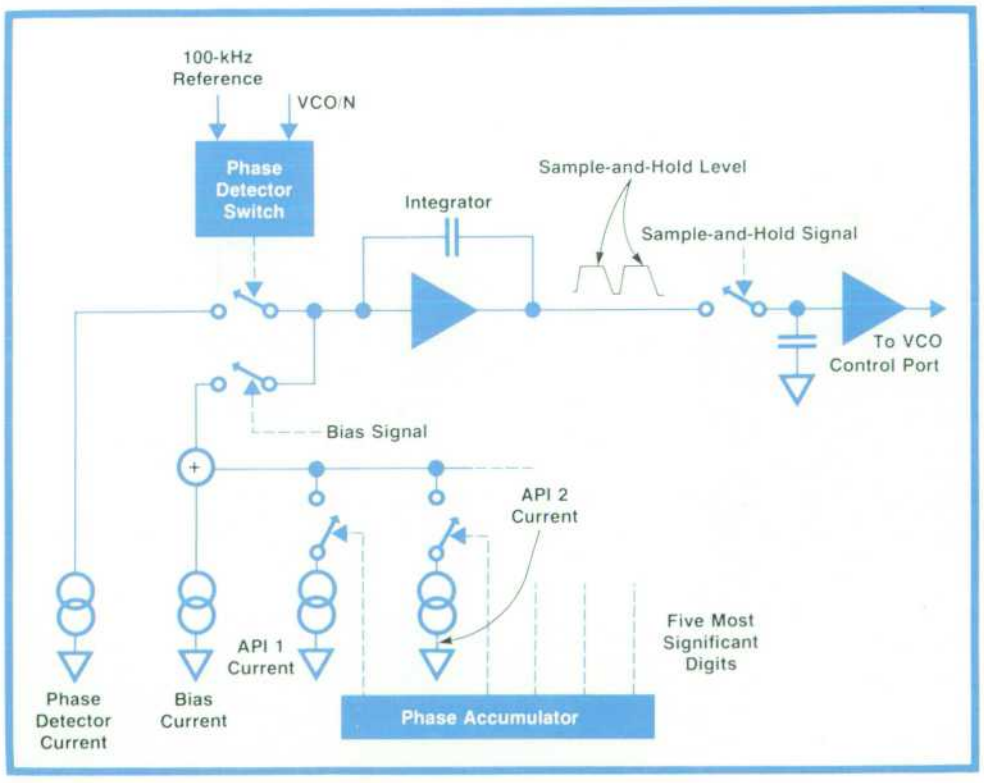



**Fig. 5.** *Details of analog phase interpolation.*

then subtracting it in the next cycle, the output phase is incremented with respect to the reference while the frequency remains unchanged.

Phase modulation is accomplished by converting the phase modulation signal into a current and subtracting this current from the bias current. Phase modulation bandwidth, however, is limited by the bandwidth of the phase-lock loop, which is about 7 kHz.

### Swept Frequencies

Phase-continuous frequency sweep of all functions was made possible by the addition of another register and BCD adder-subtractor to the count-by-0.F section. A frequency increment stored in this register is added to the F register during each reference period to cause the frequency to sweep up. Sweep down is accomplished by subtracting the increment.

The user has control of the start and stop frequencies, choice of linear or logarithmic sweep, and sweep time. The linear sweep has single-sweep and continuous-sweep modes with sweep times between 0.01 and 100 seconds. Total sweep times for single log sweep range from 2 to 100 seconds or 0.1 to 100 seconds for continuous log sweep. X-axis and Z-blank outputs are provided for driving CRTs and X-Y recorders. Also available is a TTL-level marker output that changes state during a linear sweep when the output frequency passes through the selected marker frequency.

Logarithmic sweep is approximated by a succession of linear segments. A new frequency increment is loaded 10 times per decade during single sweeps, or twice per decade in repetitive sweeps (the sweep width must be at least one decade). There is a short pause in the sweep while the microprocessor computes the next frequency increment and as a result, the X-axis output drive signal stops ramping up during the computation intervals. On a CRT display this has the effect of placing brightened vertical bars, which serve as convenient markers (Fig. 6).

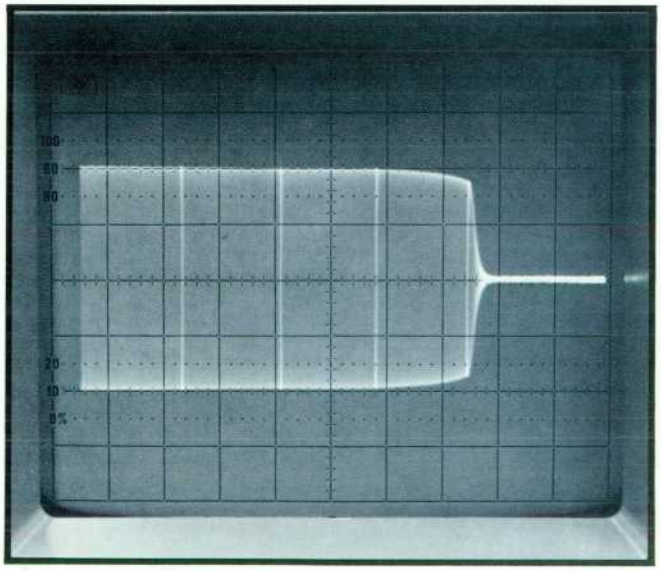


**Fig. 6.** *Logarithmic sweep generates brightened vertical bars as markers (two per decade in the continuous-sweep mode). This oscillogram shows the output of a 500-kHz low-pass filter when the input is swept logarithmically from 5 kHz to 5 MHz.*

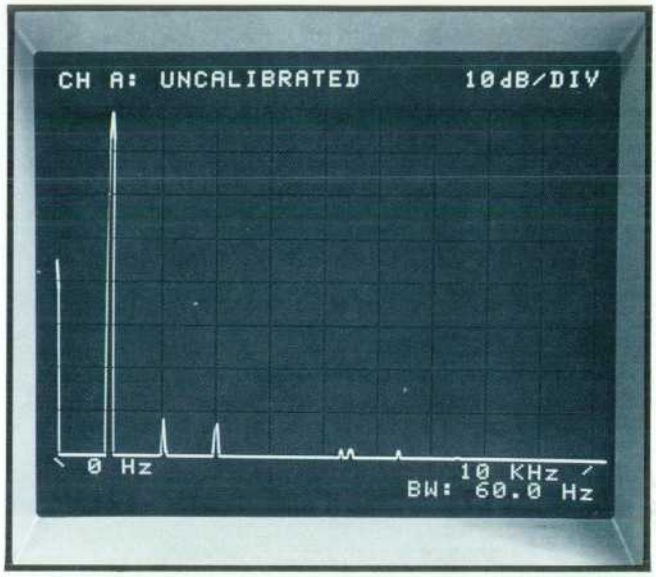



**Fig. 7.** *Spectrum of a typical sine-wave output at 1 kHz and maximum amplitude (into 50Ω) shows the relatively low distortion of Model 3325A at audio frequencies.*

### Fractional-N IC

The cost of the fractional-N digital circuits was reduced significantly by designing them into a custom NMOS integrated circuit. This IC includes the phase accumulator and F registers, timing for the analog circuits, and the adder-subtractor and auxiliary registers for implementing the sweep, but not the high-speed divide-by-N circuitry. It also has a sweep-limit register that signals when a preset frequency is reached during a sweep. This register is used to generate the TTL marker during a sweep or to stop the sweep at a preset limit.

The sweep-frequency register and adder-subtractor, when not being used for the sweep function, are used heavily by the microprocessor during the math routines such as those that derive frequencies and amplitude levels. The microprocessor itself, which is optimized for high-speed control functions, has limited computation capability.

### Waveform Generation

As shown in the block diagram of Fig. 2, the synthesized VCO output is sent to a signal-routing and buffering block. This supplies a 20-to-60 MHz output at a rear-panel connector (frequencies between 20 and

30 MHz are obtained by running the VCO in the 40- to-60-MHz range and dividing its output by two).

The 0-20-MHz sine-wave output is produced by mixing the VCO output with a 30-MHz reference. To keep spurious outputs from the mixer at a low-level, the VCO output drives a monolithic 1-GHz transistor array to derive a fast-switching square wave for use as the local oscillator (L.O.) signal in the mixer. The mixer diodes are in a ring configuration using Schottky diodes in a monolithic quad to achieve good temperature tracking and balance. The typical 2:1 and 3:2 spurious products in the 0-20-MHz range are more than 80-dB below the output signal. Harmonic distortion in the audio range typically is −70 dBc at full output (Fig. 7).

Square waves are generated by using the 0-20-MHz sine wave to drive a Schmitt trigger. This obtains a fast-rise pulse train that is used to drive a ÷2 flip-flop that generates the square wave. This arrangement insures that the square wave is symmetrical. Since it divides the sine-wave frequency by two, the maximum square-wave repetition rate is 11 MHz. Square-wave rise time is 20 ns and the use of dc-coupled output circuits ensures fast settling time ($<1\mu s$ to settle within 0.05% of the final p-p amplitude).

Triangles and ramps are generated by using an exclusive-OR mixing gate and waveforms with offset frequencies. One input to the gate is a fixed, 1-MHz reference square wave, as shown in Fig. 8. The other input is a square wave with a repetition rate 1 MHz higher than the desired output frequency, e.g., for a 10-kHz output this input would be 1.01 MHz. The output of the gate, viewed in the time domain, is the product of the two input waveforms: a rectangular pulse train with a pulse width that periodically widens to 100% and narrows to 0%. A linear-phase, low-pass filter removes the pulse transitions leaving the dc component, a triangular wave.

Looking at this process in the frequency domain, the gate output is the convolution of the spectra of the two square waves, which is the spectrum of a triangle wave with the difference-frequency components centered at 0 Hz and the sum-frequency components centered at 2 MHz. The low-pass filter removes the sum-frequency components.

The reason for generating the triangles this way is the exceptional linearity achieved, better than 0.05% between the 10 and 90% amplitude levels (Fig. 9). This is highly important when using the instrument to check amplifier and A-to-D converter linearity. However the maximum triangle frequency is limited to 11 kHz. If higher frequencies were attempted, the 1-MHz "carrier" frequency would have to be raised and the pulse-train transition times would then become an appreciable part of the pulse waveform, degrading the resulting triangle linearity.

Ramp waveforms are generated similarly except that when the ramp reaches its maximum level, a reset pulse is generated. This inverts the 1-MHz reference square wave, effectively advancing the phase of the reference 180° so the ramp resets to the starting level. Since two ramps occur within the time frame of one triangle, the frequency added to the 1-MHz variable input is one-half the desired output, e.g., for a 10-kHz ramp repetition rate, the variable input would be 1.005 MHz.

Two methods are used to derive the reset pulse for

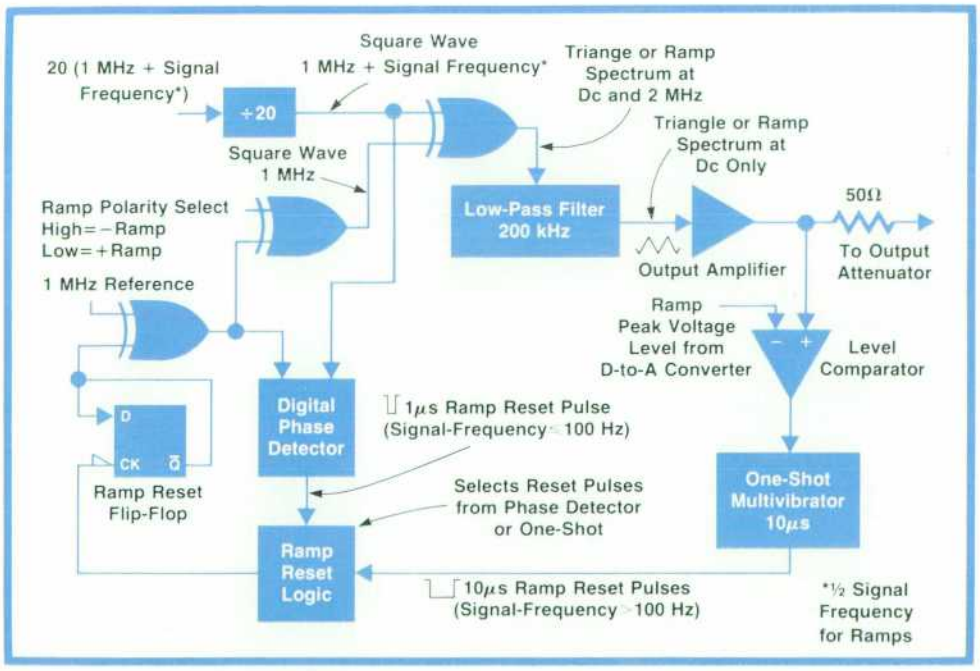



**Fig. 8.** *Circuits that generate the triangle and ramp functions use offset frequencies to obtain high linearity in the output waveform.*

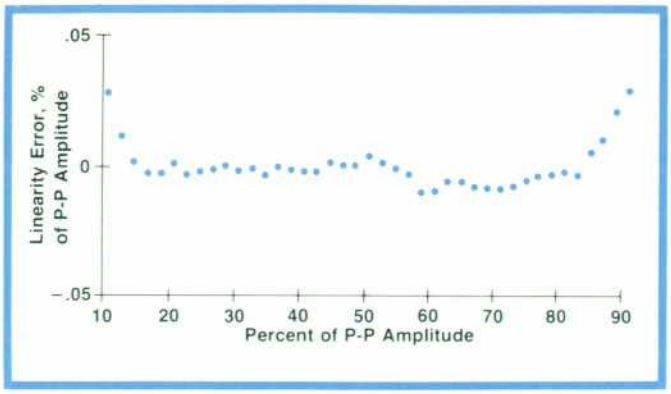



**Fig. 9.** *Typical linearity error of the 3325A triangle wave output. This measurement was made on the positive slope of a 10-kHz, 10-$V_{p\text{-}p}$ triangle wave.*

the ramps. For output repetition rates below 100 Hz, a digital phase detector senses the coincidence of the positive edges of the two square waves feeding the mixing gate. Phase coincidence occurs at the peak of the ramp. For very low frequencies, this gives a very precise indication of the ramp peak, the resolving capability of the phase detector being 1 $\mu$s, or one reference period. However, at output repetition rates above a few hundred hertz, this 1-$\mu$s uncertainty is manifested in an undesirable jitter. Thus, for outputs above 100 Hz, a comparator that fires when the ramp reaches the peak value is used for generating the reset pulse.

### Amplitude and Offset Control

Vernier control of the output amplitude, control of the dc offset, calibration of the amplitude and offset, and control of the X-drive output signal are all effected through a timeshared digital-to-analog converter (DAC). A block diagram is shown in Fig. 10.

The heart of the DAC is the integrator. It ramps up from a known voltage level at a rate fixed by the precision current source for a period of time determined by the preloadable countdown counter. The clock frequency and the number loaded into the counter thus determine what the integrator voltage level will be at the end of the ramp.

The DAC continuously produces six output voltages. The sequence of events for producing any one of them is as follows.

1. The microprocessor controller loads a four-digit BCD number, N, corresponding to the desired output voltage, into the counter.
2. The integrator is reset.
3. The counter and the precision current source are enabled simultaneously.
4. When the counter reaches 0 after counting down N clock pulses, the current source is disabled and the integrator holds at a voltage directly proportional

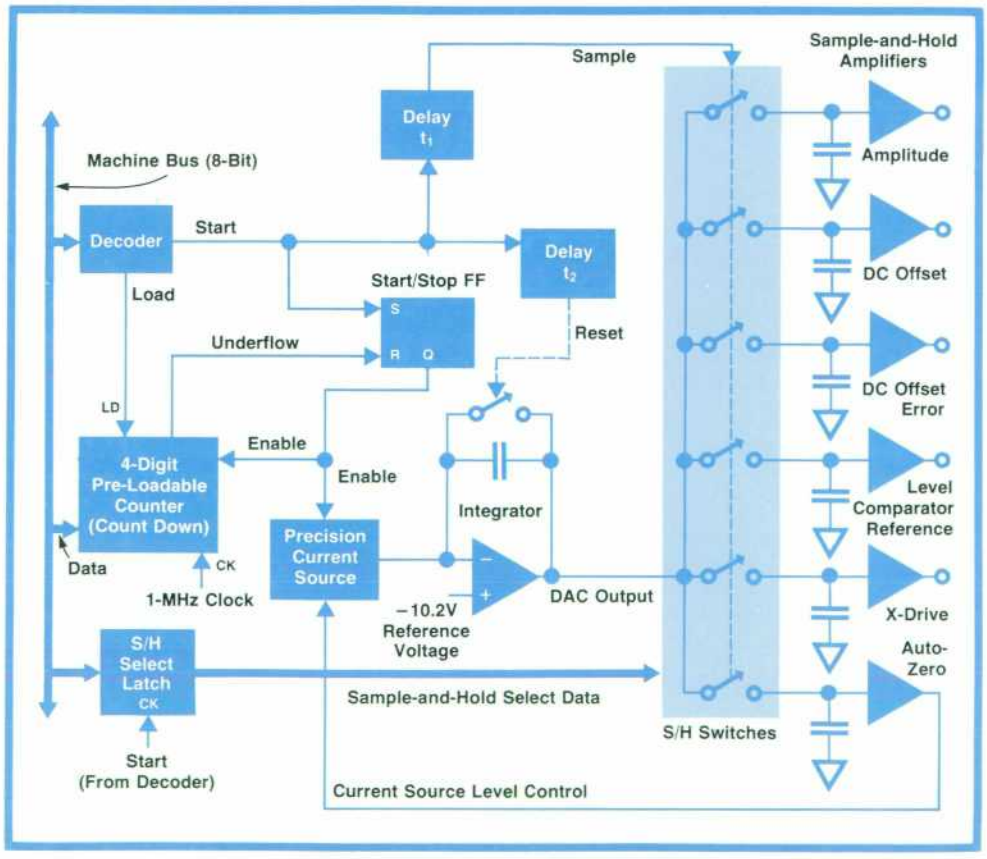



**Fig. 10.** *Time-shared digital-to-analog converter produces six dc voltages.*

to N.

5. The integrator is sampled by the appropriate sample-and-hold amplifier.

The cycle then repeats for the next value. Each cycle requires approximately 1 ms so that each of the six sample-and-hold outputs is updated every 6 ms.

The amplitude and offset control voltages are used to set output waveform amplitudes and offsets. The X-drive control voltage is used as the input voltage to the X-drive integrator. The autozero output is used for zeroing the DAC output. During the autozero cycle, the number that is supposed to generate a zero-level output is loaded into the counter. If the actual output is different from zero, the voltage adjusts the current source in a direction that tends to bring it to zero.

### Amplitude and Offset Calibration

A routine for calibrating the output amplitude and offset levels is executed whenever the instrument is turned on, whenever the output function is changed, whenever the AMPTD CAL button is pressed, and whenever an external controller transmits a device clear or an amplitude calibrate command.

Referring to Fig. 11, the amplitude and offset calibration routine consists of the following steps.

1. The controller attempts to set the signal amplitude and offset to zero.
2. The controller finds the positive and negative peak levels of the resulting output waveform by incrementing the level reference voltage and using the level comparator to indicate when a match is achieved. The average value of the two peaks is the dc offset correction and is subtracted from all subsequent dc offset settings.
3. The controller next attempts to set the signal amplitude to 8 V p-p at 2 kHz.
4. The comparator and level reference voltage are again used to find the positive and negative peaks of the output signal. The ratio of 8V to the measured peak-to-peak value is used to scale all subsequent amplitude settings.

A complete calibration takes about 1.5 seconds and assures offset and amplitude accuracy as good as 1% (see specifications, next page, for details).

### HP-IB

All of the operations of the 3325A may be controlled through the HP-IB. There are two programming modes. In one, the 3325A processes each ASCII character as it is received. Although this mode provides ease of use, it can delay the HP-IB system by causing it to wait while the 3325A processes each character. In the other mode, the 3325A can accept and store a string of up to 48 characters and not attempt to process them until a string terminator is received. The HP-IB controller may thus turn to other tasks while the 3325A processes the character string.

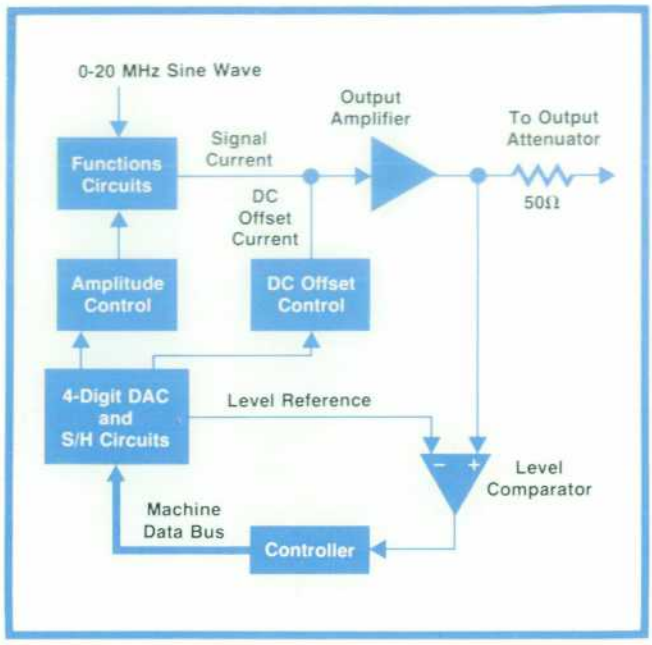



**Fig. 11.** *Circuits involved in the amplitude and offset calibration routine.*

As a convenience feature, the instrument's HP-IB address is displayed when the BUS ADRS button is pressed.

The HP-IB hardware is optically coupled to the function-generating hardware to provide ground-loop isolation.

### Mechanical Construction

Unusual in a synthesizer, the 3325A was designed with an open layout that makes the instrument easy to assemble and service. This also allows the components to remain cool, thereby improving reliability. The only shielding required is for sensitive analog circuits in the VCO and the sine wave mixer. This is done with low cost extrusions that attach to the main circuit board.

Servicing was also simplified by designing the controller for digital signature analysis.[1]


### Acknowledgments

Doug Garde, who was the original project manager, conceived the instrument and designed the synthesizer. Rodger Kahnna and Ron Riedel designed the fractional-N IC. Ron also designed the function circuits. Art Dumont designed the controller hardware and Mike Price did the software. Dennis Faerber handled the mechanical design. Much helpful advice was provided by Ray Hanson and Noel Pace.


### Reference


1. R.A. Frohwerk, "Signature Analysis: A New Digital Field Service Method," Hewlett-Packard Journal, May 1977.

## SPECIFICATIONS

### HP Model 3325A Synthesizer/Function Generator

**WAVEFORMS:** Sine, square, triangle, negative and positive ramps.

**FREQUENCY**

RANGE:
Sine: 1 μHz to 20.999 999 999 MHz.
Square: 1 μHz to 10.999 999 999 MHz.
Triangle/Ramps: 1 μHz to 10.999 999 999 kHz.

RESOLUTION: 1 μHz, <100 kHz.
1 mHz ≥100 kHz.

ACCURACY: $\pm 5 \times 10^{-6}$ of selected value, 20° to 30°C.

STABILITY: $\pm 5 \times 10^{-6}$/year, 20° to 30°C.

WARM-UP TIME: 20 minutes to within specified accuracy.

REFERENCE INPUT: For phase-locking 3325A to an external frequency reference. Reference signal, which must be a subharmonic of 10 MHz from 1 MHz to 10 MHz, can be from 0 dBm to +20 dBm into 50Ω.

**MAIN SIGNAL OUTPUT** (all waveforms)

IMPEDANCE: 50Ω.
CONNECTOR: BNC, switchable to front or rear panel.
FLOATING: Output may be floated up to 42V peak (ac + dc).

**AMPLITUDE** (all waveforms)

RANGE: 1 mV to 10V p-p into 50Ω load in 8 amplitude ranges, 1-3-10 sequence (10-dB steps).

| Function | Sine | | Square | | Triangle/Ramps | |
|---|---|---|---|---|---|---|
| Units Displayed | min | max | min | max | min | max |
| peak-peak | 1.000 mV | 10.00 V | 1.000 mV | 10.00 V | 1.000 mV | 10.00 V |
| rms | 0.354 mV | 3.536 V | 0.500 mV | 5.000 V | 0.289 mV | 2.887 V |
| dBm (50Ω) | −56.02 | +23.98 | −53.01 | +26.99 | −57.78 | +22.22 |

RESOLUTION: 0.03% of full range or 0.01 dB (4 digits).

ACCURACY is the sum of range and attenuator accuracies.

Range Accuracy (percent of each range's maximum p-p output):
Sine and Squarewaves: ±1%, 10 Hz to 100 kHz.
±4%, 100 kHz to 20 MHz (sinewaves only).
Triangles: ±1%, 10 Hz to 2 kHz.
±5%, 2 kHz to 10 kHz.
Ramps: ±1%, 10 Hz to 2 kHz.
±10%, 2 kHz to 10 kHz.

Attenuator Accuracy (percent of output reading displayed, not included when on 3-10V range):
10 Hz to 10 kHz: ±1%, 1 mV to 2.999V.
10 kHz to 10 MHz: ±2%, 1 mV to 2.999V.
10 MHz to 20 MHz: ±2%, 0.1V to 2.999V.
±5%, 1 mV to 99.99 mV.

**SINEWAVE SPECTRAL PURITY**

PHASE NOISE: −54 dB for a 30-kHz band centered on a 20-MHz carrier (excluding ±1 Hz about the carrier).

SPURIOUS: All non-harmonically related output signals will be more than 70 dB below the carrier or less than −90 dBm, whichever is greater.

### Waveform Characteristics

**SINEWAVE HARMONIC DISTORTION:** Harmonically related signals will be less than the following levels (relative to the fundamental) at full output for each range:

| Frequency Range | Harmonic Level |
|---|---|
| 10 Hz to 50 kHz | −65 dB |
| 50 kHz to 200 kHz | −60 dB |
| 200 kHz to 2 MHz | −40 dB |
| 2 MHz to 15 MHz | −30 dB |
| 15 MHz to 20 MHz | −25 dB |

**SQUAREWAVE CHARACTERISTICS:**

RISE/FALL-TIME: <20 ns 10% to 90%, at full output.
OVERSHOOT: <5% of peak to peak amplitude, at full output.
SETTLING TIME: <1 μs to settle to within .05% of final value, tested at full output with no load.
SYMMETRY ERROR: <0.02% of period + 3 ns.

**TRIANGLE/RAMP LINEARITY** (10% to 90%, 10 kHz): ±0.05% of full output for each range.

RAMP RETRACE TIME: <3 μs, 90% to 10%.

### DC Offset

**RANGE:**

DC ONLY (NO AC SIGNAL): 0 to ±5.0 V/50Ω.
DC + AC: Maximum dc offset ±4.5 V on highest range, decreasing to ±4.5 mV on lowest range.

**RESOLUTION:** 4 digits.

**ACCURACY:**

DC only: ±0.006 mV to ±20 mV depending on offset chosen.
Dc + AC: ±0.06 mV to ±60 mV to 1 MHz, ±15 mV to ±150 mV above 1 MHz, depending on ac output level: ±0.02 mV to ±120 mV for ramps to 10 kHz.

### Phase Offset

**RANGE:** ±719.9° with respect to arbitrary starting phase, or assigned zero phase.
**RESOLUTION:** 0.1°.
**INCREMENT ACCURACY:** ±0.2°.

### Sinewave Amplitude Modulation

**MODULATION DEPTH** (at full output for each range): 0-100%.
**MODULATION FREQUENCY RANGE:** Dc - 50 kHz (0-21 MHz carrier frequency).
**ENVELOPE DISTORTION:** −30 dB to 80% modulation at 1 kHz, 0 VDC offset.
**SENSITIVITY:** ±5V peak for 100% modulation.
**INPUT IMPEDANCE:** 20 kΩ.
**CONNECTOR:** Rear-panel BNC.

### Phase Modulation

**SINEWAVE RANGE:** ±850°, ±5V input.
**SINEWAVE LINEARITY:** ±0.5°, best fit straight line.
**SQUAREWAVE RANGE:** ±425°.
**TRIANGLE RANGE:** ±42.5°.
**POSITIVE AND NEGATIVE RAMPS:** ±85°.
**MODULATION FREQUENCY RANGE:** Dc-5 kHz.
**INPUT IMPEDANCE:** 20 kΩ.
**CONNECTOR:** Rear panel BNC.

### Frequency Sweep

**SWEEP TIME:**

LINEAR: 0.01 s to 99.99 s.
LOGARITHMIC: 2 s to 99.99 s single, 0.1 s to 99.99 s continuous.

**MAXIMUM SWEEP WIDTH:** Full frequency range of the main signal output for the waveform in use.

**MINIMUM SWEEP WIDTH:**

| Function | Minimum sweep width: Sweep time .01 sec. | Minimum sweep width: Sweep time 99.9 sec. |
|---|---|---|
| Sine: | 1 mHz | 999.9 mHz |
| Square: | .05 mHz | 499.5 mHz |
| Triangle: | .005 mHz | 49.95 mHz |
| Ramps: | .01 mHz | 99.99 mHz |

Minimum log sweep width is 1 decade.

**PHASE CONTINUITY:** Sweep is phase continuous over the full frequency range of the main output.

### Auxiliary Outputs

**AUXILIARY FREQUENCY OUTPUT:**

FREQUENCY RANGE: 21 MHz to 60.999 999 999 MHz, underrange coverage to 19.000 000 001 MHz, frequency selection from front panel.
AMPLITUDE: 0 dBm.
OUTPUT IMPEDANCE: 50Ω.
CONNECTOR: Rear-panel BNC.

**SYNC OUTPUT:** Square wave with $V_{high}$ >1.2V, $V_{low}$ <0.2V into 50Ω.
FREQUENCY RANGE: Same as main signal output.
OUTPUT IMPEDANCE: 50Ω.
CONNECTOR: BNC front and rear panels.

**X-AXIS DRIVE:** 0 to +10V dc linear ramp proportional to sweep frequency, 0.1% linearity, 10-90%. Rear-panel BNC connector.

**SWEEP MARKER OUTPUT** (linear sweep only): High to low TTL-compatible voltage transition at keyboard-selected marker frequency. Rear-panel BNC connector.

**Z-AXIS BLANK OUTPUT:** TTL-compatible voltage levels capable of sinking current from a positive source. Current 200 mA, voltage 45V, power dissipation 1 watt maximum. Rear-panel BNC connector.

**1-MHZ REFERENCE OUTPUT:** 0-dBm output for phase-locking additional instruments to 3325A. Rear-panel BNC connector.

**10-MHZ REFERENCE OUTPUT:** 0-dBm output for phase-locking 3325A to the internal high stability frequency reference (Opt. 001). Rear-panel BNC connector.

### HP-IB Control

**FREQUENCY SWITCHING TIME** (to within 1 Hz, exclusive of programming time): <10 ms for 100-kHz step; <25 ms for 1-MHz step; <70 ms for 20-MHz step.

**PHASE SWITCHING TIME:** <15 ms to within 90° of phase lock, exclusive of programming time.

**AMPLITUDE SWITCHING AND SETTLING TIME:** <30 ms to within amplitude accuracy specifications, exclusive of programming time.

### Option 001 High Stability Frequency Reference

**AGING RATE:** $\pm 5 \times 10^{-8}$/week, $1 \times 10^{-7}$/mo.

**ACCURACY:** $\pm 5 \times 10^{-8}$ (0° to +50°C).

**WARM-UP TIME:** Reference will be within $\pm 1 \times 10^{-7}$ of final value 15 minutes after turn-on at 25°C for an off time of less than 24 hours.

### Option 002 High Voltage Output

**FREQUENCY RANGE:** 1 μHz to 1 MHz.

**AMPLITUDE:**

RANGE: 4.000 mV p-p to 40.00 V p-p (500Ω, <500 pF load).
ACCURACY: ±2% of full output for each range at 2 kHz.
FLATNESS: ±10%.

**SINEWAVE DISTORTION:** Harmonically related signals will be less than the following levels (relative to the fundamental full output into 500Ω load):
10 Hz - 50 kHz: −65 dB
50 kHz - 200 kHz: −60 dB
200 kHz - 1 MHz: −40 dB

**SQUARE-WAVE RISE/FALL TIME:** <100 ns, 10% to 90% at full output, with 500Ω 500-pF load.

**SQUARE-WAVE OVERSHOOT:** <10% of peak-to-peak amplitude with 500Ω, 500-pF load.

**OUTPUT IMPEDANCE:** <2Ω at dc, <10Ω at 1 MHz.

**DC OFFSET:**

RANGE: 4 times specified range of standard instrument.
ACCURACY: ±(1% of full output for each range + 25 mV).

**MAXIMUM OUTPUT CURRENT:** 40 mA p-p.

### General

**OPERATING ENVIRONMENT:**

TEMPERATURE: 0°C to 55°C.
RELATIVE HUMIDITY: 95%, 0°C to 40°C.
ALTITUDE: <15,000 ft.

**POWER:** 100/120/220/240V, +5%, −10%; 48 to 66 Hz; 60 VA, 100 VA with all options; 10 VA standby.

**WEIGHT:** 9 kg (20 lb).

**DIMENSIONS:** 132.6 mm H × 425.5 mm W × 497.6 mm D (5¼ × 16¾ × 19⅝ in).

**PRICE IN U.S.A.:** $3000. High-stability frequency reference, $550. High Voltage Output, $200.

**MANUFACTURING DIVISION:** LOVELAND INSTRUMENT DIVISION
815 Fourteenth Street, S.W.
Loveland, Colorado, 80537 U.S.A.

---

**Stanley E. Froseth**

An HP employee since 1976, Stan Froseth was responsible for portions of the analog design and high voltage output option design of the 3325A Synthesizer/Function Generator. He was born in St. Paul, Minnesota, and is a 1974 BSEE and 1976 MSEE graduate of the University of Minnesota. Stan is also the author of several papers related to environmental noise, one of which was published in the *Journal of Sound and Vibration*. A member of the Loveland Environmental Quality Commission, Stan also spends much of his spare time bicycling, playing tennis, crosscountry skiing, and backpacking. Residents of Loveland, Colorado, Stan and his wife have no children, but enjoy life at home with their dog and seven cats.

**Dan D. Danielson**

Born in Grand Junction, Colorado, Dan Danielson joined HP's Loveland Instrument Division in 1972, shortly after receiving his BSEE degree from the University of Colorado. He began work as designer of the output amplifier and modulation generator for the 3312A Function Generator and then worked on the design of the synthesizing, mixer, and reference circuits for the 3325A Synthesizer/Function Generator. A resident of Loveland, Colorado, Dan is single and enjoys skiing, golfing, and backpacking in his leisure time.

# Viewpoints

## Paul Baird on Electronic Equipment Reliability

Many of our modern electronic products are feasible because advances in reliability accompanied those of technology and invention. Computers, for example, made relatively slow progress until semiconductors replaced vacuum tubes. Then prices came down while reliability improved greatly.

Reductions in price for a given performance have tended to mask the improvements in reliability that are taking place. The reason is that we commonly look at the cost of maintaining a product as a percentage of its original price. Thus the manufacturer is kept under constant pressure to meet customers' expectations with regard to reliability. Actually, this is healthy since, by meeting those expectations, powerful new products can win acceptance.

### In Search of Reliability

Reliability can be defined as the probability that a randomly selected product will successfully complete an assigned mission. It depends upon product robustness, mission stresses, mission duration, and product age (history).

It is fairly common practice among those concerned with electronic equipment to ignore the effects of product aging and use mean-time-between-failures (MTBF) as the measure of reliability. With such a model the reliability of a repaired product is no better or worse than that of one that has never failed.

This isn't quite true—most products become more reliable with age, at least for several years.

Also, because of the applicable mathematical relationships, most engineers prefer to key their discussions on failure rate, denoted $\lambda$, rather than upon MTBF. The probability that a product will fail in a time $\Delta T$ is approximated by $\lambda\Delta T$ so that the smaller $\lambda$ is, the more reliable the product is. Additionally, for nearly all products (excepting those where redundancy techniques can be justified), $\lambda_{product} = \Sigma\ \lambda_{devices}$. These relationships hold whether or not $\lambda$'s are time dependent, so we have left open our option to use sophisticated models for $\lambda$ if we choose to do so. Additionally, if the product $\lambda$ does not change much with aging we can state MTBF = $1/\lambda_{product}$.

Since it is normally true that $\lambda_{product} = \Sigma\ \lambda_{devices}$ the use of more devices means a higher failure rate *unless* certain countermeasures can be implemented. These countermeasures are extremely important and are the subject of the following discussion.

### In the Design Phase

Although nearly all field failures appear to be caused by a device, most are design- or manufacturing-controllable. The graphs below illustrate how product failure rate can be expected to vary as a function of certain design-controllable factors. As the graphs show, large design margins result in smaller $\lambda$'s since the product will not be very sensitive to drift in device parameters (design margins are easily checked by non-destructive perturbation of internal variables, such as supply voltages, noise, clock rates, etc.). An improved technology may increase the design margins and it may also reduce the number of devices, resulting in lower $\lambda$'s. Error correction involving redundancy, though effective, is practical at present only in very complex digital products. However, reducing temperature and electrical stresses can be particularly effective countermeasures because $\lambda$ is very sensitive to these stresses. Through application of these relationships, the designer can have a powerful influence on the resulting product reliability.

### Materials Management

There is a residual set of potential failures that are best controlled by device selection. Vendors frequently offer more than one level of quality so some control is possible by this means. Then too, the quality of a device varies from vendor to vendor and sometimes from the same vendor at different times. Thus, qualifying a vendor, such as destructive stress testing of device samples and use of incoming shipment acceptance procedures through some form of inspection, are quite important. Vendors also do better as they gain experience with their own products.

Experience has shown that the failure rates of most devices improve with age, even over a span of several years. Thus, another way to improve $\lambda$ is to accelerate the normal aging process, usually referred to as burn-in.

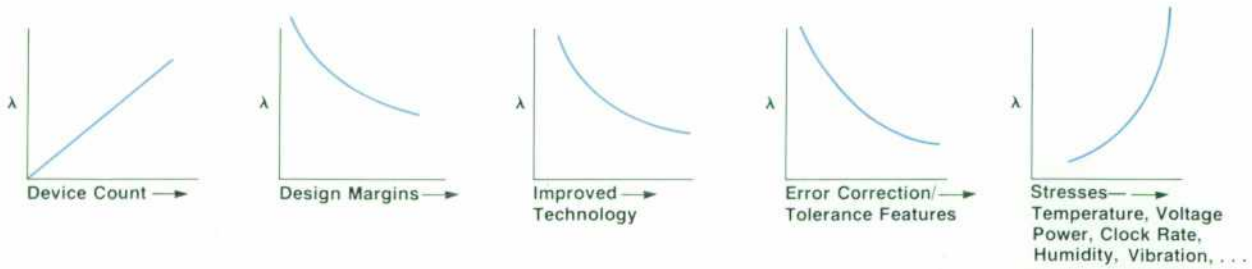
### Manufacturing

Following the selection of materials, some control over product $\lambda$ is exerted by the manufacturing process. The manufacturing task is to avoid workmanship flaws. Some of these may be latent, allowing the product to work long enough to pass final inspection. Workers basically want to do a good job so enlistment of their active support through attention to their needs has a positive effect. Proper training is also important. Motivation and training produce best results, however, when proper tools are available. As an example, many HP divisions have electronic tools that check the tolerance of each component *after* it is loaded on a printed-circuit board to assure that it is still within tolerance following the mechanical stresses of insertion and the heat stresses of soldering.

### After-Sale Support

Service support is a crucial item in how users *feel* about product reliability. If repair turnaround times are short and the cost per repair is low, customers tend to feel as if $\lambda$ were lower than it really is. Since turnaround time and cost often conflict, service strategies are often devised according to the product type. Computers, for example, are usually serviced on-site because of the economic importance of very fast turnaround time in this area.

Customer training can reduce "cockpit" errors that lead to downed instruments. Good operating and service manuals also have a positive influence here. In addition, implementation of proper preventive maintenance can reduce some types of hardware failures.



### Active Product Assurance

Reliability is only partly technology-limited. It is also likely to be limited by cost tradeoffs and by attention to detail in competititon with other work objectives, so it is highly influenced by management commitment to reliability.

To achieve low λ in their products, many companies are willing to commit the resources needed to establish product assurance departments. At Hewlett-Packard, product assurance managers, most of whom have had broad experience in other departments, provide the following services:

- To act as a participant or else catalyst in the tasks already named.
- Act as a conscience.
- Provide information relative to quality and reliability.
- Assure that somehow the proper things are happening.
- Do quality and reliability engineering.
- Assure compliance with the product safety and electromagnetic compatibility regulations of the various nations where HP products are sold.

Some of the major assurance techniques involved are listed here:

| Area | Techniques | |
|---|---|---|
| Design | environmental testing | margin testing (Shmoo plots) |
| | life testing | component stress analysis |
| | setting goals | failure rate estimation |
| | | anticipating abuses |
| Materials | stress testing | process change reviews |
| | component screening | incoming inspection |
| | failure analysis | vendor performance tracking |
| | | specifications |
| Manufacturing | sales inspection | production failure analysis |
| | warehouse audits | environmental requalification |
| | warranty analysis | process control |
| | control charts | metrology |
| Service | control of turnaround time | control of mean time to repair (MTTR) |
| | delivery time of spare parts | audits of instruction manuals |
| | customer training | information feedback |

### Results

Looking ahead we expect to benefit from both statistical and physical approaches to reliability. Statistics help set priorities by quantifying problems and relationships. At HP, very complete records are kept of warranty information about each serialized product, detailing such items as ship dates, fail dates, repair office, labor hours, turnaround time, a list of parts replaced (with failure codes), total cost of repair, and free-form comments by the customer engineer.

Very useful analyses can be derived from this data base to pinpoint troublesome models, components, or geographical areas. Data is even complete enough to fit time-dependent Weibull failure models to both products and components, which is done regularly.

After statistical definition of top problems we can concentrate upon understanding the fundamental relationships in terms of physics, chemistry, manufacturing processes and design stresses. Most of HP's major divisions are devoting resources to high-stress experiments on components followed by failure analysis of devices that don't pass. Electromigration, for example, is a failure mechanism now pretty well understood and controlled. On a selective basis, failure analysis is also done on devices failing in environmental tests, life tests, the factory floor, or in field use. Where practical, results are shared on a company-wide basis. We have, for instance, an ALERT system that can be activated by any division to warn the others of a possible problem. The ALERT also contains a recommendation for dealing with the situation. As a result, some problems are disappearing.

Reliability excellence in a product results from care in the design of the product, in the choice of materials, and in the manufacturing processes, like the links in a chain. The weakest link determines how the product will eventually fail, so careful attention must be paid to all. Recent trends have been toward a reduction of both product failure rates and costs and further improvements can be expected.

*Paul Baird, HP's Corporate Assurance Engineering Manager, is involved in product assurance R and D and in coordinating product assurance activities at HP's far-flung divisions. He is a senior member of the American Society for Quality Control. With HP since 1961, Paul was involved in voltmeter design for many years. He has a BS in mathematics from Oklahoma State University (1950), an MSEE from the University of Colorado (1953) and an Engineer degree from Stanford University (1959).*

Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, California 94304

HEWLETT-PACKARD JOURNAL

**JANUARY 1979** Volume 30 • Number 1

**Technical Information from the Laboratories of Hewlett-Packard Company**

Hewlett-Packard Company, 1501 Page Mill Road
Palo Alto, California 94304 U.S.A.
Hewlett-Packard Central Mailing Department
Van Heuven Goedhartlaan 121
Amstelveen-1134 The Netherlands
Yokogawa-Hewlett-Packard Ltd., Suginami-Ku
Tokyo 168 Japan

**Editorial Director • Howard L. Roberts**
**Managing Editor • Richard P. Dolan**
**Art Director, Photographer • Arvid A. Danielson**
**Illustrator • Susan E. Wright**
**Administrative Services, Typography • Anne S. LoPresti**
**European Production Manager • Dick Leeksma**



CHANGE OF ADDRESS: To change your address or delete your name from our mailing list please send us your old address label (it peels off). Send changes to Hewlett-Packard Journal, 1501 Page Mill Road, Palo Alto, California 94304 U.S.A. Allow 60 days.