An Enhancement-Mode PHEMT for Single-Supply Power Amplifiers

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To address the growing handset power amplifier needs for the emerging Personal Communications Services (PCS) markets, a 3-volt, single-supply, enhancement-mode pseudomorphic high-electron-mobility transistor (E-PHEMT) has been developed. The device exhibits +33-dBm output power and 65% drain efficiency at 1.88 GHz.

PCS telephone handset manufacturers have had to face some tough choices to find the most suitable technology for their output power amplifiers. Most manufacturers would prefer to use an amplifier that operates on the 3.0V to 3.6V provided by three nickel-cadmium battery cells or one lithium-ion battery cell.

However, GaAs MESFETs (metal-semiconductor field effect transistors) or PHEMTs (pseudomorphic high-electron-mobility transistors) capable of meeting this need have also required an additional negative voltage supply for proper biasing. Alternatively, a manufacturer could choose a single-supply amplifier using silicon bipolar junction transistors, GaAs heterojunction bipolar transistors, or silicon MOSFETs (metal-oxide-semiconductor field effect transistors). These devices typically require a supply voltage around 4.8V, and to use them the manufacturer would have to raise the battery voltage or use a dc-to-dc converter. All of these approaches have efficiency, size, complexity, or cost trade-offs that manufacturers would prefer not to accept if a better device technology were available.

To address this need, an enhancement-mode PHEMT (E-PHEMT) has been developed that provides excellent performance using a single 3V supply. In this paper, the original enhancement-mode technology development by HP Laboratories is presented, followed by device development work performed at the HP Communication Semiconductor Solutions Division (CSSD). RF performance results of both a process control monitor device and a 12-mm gate

periphery device are discussed, and a comparison of E-PHEMT performance with other device technologies highlights the merits of this technology. Preliminary device reliability and qualification test results are presented, and test results from a low-cost, plastic packaged, 12-mm gate periphery transistor are discussed.

Development at HP Laboratories

HP Laboratories has been developing an enhancement-mode field effect transistor (EFET) to improve the speed of driver devices in enhancement/depletion-type digital circuitry. This type of device offers two special benefits in handset power amplifier circuitry. Firstly, an EFET only requires positive bias voltage, and can be turned off with zero volts on the gate, but conducts current with positive voltage applied to the gate. Since the drain of a PHEMT is also biased with positive voltage, eliminating the need for negative gate voltage (required for the conventional depletion-mode FET, or DFET) would simplify the operation of the PHEMT.

Secondly, because of the requirement to deliver maximum current over a small gate voltage swing (~1 volt), a correctly designed EFET inherently has higher transconductance (g_m), and, more important for class-B power FET operation, better g_m linearity than a conventional DFET. The HP Laboratories' approach employs molecular beam expitaxy (MBE) to place a highly doped, thin electron donor layer close to the gate, with the electron donors on both sides of the $In_{0.2}Ga_{0.8}As$ channel. Highly selective reactive ion etching is used to define the vertical position of the Schottky gate. **Figure 1** is a schematic diagram of the MBE layer structure of the enhancement mode PHEMT.[1]

Figure 1

Schematic diagram of the MBE layer structure of the enhancement-mode PHEMT.

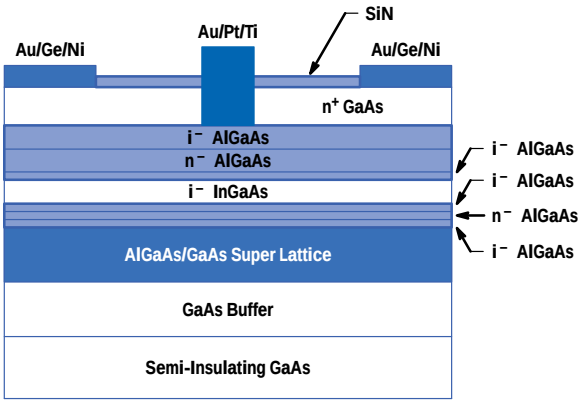


Table I summarizes the key characteristics of HP Laboratories' enhancement-mode self-aligned contact (SAC) PHEMT. An important point is that the maximum current achieved is no less than that of similarly fabricated depletion-mode PHEMTs, and is far higher than that of typical MESFETs.

To explore the potential of HP Laboratories' enhancement-mode SAC PHEMT as a handset power device, a large-signal model was extracted from 100-μm gate width devices. An extensive HP Microwave Design System simulation was performed for both analog and digital handset applications. Table II summarizes the simulated results for both two-tone input (digital modulation) and one-tone input (analog modulation).

Table I
Key Characteristics of HP Laboratories' E-PHEMT

Parameter	Unit	Conditions	Typical Wafer Mean	Typical Wafer σ
Threshold Voltage	V	$V_d = 2V$	0.06	0.04
Maximum Transconductance	mS/mm	$V_d = 2V$	708	57
Maximum Drain Current	mA/mm	$V_d = 2V$, $I_g < 100$ mA/mm	515	36
f_T	GHz	optimum	60	
f_{max}	GHz	optimum	120	

Table II
Power Performance of E-Mode SAC PHEMT

Parameter*	Unit	Specification	Simulation Results
2-Tone Power Out	dBm	28.5	28.5
Power-Added Efficiency @ 28.5 dBm	%	> 50	53
Gain @ 28.5 dBm	dB	> 15	19.6
IM3 @ 28.5 dBm**	dBc	< −26	−40
IM5 @ 28.5 dBm**	dBc	< −36	−37
IM7 @ 28.5 dBm**	dBc	< −45	−45
1-Tone Power Out	dBm	31.5	31.5
Power-Added Efficiency @ 31.5 dBm	%	> 60	71.6
Gain @ 31.5 dBm	dB	> 15	19.5
Quiescent Current	mA		145
Gate Width	mm		8.6

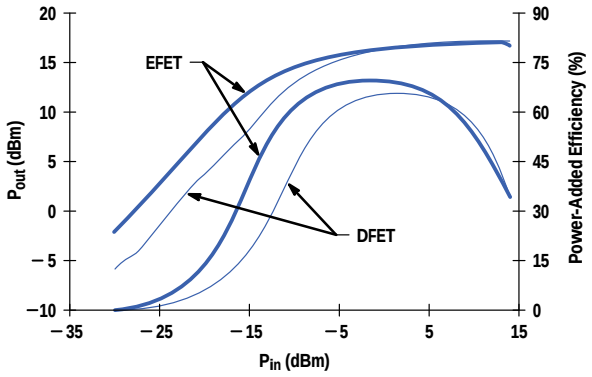
* Test Condition: 900 MHz and V_d = 3V
** Intermodulation (IM) distortions have been calculated for two tones spaced by 5 kHz at 900 MHz.

The very encouraging simulated results prompted the HP Communication Semiconductor Solutions Division (CSSD) to further examine HP Laboratories' enhancement-mode SAC PHEMT. Load-pull measurements at 2 GHz performed on 100-μm gate width devices indicated 13.4-dBm (219-mW/mm) power, 19.4-dB gain and 75.3% power-added efficiency at V_d = 3 volts. Since these results exceeded the anticipated product specifications by significant margins, a strategy was formulated to make available a first-generation product based on a simpler, nonself-aligned process.

Figure 2 shows the power performance at 2 GHz of 200-μm gate width DFETs and EFETs fabricated at CSSD with a nonself-aligned process. Although the performance was not as good as HP Laboratories' self-aligned FETs, the 223-mW/mm saturated power and 66% power-added efficiency exhibited by these devices at $V_d = 3$ volts are still state-of-the-art. **Figure 2** also clearly establishes the superior gain and efficiency of EFETs compared to DFETs at low input power.

Figure 2

Comparison of the power performance of EFETs and DFETs. Gates are 200 μm wide and 0.2 μm long. Gates and contacts are not self-aligned to each other.



The power measurements taken on EFETs and DFETs, which are processed the same way, also dispell another concern of employing EFETs for power amplification: that EFETs will draw unusually large gate leakage current in power saturation. From the load-pull measurements done for the data shown in **Figure** 2, the quiescent gate leakage current at 3-dB gain compression is positive and < 1 mA for the EFET, and is negative and < 1 mA for the DFET.

With the groundwork at HP Laboratories clarifying the potential of an enhancement-mode power PHEMT, a project was launched at CSSD and the results from that project are described in the remainder of this article.

Development at CSSD

For the 3-volt, enhancement-mode, high-gain power transistor, one has to investigate candidate devices to determine their potential for low knee (saturation) voltage, high transconductance at low quiescent current, and high current supply capability. High transconductance at low current gives better linearity when the device is operated at low currents in high-linearity applications, and high current capability leads to better power output. The 3-volt operation favors PHEMTs because the PHEMT drain current saturates at very low voltages (low knee voltage). This allows greater dynamic voltage swing. In addition, the high electron mobility of PHEMTs provides high gain and high current. Pseudomorphic HEMTs are fabricated on GaAs substrates using MBE.

Discrete devices were fabricated with several different MBE material profiles. To evaluate these devices, on-wafer small-signal data and load-pull data was collected on small devices, while RF circuit evaluation was done on large devices of 12-mm total gate periphery. The quick turnaround of the on-wafer measurements speeded the optimization of MBE material structures. Circuit evaluation and load-pull data on 12-mm devices further validated the small-signal results. CSSD's implementation of the material structure from HP Laboratories (the enhancement-mode PHEMT originally for digital applications) initially showed poor performance. After material growth optimization with the help of HP Laboratories, performance improved dramatically and a final structure was adopted for the project.

This demonstrates the problems that can occur in technology transfer, since the material growth and processing conditions used at HP Laboratories needed to be adapted and modified to run on the different equipment and processes used at CSSD. Through close collaboration with HP Laboratories, high-quality E-PHEMT epitaxial material is now routinely grown at CSSD. Wafer processing was refined and adapted to the standard PHEMT process used in the CSSD GaAs fabrication facility.

Device Layout

Key factors that determine the best device layout are total current capability, frequency response, cost, thermal dissipation, and specific performance requirements. A power transistor consists of an array of interdigitated source and drain pads separated by gate fingers, essentially a combination of small unit cells. The total current available is determined by the product of the number of fingers and the width of each finger. The current capabiity of a PHEMT also varies with the material structure, and the goal is to have the current necessary for a specified power output in the smallest device possible. To evaluate device layout trade-offs, a mask was generated with eight devices having different geometries.

For better response at higher frequencies, the width of the individual fingers of the transistor needs to be smaller. Finger widths range from 200 to 400 μm for the eight devices. The wider the fingers, the more symmetric the device aspect ratio, the better the real estate utilization, hence the lower the device cost, a typical trade-off of cost versus performance. On a microwave transistor, the bonding pads often occupy half the device. On this mask set, the cost of some devices was reduced by having separate narrow source bonding pads instead of a large conventional one-piece source pad surrounding all the gate pads.

Within each device, in addition to the gate finger width, the gate length (the narrow dimension of the gate) sets the upper limit of the frequency of operation. For the PCS/PCN frequency bands, 0.5-μm gate length is suitable, and has been adopted in the present project.

Fabrication Process

The wafer processing uses the standard CSSD PHEMT process. Fabrication of an enhancement-mode PHEMT requires some precaution. The gate metal needs to be placed just on top of the upper undoped AlGaAs layer to achieve zero-volt threshold operation. Since the active channel of the device lies very close to the exposed top surface, inadvertent exposure to some chemical solutions during processing can erode the channel, resulting in nonuniformity and current loss. With conventional chemical wet etching of 10-nanometer-thick layers, nonuniformity is inevitable. Fortunately, the composition of the different layers lends itself to a selective plasma reactive ion etching process that is self-stopping at the top AlGaAs layer.

After isolating the active area of the transistor with proton implantation, ohmic contacts to the source and drain pads are deposited. Then the gate opening is delineated in photoresist and the wafer placed in a reactive ion etcher to remove the top GaAs layer from the gate opening region. Immediately afterwards, multilayer metal is evaporated onto the wafer to form the gate electrode. Excess metal is lifted off by removing the photoresist in solvent. Wafer passivation is achieved using plasma silicon nitride. A final gold plating step forms the “air-bridge” interconnect metal (second metal), which links the individual fingers of the transistor array through bridges arching over bus bars underneath.

Process Control Monitor Device Performance

The current-voltage (I-V) characteristics of a 60-μm ($L_g = 0.5$ μm), double-doped E-PHEMT process control monitor device are shown in **Figure 3**.

Typical dc results are as follows. The drain-source saturation current density (I_{dss}) measured at $V_{ds} = 3$ volts is less than 10 mA/mm. The maximum drain current density (I_{max}), measured at $V_{gs} = 0.8$ volts and $V_{ds} = 3$ volts is greater than 300 mA/mm. The maximum transconductance (g_m) is greater than 370 mS/mm. The gate-to-drain breakdown voltage (BV_{gdo}) measured at a gate current of 0.5 mA/mm is more than 10 volts. The pinch-off voltage (V_p) measured at $V_{ds} = 2$ volts and drain current density of 2 mA/mm, is 0 volts. The knee voltage, defined as the drain-source bias when

Figure 3

The I-V characteristics of a 60-μm process control monitor device.

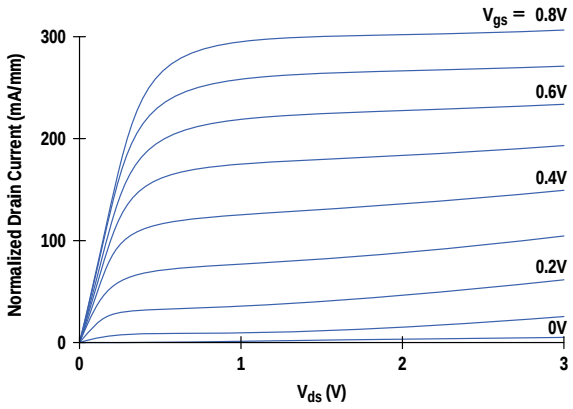
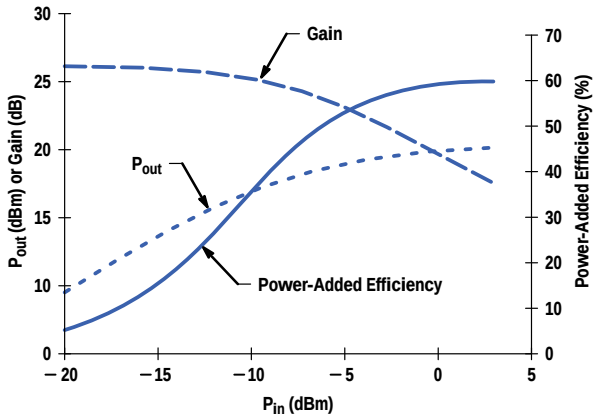


Figure 4

The power saturation characteristics of the 300-μm process control monitor device at 3 volts and 2 GHz.



the drain-source current density becomes 200 mA/mm with V_{gs} equal to 0.8 volt, is 0.3 volt. The on-resistance, measured at $V_{gs} = 0.8$ volt, is 1.5 ohms-mm.

The small-signal parameters of the 60-μm devices were measured on-wafer using an HP 8510C automatic network analyzer. Based on the s-parameter results, the unity-current-gain frequency (f_T) for $V_{ds} = 3$ volts and $I_{ds} = 20$ mA is calculated to be 36 GHz. The maximum available gain/maximum stable gain at 2 GHz is 22 dB under the same bias condition.

The large-signal performance of the process control monitor devices was also monitored on-wafer using an automatic load-pull system. The large-signal characteristics were measured at $V_{ds} = 3$ volts and $I_{ds} = 20$ mA. With fixed input power, the system sets the input impedance to provide maximum small-signal gain, and then tunes the load impedance for maximum gain, maximum power, and maximum efficiency.

The power saturation characteristics for a 300-μm device under the maximum output power tuning are shown in **Figure 4**. The device exhibited an output power of 16.4 dBm at the 3-dB gain compression point with 3-volt bias at 2 GHz, corresponding to a power density of 140 mW/mm. In addition, the device demonstrated a saturated output power of 18 dBm, power-added efficiency of 60%, and power gain of 13 dB, which corresponds to a power density of 210 mW/mm.

12-mm Device Performance

The next step in the E-PHEMT development project was to measure the performance of a large device that could actually be used as the output stage in a PCS telephone. The power device used for this evaluation was a 0.5-μm gate length and 12-mm (330-μm × 36-finger) gate periphery E-PHEMT. The layout of the device is shown in **Figure 5**.

The power performance of the 12-mm E-PHEMT was measured with a drain bias of 3 volts and a quiescent drain current of 100 mA ($V_{gs} = +23$ mV) at 1.8 GHz. To improve yield and reduce cost, the wafer was lapped to a thickness of 0.004 inch with no via grounding. The device was then eutectically mounted onto a metal carrier, and two ceramic probe adapters, which provide the coplanar-to-microstrip transition, were placed at the input and output of the device (**Figure 6**). Bond wires were used to connect the gate and drain metallization to the adapter microstrip. Several bond wires were also bonded down from the source pads to the ground metallization to ensure low ground inductance.

Figure 5

The layout of a 12-mm power device.

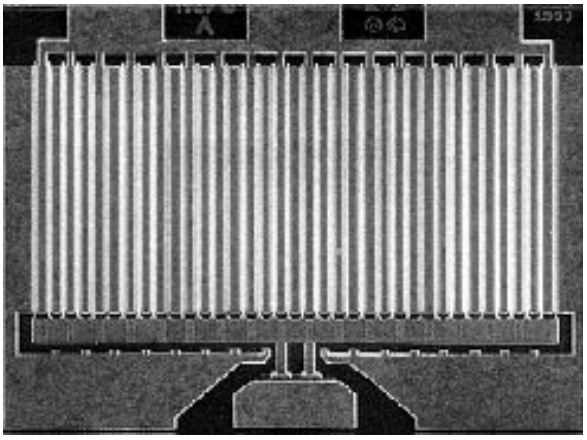
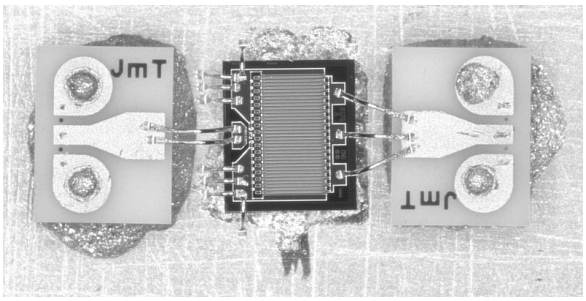


Figure 6

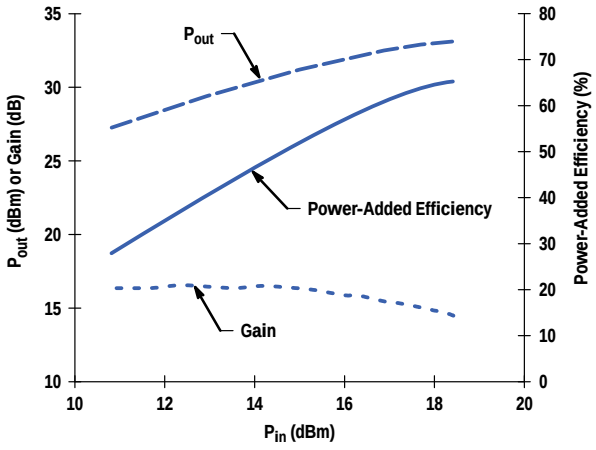
A 12-mm device mounted on a microprobing test fixture used in the on-wafer active load-pull system.



The power characteristics were measured using a vector-corrected, active load-pull system.[2] The use of an active load-pull system ensures that sufficiently low impedance is presented to the device for optimal performance. In addition, it also provides the capability to study the effects of harmonic tuning on power performance. **Figure 7** shows the power saturation characteristics for the 12-mm device under maximum-power tuning. The results were obtained with both fundamental and second-harmonic tuning. The improvement in power-added efficiency by terminating the second harmonics is about 4 to 6 percent. The 12-mm device achieved +33-dBm output power (corresponding to a power density of 167 mW/mm), 14.7-dB power gain (2-dB gain compression), and 65.4% power-added efficiency at 3 volts and 1.8 GHz, which is the highest combined power performance ever reported at such a low bias voltage.

Figure 7

Power saturation characteristics for the 12-mm device at 3 volts and 1.8 GHz.



State-of-the Art Performance Comparison

To benchmark the performance, the results obtained were compared with several competing technologies used in similar applications. The power performance (in terms of the power density) of the E-PHEMT was compared with several state-of-the-art, depletion-mode PHEMT devices operating in the 3-volt range (**Figure 8**). Several results were reported in the 900 MHz range. Also, most of the depletion-mode devices require dual supplies, as opposed to a single supply in our case.

Figure 8

Power performance comparison of state-of-the-art PHEMTs in the 3-volt range.

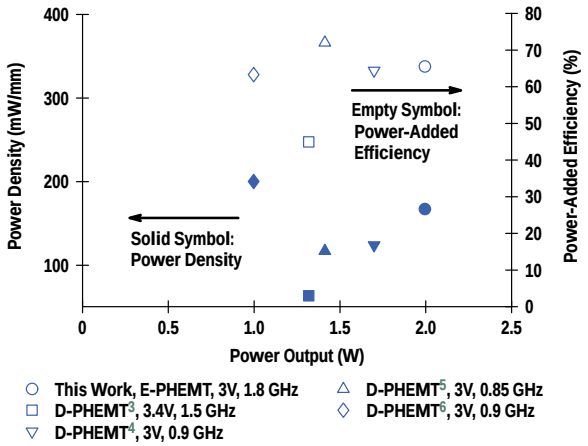


Table III compares HP's 12-mm E-PHEMT device performance with high-performance MESFETs, GaAs/AlGaAs heterojunction bipolar transistors (HBTs), high-performance silicon bipolar junction transistors (BJTs), Si lateral-diffused metal-oxide-semiconductor (LDMOS) devices, and SiGe HBTs. The ability to operate from a single power supply and demonstrated excellent power performance (battery-efficient) at low voltages make the E-PHEMT very suitable for power generation in portable wireless applications.

Reliability

Reliability studies have been performed on devices from five separate wafer runs. The initial purpose of these studies was to determine whether a 2-layer or 3-layer passivation process should be applied. Stress-induced changes in I_d ($V_g = 0.75V$) and BV_{gdo} ($I_g = 500$ mA/mm) were examined. Since this is an enhancement-mode device, it is impractical to use changes in I_{DSS} as a failure parameter, so I_d ($V_g = 0.75V$) was selected.

In a 3-layer SiN_x passivated E-PHEMT, the first layer of SiNx is plasma deposited immediately after MBE. It is believed that this step protects the surface of the wafer from contamination during processing. Any contamination can create surface states that provide a leakage path between the gate and drain fingers, thus increasing sheet resistance and eventually degrading BV_{gdo}. The second layer of SiN_x is deposited after the formation of the ohmic contact metal on the source and drain. The final SiN_x passivation is performed after gate metal liftoff. The 2-layer passivated E-PHEMTs skip the first step.

Table IV shows the change in BV_{gdo} after greater than 1000 hours of stress. All devices were electrically stressed at $I_{ds} = 50$ mA/mm, $V_{ds} = 3V$. In addition to a less severe change in BV_{gdo}, the 3-layer devices also show less degradation at I_d ($V_{gs} = 0.6V$) and $g_{m\ max}$, as shown in **Figures 9a and 9b**.

Table III

Power Performance Comparison for Competing Technologies in Portable Wireless Applications

Device Technology	Frequency (GHz)	P_{out} (dBm)	Power-Added Efficiency (%)	V_{ds} (V)
This Work	1.8	33	65.4	3
SiGe HBT[7]	1.9	30	44	4.7
Double-Poly Si BJT[8]	1.8	24	60	3.5
Hi-Lo MESFET[9]	0.9	31.3	68	2.3
MESFET, $2f_o$ Tuning[10]	0.93	32.8	71	3.5
GaAs/AlGaAs HBT[11]	1.9	22.6	69	3
GaAs/AlGaAs HBT[12]	1.88	33	70	5
BPLDD SAGFET*[13]	1.9	24.7	54	3.3
Delta-Doped MESFET[14]	1.5	30.4	48	3.5
Si LDMOS[15]	0.85	31.8	65	5.8

* BPLDD SAGFET = buried p-layer lightly doped drain self-aligned gate field effect transistor.

Table IV

Degradation of BV_{gdo} in 2- and 3-Layer Passivated E-PHEMTs

2-Layer SiN_x Passivation

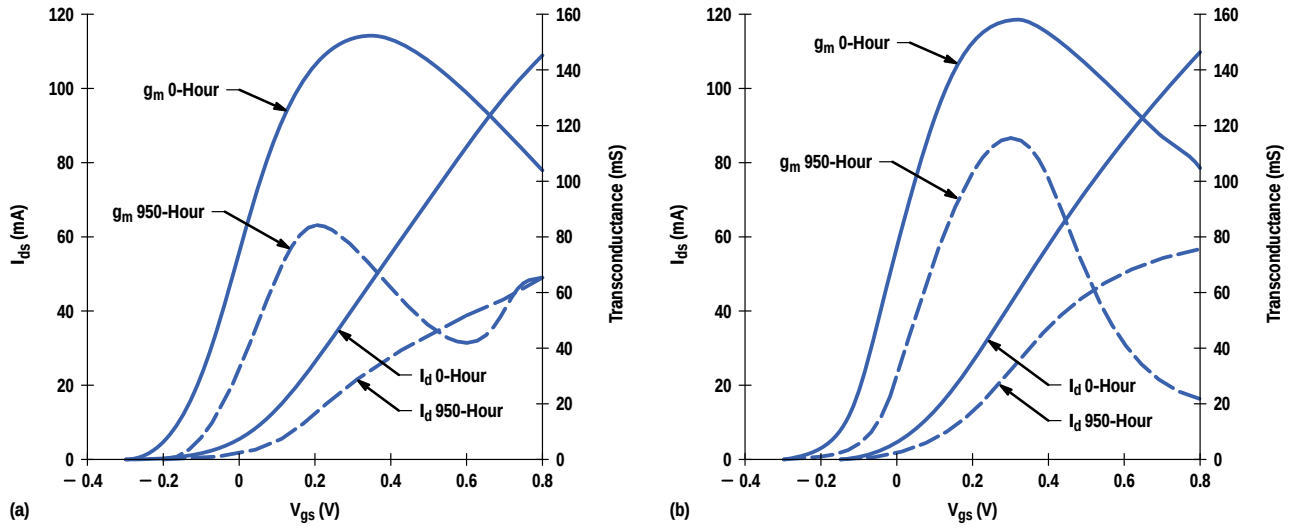
$T_{channel}$ (°C)	BV_{gdo} (V) 0-hr	BV_{gdo} (V) 1085-hr	Percent Change
175	8.72	7.71	−11.58
200	9.52	7.92	−16.80
225	9.31	6.54	−29.75

3-Layer SiN_x Passivation

$T_{channel}$ (°C)	BV_{gdo} (V) 0-hr	BV_{gdo} (V) 1181-hr	Percent Change
175	9.66	10.22	5.79
200	N/A	8.97	
225	9.1	9.12	0.21

Figure 9

(a) I-V characteristics after 950 hours of stress for a device with 2-layer passivation. Solid lines are for 0 hours. I_{ds} (0.6V) and $g_{m\,max}$ degraded by 54% and 49%, respectively. (b) I-V characteristics after 950 hours of stress for a device with 3-layer passivation. Solid lines are for 0 hours. I_{ds} (0.6) and $g_{m\,max}$ degraded by 42% and 27%, respectively.



Since this data indicates superior performance for a 3-layer process, all subsequent reliability tests have been performed using devices with a 3-layer passivation.

The change in s-parameters during dc burn-in has also been examined, as shown in **Figure 10**. The filled data points are for 0 hours, while the open data points are after 1709-hour burn-in. The results from this test are extremely encouraging, in that s_{21} shows virtually no change. The biggest change (average 3-dB reduction) was seen in s_{12}. However, the sensitivity of this measurement could account for this change.

To date, the reliability tests have been preliminary. For the technology qualification, three recent wafers, with 30 devices from each wafer, will be dc stressed at 175°C, 200°C, and 225°C. The parameters that will be monitored are I_d ($V_g = 0.4$) and BV_{gdo} ($I_g = 500\ \mu A/mm$). RF burn-in has also been planned, and additional tests to compare results between 2-layer and 3-layer passivated devices will be done.

Packaged Device Evaluation

The low-cost plastic package chosen to evaluate the performance of the E-PHEMT was an HP micro-small-outline package (MSOP) with grounded backside. This package features an exposed die attach paddle that can be soldered directly to the printed circuit board for thermal and electrical grounding (**Figure 11**).

The die attach paddle is approximately 0.040 inch wide by 0.090 inch in length, which is large enough to incorporate the first LC sections of the RF matching structures. These matching networks consist of silicon MOS capacitors attached to the paddle, resonated with the device drain and gate bond wires (see **Figure 12** for a photograph of the structure and **Figure 13** for a schematic diagram). Placing the capacitors inside the package on the grounded die attach paddle provides the shortest possible ground return path and minimizes parasitic inductive loss elements.

Figure 10

Zero and 1709-hour s-parameter data at 1.8 GHz, showing the effect of burn-in. The channel temperatures were 175°C, 200°C, and 225°C for devices 46-52, 53-59, and 60-67 respectively. Devices 68 and 69 were control devices.

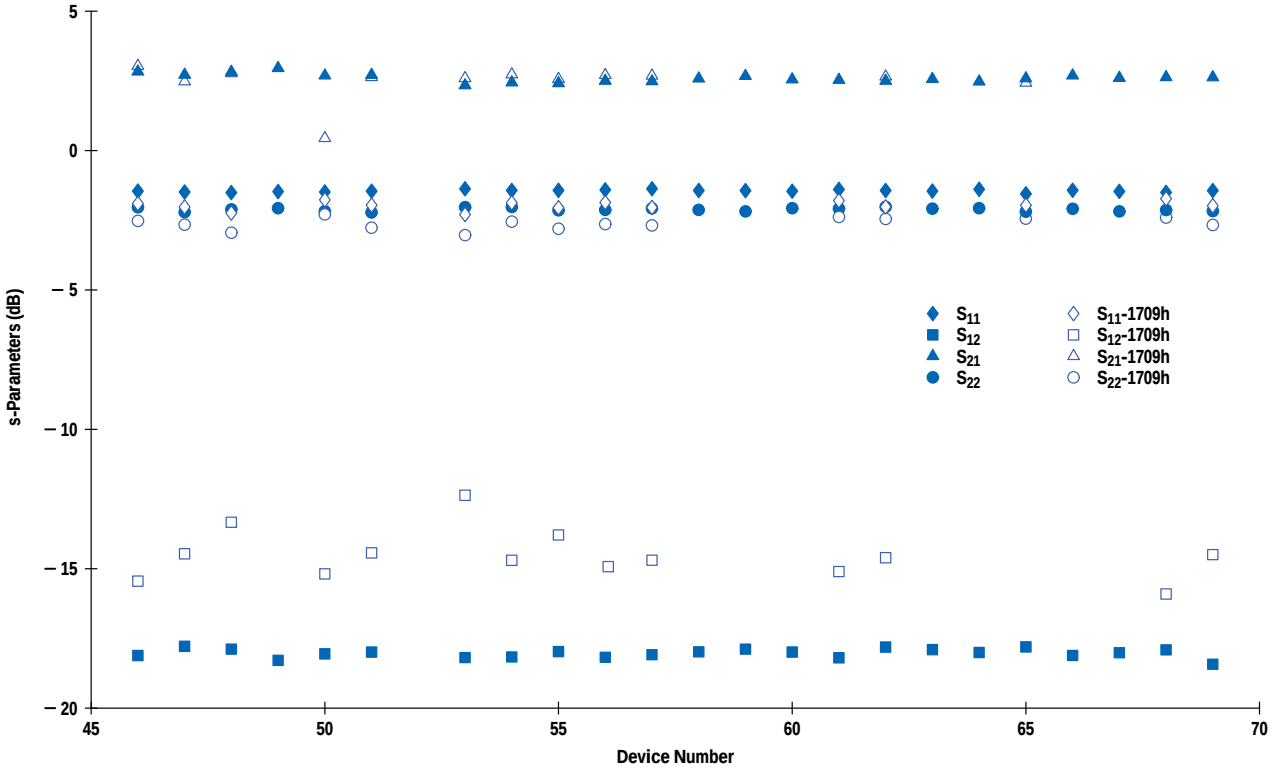


Figure 11

HP MSOP package top and bottom views.

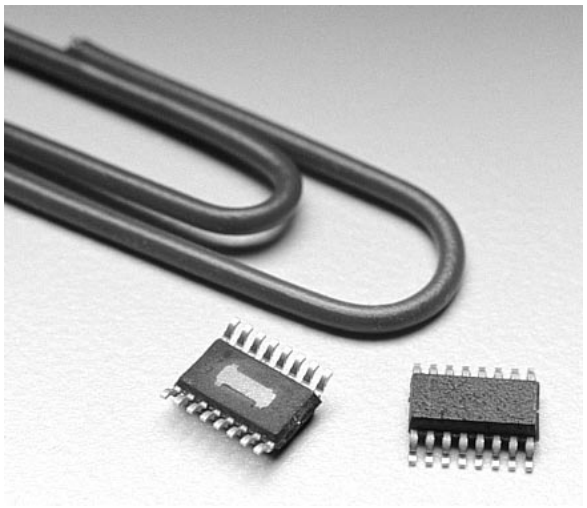


Figure 12

Internal bonding configuration of the E-PHEMT in the MSOP package.

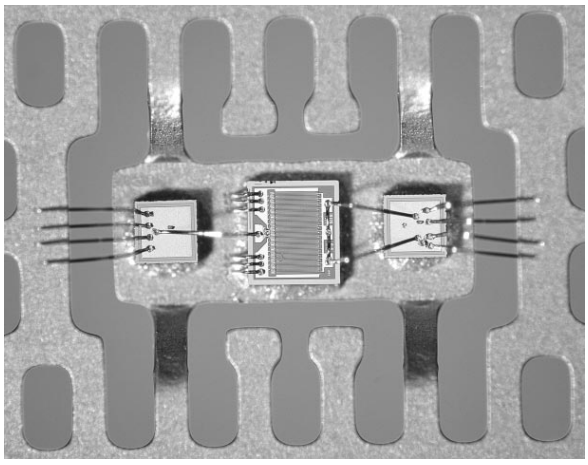
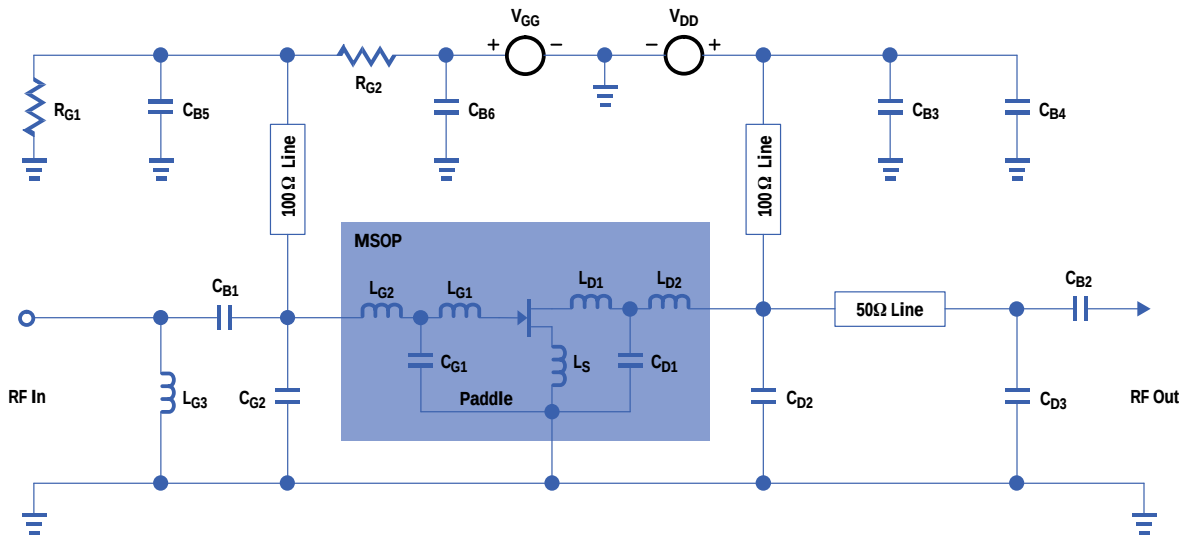


Figure 13

Schematic diagram of the packaged E-PHEMT evaluation circuit.

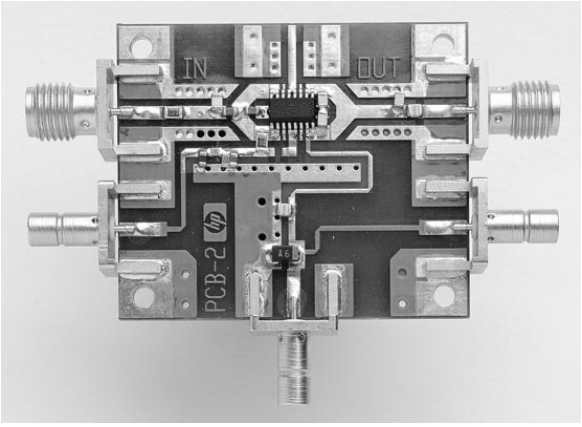


Evaluation Printed Circuit Board

The matching networks contained within the package provide only partial matching for the device gate and drain. Additional matching networks are required external to the package to match the input to 50 ohms and the output to the optimum impedance for maximum power, linearity, or efficiency. The evaluation printed circuit board (see **Figure 14**) provides pi-section matching networks on both the input and output to achieve these goals, along with quarter-wavelength transmission line networks for gate and drain biasing.

Figure 14

Printed circuit board used to evaluate the packaged E-PHEMT.



The complete schematic of the packaged device, external matching networks, and biasing networks is shown in **Figure 13**.

Performance

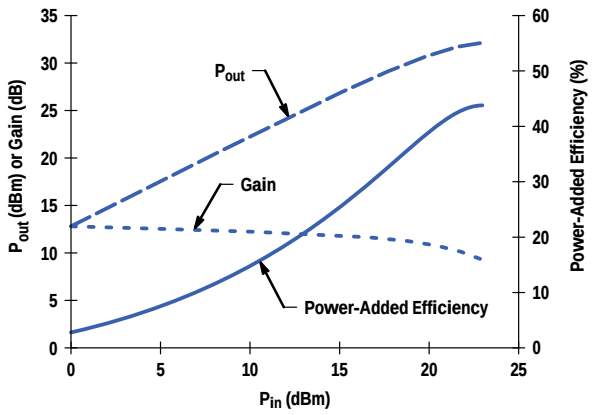
The following test conditions were used to characterize the basic gain, power, and efficiency performance of the packaged E-PHEMT:

- Frequency = 1880 MHz
- V_{dd} = 3.0 volts
- Duty Cycle = 100% (CW)
- I_{ds} (no signal) = 200 mA (set by adjusting a positive bias voltage at the gate).

The measured small-signal gain was 12 dB. Measured output power was +31.0 dBm at 1-dB compression and better than +32.6 dBm at 3-dB compression. At 32.6 dBm, the power-added efficiency was 42 percent. The performance is summarized in **Figure 15**. Note that for the power and efficiency measurements, the matching network losses were not removed.

Figure 15

Performance of the packaged E-PHEMT in the evaluation circuit.



In addition to the basic single-tone performance described above, PCS systems also require the handset power amplifier to meet certain linearity requirements to maintain low bit error rates in the transmitted signal. The requirements vary with the modulation technique employed. **Table V** summarizes the performance of the packaged E-PHEMT compared with the requirements for typical CDMA and TDMA PCS systems. Test conditions for these measurements were the same as for the preceding gain, power, and efficiency tests. A 0.8-dB correction has been applied to account for the measured output circuit matching loss.

Table V
Performance of Packaged HP E-PHEMT versus PCS System Requirements

Parameter	PCS CDMA	HP E-PHEMT	PCS TDMA	HP E-PHEMT
Output Power (dBm)	+28.5	+28.4	+28.5	+28.5
Efficiency (%)	30	33.6	40	43
Adjacent Channel Power (dBc)	−29	−31	−26	−27

Conclusion

Leveraging initial work at HP Laboratories, an enhancement-mode PHEMT device technology has been developed that offers excellent gain, power, and power-added efficiency using a 3V bias. Fundamental elements of this new device technology include careful selection of MBE material structure, adaptation of HP Laboratories' fabrication process to mesh with CSSD's existing PHEMT process, and device layout optimization to achieve the best overall measured performance. Devices built using this new technology have demonstrated +33-dBm output power with 65% power-added efficiency and 15-dB power gain when operated from a 3V supply at 1.8 GHz. This compares very favorably with the performance that can be achieved using other device technologies, which require additional components like dc-to-dc converters or higher supply voltages.

HP's new E-PHEMT technology is very well-suited for use in power amplifiers for PCS telephones. Using this technology, PCS power amplifiers that can operate from a 3V single supply with excellent performance are now a reality.

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