RF Technology Trade-offs for Wireless Data Applications

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Rapidly evolving wireless system standards and applications are placing demands on RF semiconductor manufacturers to produce highly specific and optimized RFIC solutions for specific growth segments including wireless data terminals.

Current RF wireless connectivity standards used for LANs and WANs include cellular and PCS (Personal Communications Services) protocols such as GSM (Global System for Mobile Communications) and AMPS (Advanced Mobile Phone System), trunk radio systems such as RAM and Ardis (proprietary systems), and ISM (industrial-scientific-medical) systems. In the future, satellite-based standards and dedicated wireless data systems such as HIPERLAN (European 5-GHz LAN) and U-NII (Unlicensed National Information Infrastructure) will be more commonplace. From a wireless data user standpoint, the radios based upon these standards can be implemented in a variety of physical form factors including removable PC cards that contain an entire radio, radios that are built into a dedicated data collection terminal, or cellular and PCS phones that connect to a laptop modem via a cable.

The applications listed above are made possible through high-performance RF semiconductor components. These applications range in frequency from several hundred megahertz to 6 GHz and above and require several watts of power output in some cases. These requirements need to be satisfied along with aggressive cost goals, achieved by means of low-cost, surface mount plastic packaging. The RF semiconductor technologies on which these components are based currently include gallium arsenide (GaAs) and silicon bipolar and will increasingly include CMOS in the future. Some specific examples of end-product benefits that RF component technologies can affect on a first-order basis include the cost, size, weight, and battery life of the wireless data terminal.

Lower cost is now being achieved in end-user applications as a result of the tremendous growth of the RF semiconductor industry and the corresponding economies of scale that are created. Innovative RF architectures and approaches to high-level integration can also lead to much lower cost.

Smaller wireless data terminals are made possible by highly integrated components that allow multiple functions and previously external support elements to be incorporated onto a single RFIC. This approach is usually only justified for high-volume standards and applications and the resulting IC does not have the flexibility to be used for a wide variety of standards. For the digital cellular standard GSM (Global System for Mobile Communications), a highly integrated approach is justified because of the large production volumes and relative homogeneity of the technical approaches used by various customers. However, the relatively small wireless data market currently consists of a fragmented group of existing and emerging standards. Therefore, a highly integrated RFIC approach is risky to the component manufacturer and limits the number of these RFICs that are being developed for the market. An alternative way of accomplishing the small size objective is to use very small, flexible, high-performance building-block RFICs that contain a few key functions per product. These RFICs can be used in a variety of systems and with a variety of customers. This wide range of use allows these RFICs to be produced at a very low cost.

Substantially longer battery operation has been achieved in RF communications equipment partly by RF components that have lower supply current requirements (higher efficiency). Within the radio system, the power amplifier usually requires a large percentage of the supply current budget relative to the rest of the RF components. As a consequence, many of the component developments geared for improved efficiency are targeted toward the power amplifier.

Lower-weight systems have emerged because RF component manufacturers have been able to reduce their supply voltages, thus enabling operation from fewer battery cells. The battery is the heaviest component in many battery-powered communication devices. Despite its high cost, lithium-ion is a common battery technology that is in favor for its improved battery life, reduced memory effects, and longer storage times.

Target Applications and Available Technologies

RF system specifications have a great impact upon the ultimate cost, size, weight, and battery life of any radio implementation. System-level trade-offs that include data rate, bit error rate (BER), system capacity, and range ultimately drive the radio specifications. These specifications directly affect the choice of RF components and technologies used in the radio. The major RF component drivers include operating frequency, RF output power, and modulation technique. Key system specifications of some examples of wireless data systems are summarized in **Table I**.

Table I
Examples of Wireless Data Systems

System	Frequency Band (MHz)	Data Rate (kbits/s)	Channel Spacing (MHz)	Modulation	Transmit Power (W)	Range (m)	Comments
CDPD	824-849 Tx 869-894 Rx	9.6	0.03	GMSK	0.6	10000	Uses empty analog cellular channel
U-PCS	1910-1930	1152	1.0	π/4 DQPSK	0.1	200	Unlicensed part of U.S. PCS bands
IEEE 802.11	2400-2483	1000 2000	1.0	2-GFSK 4-GFSK	0.1, 1	100	Subject to significant interference
HIPERLAN	5150-5300	23500	30	GMSK	1	50	

CDPD = Cellular Digital Packet Data.
GMSK = Gaussian minimum shift keying.
2,4-GFSK = 2-level or 4-level Gaussian frequency shift keying.
IEEE 802.11 = 2.4-GHz wireless LAN standard.
π/4 DQPSK = π/4 differential quadrature phase shift keying.

The operating frequency is a key specification because it affects many RF component decisions including whether GaAs or lower-cost silicon bipolar components can be used. Other considerations include whether the convenience of easy-to-use RFICs can be exploited or if discrete components are the best way to achieve the required noise figure and power efficiency. Development time and available RF expertise are also factors in choosing between RFICs and discrete components.

The modulation technique employed in a radio is a critical specification because it drives the type of modulator used in the system. A simple FSK (frequency-shift keying) technique can be implemented with minimal cost by direct modulation of the phase-locked loop. FSK-based systems do not require a linear transmit path, so lower-cost and lower-current components can be used. Techniques based upon QPSK (quadrature phase-shift keying) modulation require an I-Q (in-phase and quadrature) modulator in the transmit path, which adds cost. In addition, linear power amplifiers, which consume larger currents, are required for modulation techniques that have envelope fluctuations, such as QPSK. The benefit of QPSK systems is greater spectral efficiency or user density, but this is often sacrificed in unlicensed wireless data applications where no revenue stream is available to subsidize the terminal cost.

The power output levels of wireless data terminals typically range from milliwatts to watts. On the high end of the range, a GSM data terminal (two watts out of the antenna) might use a hybrid power module. A wireless LAN output stage with power output of 10 mW can use a simple bipolar transistor or RFIC that may cost only one twentieth as much as the GSM solution. The required power levels, along with the modulation technique, help determine the semiconductor technology that will be used. For a 2.4-GHz wireless LAN system that requires 1W output power and uses QPSK modulation, a GaAs-based output amplifier is essential for the higher gain and linearity provided by this technology. On the other extreme, a 0.5-mW average remote control device operating at 900 MHz with an on/off modulation technique may favor the use of a low-cost silicon bipolar transistor or RFIC.

Table II summarizes the key HP RF semiconductor technologies currently used to develop high-volume wireless RFICs, as well as potential future candidate technologies. GaAs RFICs based on PHEMTs (pseudomorphic high-electron-mobility transistors) are typically restricted to fairly low-levels of integration in front-end components such as low-noise amplifiers, transmit/receive switches, or power amplifiers. PHEMTs can also be used to make excellent upconverters and downconverters, but the cost penalty relative to silicon bipolar often overcomes any slight performance advantage. HP's ISOSAT silicon bipolar technology features good high-speed n-p-n transistors combined with excellent passive elements including high-Q inductors, precision high-Q capacitors, integrated varactor diodes, and integrated 100-GHz Schottky diodes. This makes ISOSAT ideal for most frequency converter applications including I-Q vector modulators and high-dynamic-range downconverters. ISOSAT passive elements can also be used to improve narrowband amplifier performance and even build fully monolithic voltage-controlled oscillators (VCOs).

The HP-25 process listed in **Table II** is an example of a state-of-the-art, high-speed, highly manufacturable silicon bipolar process that can provide high levels of integration even for RF applications. HP-25 is based on a mainstream CMOS process and is built in the same high-volume fabrication facility with the same tools as CMOS. Next-generation RF bipolar processes are expected to have even higher-performance n-p-n transistors while using passive elements improved upon from ISOSAT. By continuing the HP-25 philosophy of using CMOS-based unit processes, these next-generation RF bipolar processes should be highly manufacturable and low in cost. However, CMOS technologies are also improving dramatically over time, and next-generation CMOS will be capable of implementing many RF functions, especially those used in frequency synthesis and IF demodulation.

Table II
RF Device Technologies

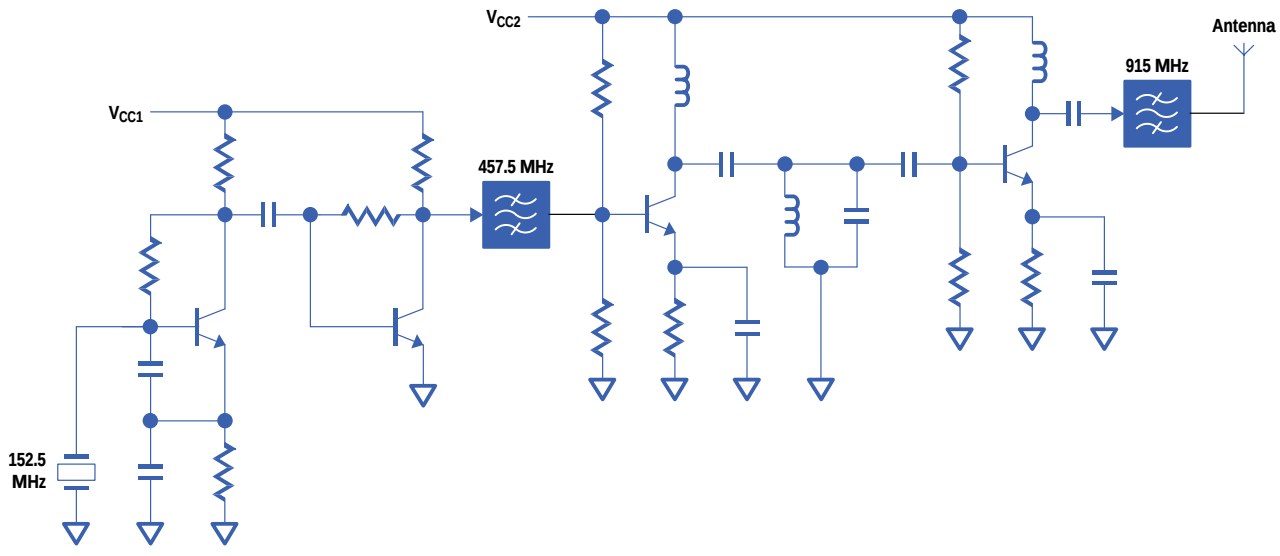
Process Technology	f_T (GHz)	f_{max} (GHz)	$Q_{inductor}$ (4 nH at 2 GHz)	Manufacturable Die Size (mm^2)	Cost
ISOSAT	14	30	10	2-3	Medium
HP-25	25	30	5	10-20	Low
HP PHEMT	60-90	N/A	20	< 1	High
Next-Generation RF Bipolar	30	> 50	15	10-20	Low

Example 1: Low-Cost 900-MHz Remote Control Data Device

Consider an extreme example of a very simple wireless data device implemented at the lowest possible cost. This type of one-way device could be used for keyless entry (with a data-encrypted security code), meter reading, or remote control of digital equipment. Key attributes are low cost and current consumption at the expense of short range, very low data rate, and somewhat unreliable operation.

A possible circuit schematic is given in **Figure 1**. Conceptually, the transmitter consists of a crystal oscillator, frequency tripler, frequency doubler, and output amplifier to provide an on/off keyed data stream in the 902-to-928-MHz ISM band under U.S FCC Part 15.249 low-power rules. The RF section would have the crystal oscillator and tripler turned on

Figure 1
Low-cost transmitter.



several milliseconds before transmission. The on/off keying could be as crude as simply enabling V_{CC2} by a depletion-mode FET controlled by a CMOS bit from a microcontroller. This can work quite well for low data rates of 10 kbits/s or less (100-μs-duration pulses). Under Part 15.249 rules, the average transmit power in any 100-ms period must be less than 0.5 mW. This would allow, for example, 5-mW transmit power at the antenna in **Figure 1** so long as the bursts are only 10 ms long (or 100 bits at 10 kbits/s) and spaced 100 ms apart.

As illustrated in **Figure 1**, the RF semiconductor portion of the transmitter is only four discrete bipolar transistors, which can be identical, ultralow-cost AT41533s. The 457-MHz bandpass filter can be realized easily by printed coupled lines, so the 152.5-MHz crystal and the 915-MHz bandpass filter represent the only significant passive elements in terms of cost. In the U.S.A., in sufficiently high volume, the RF transistors are much less than one dollar for all four and the total cost of this solution is only two to three U.S. dollars, making it competitive with an infrared solution.

Example 2: Highly Integrated 2.4-GHz Wireless LAN

In the 2.4-GHz wireless LAN market, meeting the small size requirements of the popular PC-card form factor demands a high level of integration, both in the RF and digital circuits of the device. The digital part of the device is now routinely accommodated in only a few components, typically an application-specific controller IC and associated ROM and RAM, and as such can easily be accommodated within the PC-card form factor. However, the RF sections are not so easily integrated, and therefore careful consideration must be given to the radio architecture to ensure an optimum trade-off of size, power consumption, and component cost. One such architecture for a frequency-hopping wireless LAN, with the majority of functionality resident in only a few ICs, is illustrated in **Figure 2**.

The radio consists of a double-conversion superheterodyne receiver and a single-conversion transmitter. This arrangement is helpful in achieving the 100-MHz operating width of the 2.4-GHz ISM band while providing adequate suppression of transmitted spurious and received image responses. Some care must be exercised in choosing the first intermediate frequency (IF) to ensure that it is not affected by spurious products generated elsewhere (e.g., harmonics of the crystal reference) and that its own harmonics will not be a problem. In this example, 236 MHz is used for both the transmitter and the receiver since this allows small, low-cost, three-pole ceramic filters to be used in the transmit chain, meets the limits for spurious emissions dictated by the regulatory bodies, and is not affected by the 16-MHz reference.

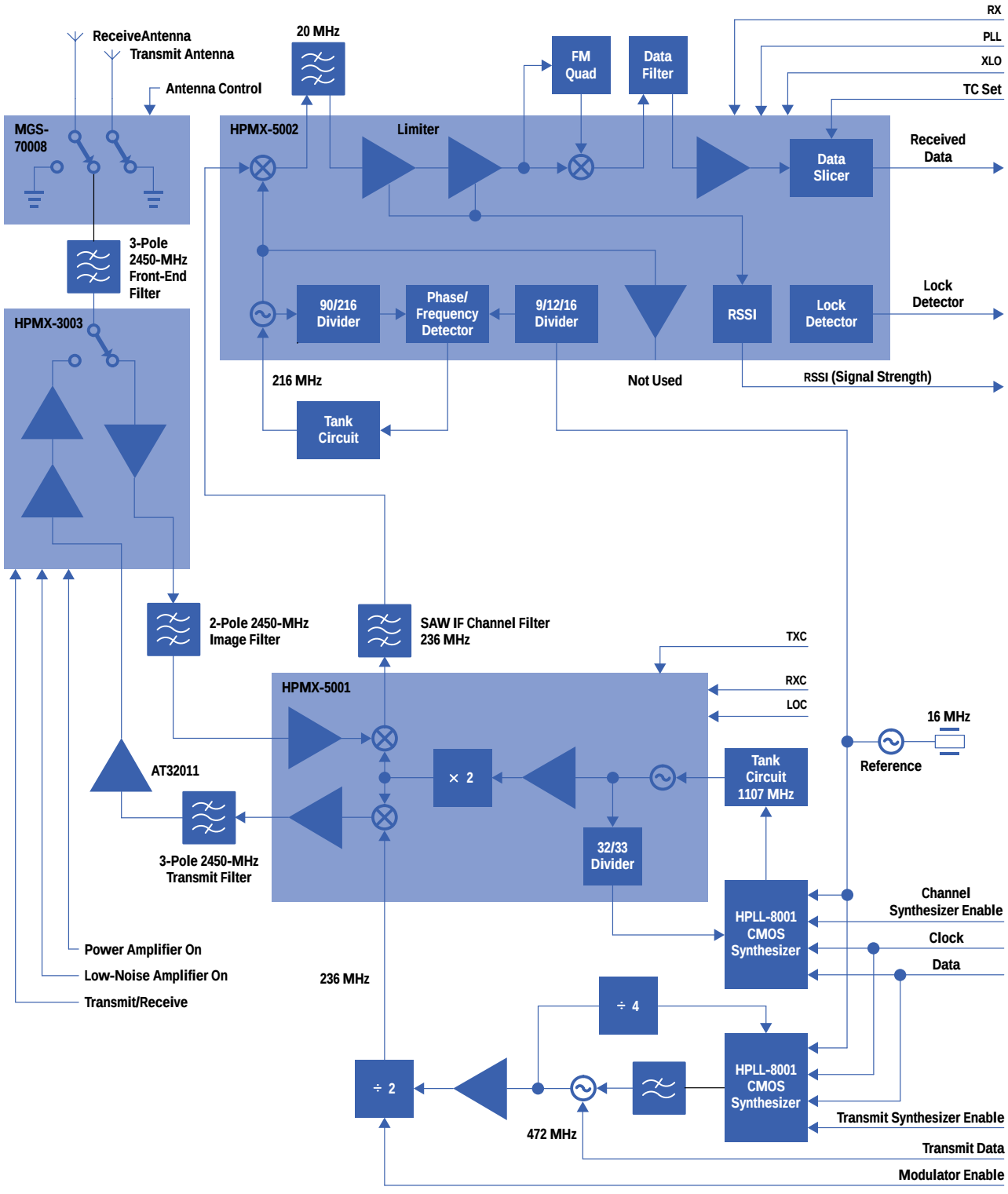
Translation between the first IF and 2.4 GHz is performed by the combination of the HPMX-5001 upconverter/downconverter IC and the HPLL-8001 high-speed CMOS synthesizer. The synthesizer, operated in a dual-modulus configuration with the HPMX-5001's 32/33 dual-modulus prescaler is used to define the channel of operation. Driven from a 16-MHz reference—an integer multiple of the system channel spacing—the synthesizer can hop channels easily within the 224 μs required by the IEEE 802.11 standard. Transmit/receive turnaround time is less than 19 μs, the fast turnaround dictated by the RTS/CTS protocol normally used in a wireless LAN system. This is achieved by continuously running the modulator synthesizer at twice the second IF so as not to interfere during receive periods, and then connecting via a divide-by-2 circuit to the HPMX-5001 only during transmit periods.

The HPMX-3003 provides the major front-end functions of low-noise amplifier, switch, and power amplifier. The transmitted signal from the HPMX-5001 followed by the AT31011 driver is amplified to a final output power level at the antenna in excess of 200 mW by the HPMX-3003. Note that 100% duty cycle operation is possible with this device, which is an important consideration in asynchronous wireless LAN applications, in which the transmit duty cycle is determined by traffic loading to a large extent and is not usually limited to any significant degree. Transmit/receive antenna switching is provided by the HPMX-3003's low-loss switch. In the receive path the HPMX-3003's high gain and low noise figure ensure a good overall sensitivity for the receiver.

To improve the overall system performance and data throughput it is often desirable to include some form of diversity in the transmission channel. Most popular in low-cost systems is receiver antenna diversity, that is, a dual-antenna receiver, which can offer up to 10-dB improvement in system error performance. In **Figure 2** we illustrate this with two antennas spaced nominally λ/2 apart and selected by an MGS-70008 GaAs MMIC switch.

Figure 2

Frequency-hopping 2.4-GHz wireless LAN.



The HPMX-5002 provides all the necessary functionality for the demodulation of a downconverted 2-FSK signal. The HPMX-5002 contains the receiver's second mixer, limiting IF amplifier chain, discriminator, data slicer, lock detector, and RSSI (receive signal strength indicator) circuits. Also included are the necessary active components and dividers to generate the receiver's second LO. In **Figure 2** we use a second LO frequency of 216 MHz derived from the 16-MHz reference to create a 20-MHz second IF. The second IF is chosen low enough to ensure that the quadrature discriminator can be designed with low-tolerance components to minimize cost and avoid production adjustments while maintaining a low fractional bandwidth. Output from the discriminator's Gilbert-cell mixer is fed via an external data filter to the data slicer. The sliced receive data is then passed to the radio controller where it is processed and decoded according to the MAC (media access control) protocol being used (e.g., IEEE 802.11).

The complete RF section of this highly integrated wireless LAN consisting of RFICs, filters, and associated passive components is accommodated in less than 15 cm^2 of printed circuit board surface area, making it ideally suited to PC-card applications. The use of low-voltage operation in the devices combined with their power management facilities creates a low-power design particularly suited to portable applications. Interfacing to the radio controller is straightforward, with the majority of signals interfacing directly at normal CMOS levels. Only a minimum of interface circuitry is required to implement the full level of control required for the current generation of wireless LAN systems. Many of the key performance parameters are summarized in **Table III**.

Table III
Summary of 2.4-GHz Wireless LAN RF Section Performance

Supply Voltage	3V
Receive Mode Current	100 mA
Transmit Mode Current	500 mA
Frequency Band	2.4 to 2.48 GHz
Transmit Power	200 mW
Data Rate	1 Mbit/s
Sensitivity	−80 dBm
Range (Loss of Signal)	>100 m
Board Area	15 cm^2

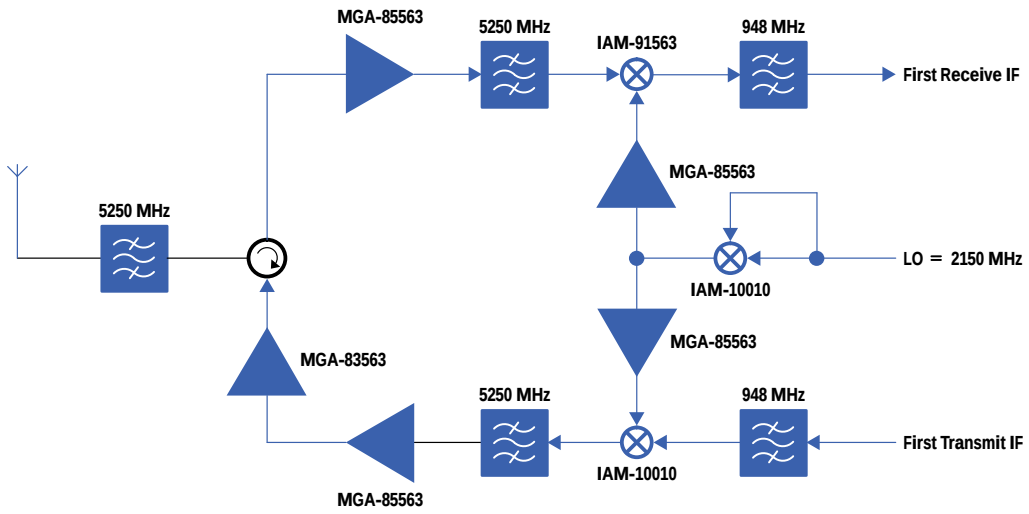
Example 3: Rapid Development of a 5-GHz Wireless LAN

Recently, considerable interest has arisen in building wireless LANs at 5 GHz to obtain much higher data rates (of the order of 10 Mbits/s) in unlicensed operation without the burdensome rules and problematic interference of the 2.4-GHz ISM band. An example of this is HIPERLAN in Europe. In the U.S.A., the FCC is considering allocation of the band from 5.15 to 5.35 GHz for similar types of high-data-rate wireless LANs. However, wireless terminal manufacturers wanting to build real products in this band will not have highly integrated chipsets as shown in Example 2 for the near future because of the immaturity of the applications and the standard, as well as the difficulty of RF integration at 5 GHz. While discrete RF devices using circuit techniques similar to Example 1 are theoretically possible at 5 GHz, the development time and engineering resources required would be huge for a complex system such as a high-data-rate wireless LAN. The best alternative by far is to use RFIC building blocks. HP manufactures many different building-block RFICs using both ISOSAT (silicon bipolar) and PHEMT (gallium arsenide) technologies. In general, these products are available in tiny surface mount plastic packages such as SOT-363, MSOP-10 and SSOP-16. The building blocks are usually one-function or two-function devices that have a wide range of uses and can be easily matched without stability problems.

An example of a 5-GHz wireless LAN RF front end running completely from a single supply voltage of 3.0V (a single lithium-ion cell) is shown in **Figure 3**. This block diagram can be implemented completely using low-cost, single-function RF building blocks as denoted by the HP part numbers in **Figure 3**. The choice of 948 MHz as a first IF is not accidental.

Figure 3

Building-block up/downconverter for a 5-GHz wireless LAN.



Most proposals for this 5.15-to-5.35-GHz band have wide channels ranging from 10 to 25 MHz. At 948 MHz, two very high-volume off-the-shelf SAW (surface acoustic wave) filters that could be used as channel filters for this application are the 935-to-960-MHz GSM receive filter or the 940-to-956-MHz PDC transmit filter. There are a number of highly integrated GSM receiver RFICs available, and these could be leveraged to minimize design effort. Also, a variety of transmit solutions are possible, including, for example, the HPMX-2007 vector modulator and upconverter.

In **Figure 3**, the nominally 4300-MHz first LO is generated by frequency doubling a 2150-MHz VCO. The doubler is an ISOSAT silicon bipolar RF building block, the IAM-10010, which can also be used as an upconverter at 5 GHz in the transmit chain. The channel synthesizer for the nominally 2150-MHz LO can be implemented in many ways, including, for example, a low-cost prescaler and the HPLL-8001. The output power amplifier in this example is the MGA-83563, which is a fully monolithic, two-stage PHEMT power RFIC usable to 6 GHz with 200-mW output power matched into 50 ohms. On the receive side, the MGA-85563 (another PHEMT RFIC) is used as the low-noise amplifier for its <2-dB noise figure and excellent matching even at these high frequencies. The IAM-91563 downconverter is also a PHEMT RFIC and is ideal for this application because of its 10-dB SSB noise figure and high IF bandwidth including conversion gain into 50 ohms. The versatile MGA-85563, although nominally a low-noise amplifier, is also used in three other blocks in **Figure 3** as an LO buffer and transmit driver.

At first glance, the use of eight separate RF building blocks at 5 GHz in **Figure 3** to provide the functionality of two highly integrated RFICs at 2.4 GHz in **Figure 2** may seem to increase the size of the solution astronomically. However, it is important to note the extremely small physical size of these RF building blocks. The IAM-10010 is housed in a tiny MSOP-10 package, which requires less than 50% of the area of the industry-standard SOIC-8. The MGA-83563, MGA-85563, and IAM-91563 are all housed in the ultraminiature SOT-363 package (or 6-lead SC-70), which is actually 30% smaller than the industry-standard SOT-23 transistor package. In addition, separate RF building blocks often provide much better board layout flexibility for filter placement than do highly integrated RFICs. A summary of some key performance parameters for the block diagram of **Figure 3** is given in **Table IV**.

Table IV
Summary of 5-GHz Wireless LAN Up/Downconverter Performance

Supply Voltage	3V
Receive Mode Current	70 mA
Transmit Mode Current	250 mA
Frequency Band	5.15 to 5.35 GHz
Transmit Power	100 mW
Receiver Noise Figure	< 10 dB
Receiver Input Third-Order Intercept (IIP3)	− 10 dBm
Board Area	20 cm^2

Future Technology Trends

A key trend is the growing proliferation of incompatible data communications services. Data communications is being provided by paging, short-messaging services, data connections through cellular systems, wireless in-building LANs, and fixed satellite systems. Services that are just becoming available include mobile satellite systems, community wireless networks, and wireless multimedia networks. This proliferation of communications standards is occurring in the U.S. cellular industry as well. The new Personal Communications Services (PCS) bands are being populated with at least four different digital communications standards, and compatibility with the existing analog standard will be desired as well. A technical challenge, but one many consumers request, is to build a single radio that is flexible enough to be used for many of these multiple applications.

Another major trend arises from the demand for higher bit rates, which require the allocation of larger blocks of spectrum. Such expansive swaths of bandwidth are only available at higher frequencies. For example, the U.S. FCC has recently reallocated 300 MHz of bandwidth to unlicensed data communications at 5 GHz, and has already approved 5 GHz of spectrum at 60 GHz for unlicensed data communications. One advantage of using higher frequencies is a reduction of the size of an antenna. However, creating circuits that operate at such high frequencies requires improved design techniques and higher-performance devices.

Presently, cellular telephones are made from hundreds of components assembled on high-quality printed circuit boards. While the integration level of microprocessors has grown exponentially, the very high performance requirements of radio communications has slowed efforts toward integration. However, as low-cost technologies with high integration capabilities gain greater performance, the ability to integrate radios increases. An obvious example is the HPMX-5001 from the wireless LAN of Example 2 at 2.4 GHz. This one RFIC replaces several building-block-level RFICs or dozens of discrete components. However, CMOS, with its tremendous scale of integration capabilities and rapidly improving performance, offers the potential for substantial increases in radio integration. Research at universities hypothesizes that it may someday be possible to put a complete radio on a single IC with very few external components, at least for fairly simple systems such as ISM-band wireless LANs. The size reduction, along with the ease of embedding such a one-chip radio, should enable the use of radios in palm-tops, lap-tops, and other computing appliances. Also, much of the cost of a radio is presently in the discrete passive components, assembly, and test.

In Examples 2 and 3, **Figures 2 and 3** showed the block diagram of a traditional superheterodyne radio. This architecture has been used in virtually every commercial radio for the past 50 years. The great advantage of this technique is that the filtering to select the desired channel can be done in stages at conveniently located fixed frequencies.

Unfortunately, the filters shown in the heterodyne radio architecture are very difficult to implement on an integrated circuit. Precise high-performance filtering can be performed on an IC, but only at low frequencies. A number of techniques, which have been known for years but rarely used, are being reexamined to solve this problem. **Figure 4** shows an implementation of a direct-conversion (or homodyne) radio. In this architecture the carrier frequency is immediately converted to a very low frequency where it can be filtered and digitized with great precision by on-chip circuitry. There are several serious drawbacks to this approach, many related to the very high dynamic range required by radios in a naturally interference-prone environment. Solving these drawbacks will require further research, but the new design possibilities available in monolithic integration could provide possible solutions.

Figure 4

Direct-conversion homodyne receiver architecture.

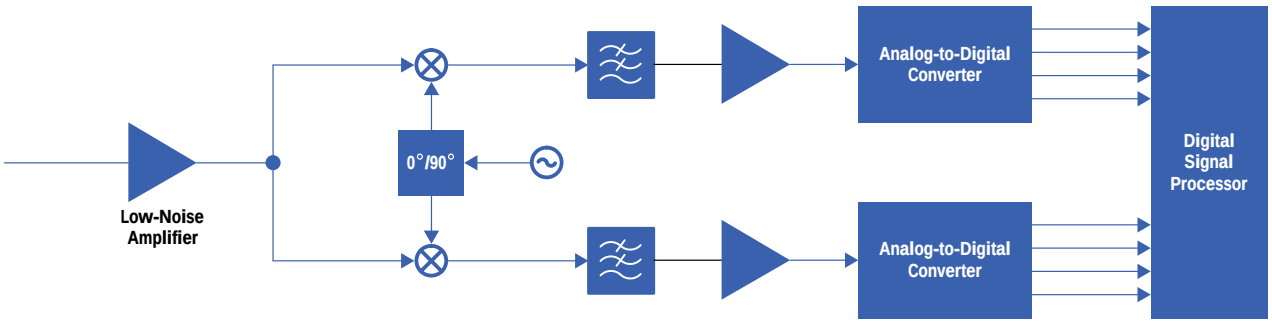


Figure 4 also raises the issue of digital versus analog processing. Presently, most radios convert the signal into the digital domain only after extensive processing in the analog domain. All filtering, gain control, and demodulation are performed in the analog domain. This approach has been mandated by the great precision and relatively high speed required for these functions.

However, as CMOS technology has progressed, the ability to do digital computations has grown nearly exponentially. It is now possible to perform digital operations to accomplish what has been done with analog filters at comparable power dissipation levels. The advantages of digital processing are many. Digital circuits can be designed more rapidly and verified more accurately. Digital circuits operate extremely reliably. They are less sensitive to temperature, power supply, and processing variations, and do not need tuning or adjustment.

Perhaps most important, the move to more digital processing simplifies attempts to provide flexible radios for multiple applications. For example, if the final channel filtering is performed in the digital domain, it is much simpler to adapt to the different channel bandwidths that are required for various applications. Similarly, different modulation formats can be decoded by a simple change in the programming of the digital part. Such wide-ranging flexibility (consider switching from a 30-kHz-wide channel for data on U.S. cellular bands to 1-MHz channels for data on the U.S. ISM bands) is very difficult for analog filters.

In the long term, the ability of high-performance CMOS to alter the boundary between traditional analog circuitry and digital processing will have a profound effect on RF products independent of the tremendous potential for CMOS as an RF analog device.

Conclusion

Rapidly evolving system standards and applications are now placing even more demands upon the RF semiconductor manufacturer. As standards stabilize, more semiconductor manufacturers will produce highly specific and optimized RFIC solutions for specific growth segments including wireless data terminals.

Customers increasingly demand easy-to-use RF solutions that are available from a reduced set of vendors. This is especially true in the area of wireless data as nontraditional RF customers add connectivity to their end-products to increase the utility of these products. These customers desire component solutions that allow quick entry into the market with minimum risk.

Active RF components will continue to absorb functionality that was previously implemented with passive RF components. This provides benefits in the areas of cost, size, and weight. HP has already introduced silicon bipolar products that include on-chip bandpass filtering, on-chip Schottky diodes in a mixer configuration, and reactive elements for output stage matching.

Despite its relatively small market size in 1997, increased attention and resources are being devoted to the wireless data market by RF component manufacturers, who are betting on the emergence of widely used applications, adoption of interoperability standards, and installation of infrastructure so that this market can grow in accordance with explosive forecast projections.

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