Testing with the HP 9490 Mixed-Signal LSI Tester

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The tester's features include a timing interval analyzer for statistical analysis of clock periods, synchronous generation of arbitrary waveforms with respect to master digital clocks, and a library of digital signal processing routines. These features have been applied to production measurements of key parameters like AGC loop bandwidth, phase-locked loop timing jitter, and ADC signal-to-noise ratio and distortion parameters.

In recent years, there has been significant theoretical work on defining a methodology for fault detection and classification in analog circuits.[1-4] However, because input-output relationships are more complex for analog circuits than for digital circuits, the development of a systematic, automated approach for detecting defects in analog circuits is far behind the digital counterpart. For this reason, implementations of analog test strategies remain largely functional.[3] This is also the case in the work described here.

The purpose of this paper is not to further the state of mixed-signal test theory and methodologies, but rather to share with the reader the state of mixed-signal testing within the HP Integrated Circuit Business Division (ICBD) today. We present descriptions of the test development processes for a partial response maximum likelihood (PRML) read channel ASIC and a charge-coupled device (CCD) signal processor ASIC, including specific examples of analog test implementation demonstrating some of the capabilities of the HP 9490 tester.

The read channel IC was designed for HP's DDS3 format DAT (digital audio tape) drive. The CCD signal processor is a three-channel interface chip designed for HP's scanner products. These chips contain significant analog functionality, including programmable and automatic gain control (AGC) amplifiers, switched capacitor filters, a clock recovery phase-locked loop, moderate- and high-resolution analog-to-digital converters (ADCs), and several

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digital-to-analog converters (DACs). The test strategy implemented for these blocks was largely functional. Many circuits could not afford the additional complexity and parasitics of embedded test access. However, provisions were made in the designs for accessing inputs and outputs of functional blocks, and to allow special test modes of operation. The HP 9490 tester has sufficient analog resources to efficiently execute detailed functional testing with high resolution for detecting subtle variations in performance resulting from process variations and defects (see "Tester Description" on page 66).

The emphasis of this paper is primarily on analog test, with specific examples given for the read channel AGC and phase-locked loop blocks and the CDD signal processor analog signal path.

Test Program Evolution

The test programs for the read channel and CCD signal processor chips both evolved in three distinct phases:

- Turn-on
- Performance verification and debug
- Consolidation and production worthiness.

The turn-on stage, typically lasting a few weeks before and after first silicon, involved putting together a very basic screen test consisting of continuity test, reference voltage verification, digital functional vectors, and tests for signs of life from the analog blocks. Simplicity of the initial analog tests was necessary to get screened parts into the customer's hands quickly. We discovered that development of complex analog tests required an intimate knowledge of the tester and the overall function of the chip, the main challenges being getting the chip into the desired state, constructing the correct analog stimulus, and synchronizing the analog and digital inputs.

The performance verification and debug stage of test development lasted from after the initial prototype shipments until artwork release for the final chip revision. During this stage, digital and analog static current tests were debugged, pad leakage tests were added, and any remaining digital functional tests were added, but the majority of time was spent adding complexity and refinements to the original analog tests and creating new analog tests to verify that all analog functions met the required specifications. Often this activity was interrupted by the need to create specific tests to debug unexpected behavior discovered either by the customer or the test development process. In the case of the read channel ASIC, the customer provided a test harness that could be used to power up the chip, write to registers, and view outputs while stimulating the analog inputs. This proved to be very useful for debug activities. However, there were several cases in which the HP 9490 tester's ability to control the timing of analog inputs and capture outputs on a cycle-by-cycle basis was invaluable in isolating design bugs or marginalities.

During the final test development phase, the many analog functional and debug tests were consolidated into fewer, more efficient tests. For both ICs, we retained the capability of putting the test programs in a debug mode in which additional data is saved in diagnostics files and captured waveforms are saved for viewing.

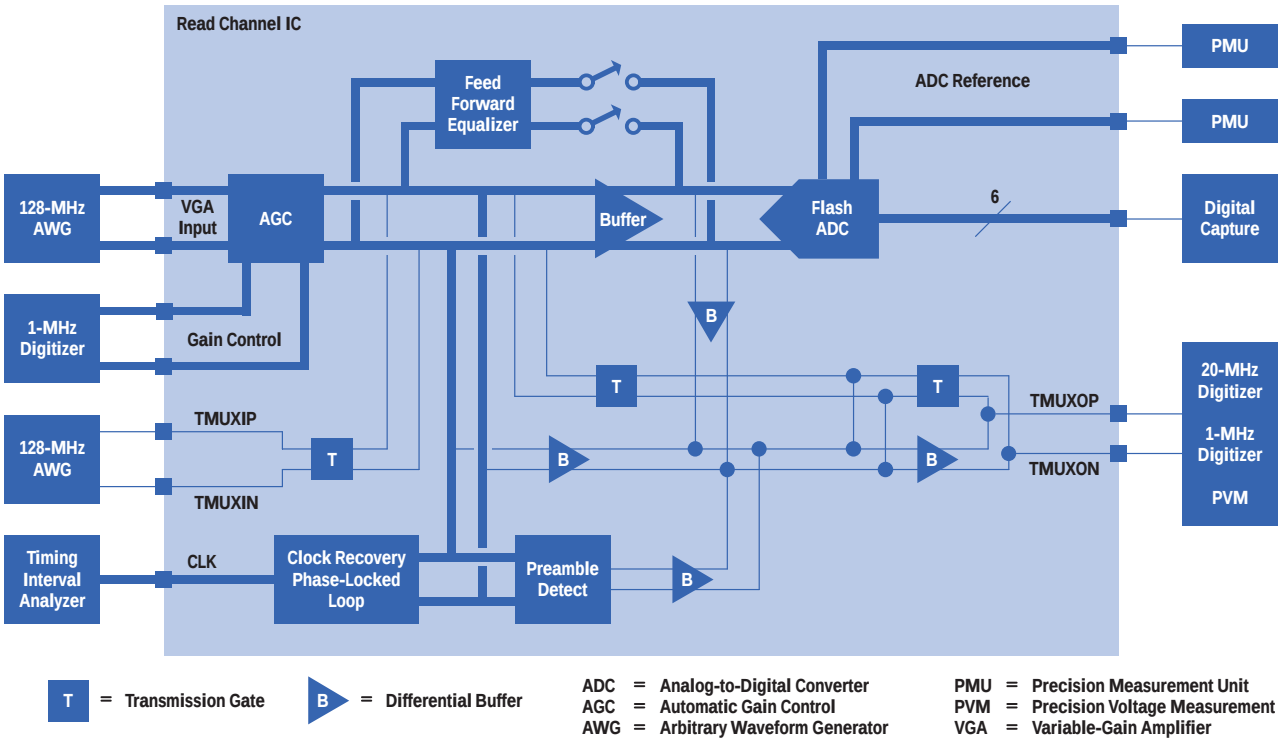
Analog Test Strategy

The strategy used for guaranteeing that the analog blocks were defect-free was first to measure the analog supply current in both the static (power-down) and power-on states, and second, to generate functional tests that both isolate subblocks and mimic customer use to verify all specifications listed in the ERS. The general premise was that a manufacturing defect would cause an individual subblock such as an op amp or comparator or a larger functional block to produce an unexpected output or compromised performance. An unexpected output might be an incorrect comparison, an incorrect dc level, excessive offset, instability, or an unavailable mode of operation. Compromised performance might be measured in terms of gain, linearity, dynamic range, resolution, settling time, bandwidth, acquisition range, detection threshold, or some other appropriate measure. Very often, individual subblocks cannot be specifically isolated, but their performance can be inferred from higher-level tests that exercise the subblocks in a variety of ways.

Any attempt to assess test coverage must first consider how a possible defect could manifest itself at one of the observation ports. The observable effect of a given type of defect will vary depending upon several factors, including the function of the block and the location of the defect. Generally speaking, in a fully differential circuit such as the read channel AGC, a defect that occurs in the differential signal path is likely to cause some type of offset, whereas a defect occurring in common-mode circuitry, such as bias

Figure 1

Read channel analog signal path with simplified test access circuitry and HP 9490 analog resource utilization.



circuits, or single-ended signal paths is likely to cause faults such as improper dc or common-mode voltages, excessive current, or reduced range of operation.

Specification limits are set based upon both the customer's performance requirements and the observed distribution of the test parameters during characterization testing. Test specification windows must be set wide enough to cover expected process variations, provided that there is adequate performance margin, but narrow enough to weed out defects that cause "soft" faults. Of course drawing the line between process variation and soft faults is a tricky business, which can be mitigated to some extent by multiple tests with overlapping coverage of potential defects.

Testing the Read Channel IC

For a complex analog system such as a PRML read channel, it was necessary to design in test access points that allowed the inputs and outputs of functional blocks to be stimulated and measured as directly as possible. Such access proved invaluable in debugging and verifying that the individual blocks met their respective design goals. It was also useful for achieving a level of test coverage adequate to meet quality goals. The read channel design includes an analog test multiplexer with programmable ac and dc test paths for bypassing analog blocks and observing internal nodes (**Figure 1**). The ac test paths are isolated from the main signal path by transmission gates (T) and wideband differential buffers (B). Two pads (TMUXOP and TMUXON) dedicated to observing analog voltages have a pair of wideband ac buffers capable of driving the tester load, including the 10-kΩ input impedance of the HP 9490 20-MHz digitizer. Auxiliary differential input pads (TMUXIP and TMUXIN) allow the AGC block to be bypassed and the ADC, preamble detector, and clock recovery block inputs to be driven directly. Individual control of all transmission gates in the test path allows calibration of the dc offset of the buffer paths. The read channel IC also includes a digital test multiplexer that directs digital outputs generated by analog blocks to test pads.

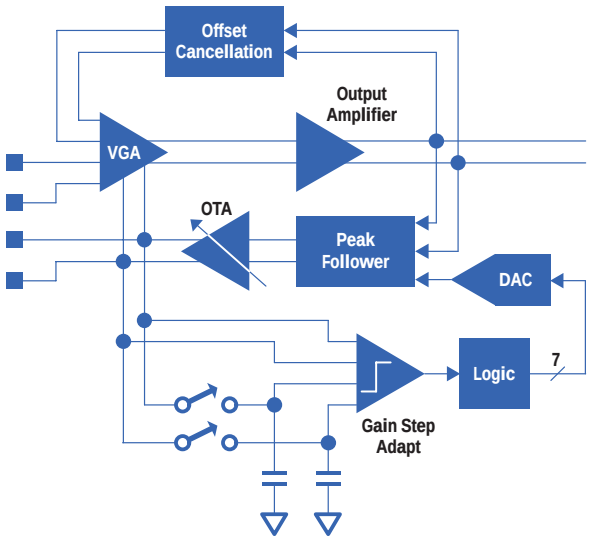
Additional constraints placed on the design of the analog blocks were that (1) they needed to be individually powered down to a state in which they drew no current from the analog supply, (2) analog outputs were tristated (in a high-impedance state), and (3) digital outputs were driven to the rails. Also, the current drawn by any block from the analog supply was required to be proportional to a reference current set by an on-chip bandgap reference and an external precision resistor.

Testing the Read Channel AGC

The AGC block, pictured in **Figure 2**, is one of the most complex analog systems tested on the ICBD HP 9490 testers. It includes a fully differential four-stage variable-gain amplifier (VGA) with a gain range of 12 dB to 32 dB, a fixed-gain linear output amplifier, continuous-time global offset cancellation, a peak follower for amplitude detection, a programmable operational transconductance amplifier (OTA) for multiple loop bandwidth selection, a 7-bit DAC for output amplitude setting, and circuitry that adaptively eliminates the gain step that occurs at the DAT preamble-data boundary.

Figure 2

Read channel AGC (automatic gain control) block diagram.



DAC = Digital-to-Analog Converter
OTA = Programmable Operational Transconductance Amplifier
VGA = Variable-Gain Amplifier

The specifications used to design this block were used as a guide for developing the test routines for debug and performance verification and finally for production screening tests. The three test input ports for the AGC block are the VGA input, the gain control input, and the digital input to the reference DAC. The test output ports include the amplifier chain output, the peak follower output, the DAC output, the loop filter output, and the output of the gain step adaption comparator. Needless to say, this leaves many internal circuit nodes that can only be observed through their interaction with the outputs of major subblocks.

The AGC block test is separated into several subtests which individually target the amplifier chain including offset cancellation, the peak detector, the AGC loop, the gain step adaption circuit, and the DAC. In many cases, a subtest will exercise a large portion of the AGC system to produce the stimulus needed to extract the performance measure of a particular subblock. This results in an overlap in coverage, which increases overall test coverage. The amplifier chain is tested by allowing the AGC loop to lock separately to three different ~2-MHz sine waves with input amplitudes covering the extremes and center of the VGA input dynamic range. The amplifier output is digitized for the three different inputs by an HP 9490 20-MHz digitizer through the analog test multiplexer output pads. A fast Fourier transform (FFT) is performed on the three sets of digitized data to extract the output amplitude, offset, total harmonic distortion (THD), and signal-to-noise ratio (SNR), which are all compared against pass/fail limits. Additional measurements are made of the amplifier output common-mode level and of the test buffer path offset for correction of the amplifier chain offset measurements. This series of tests provides wide coverage of potential defects in the amplifier chain and the rest of the AGC loop.

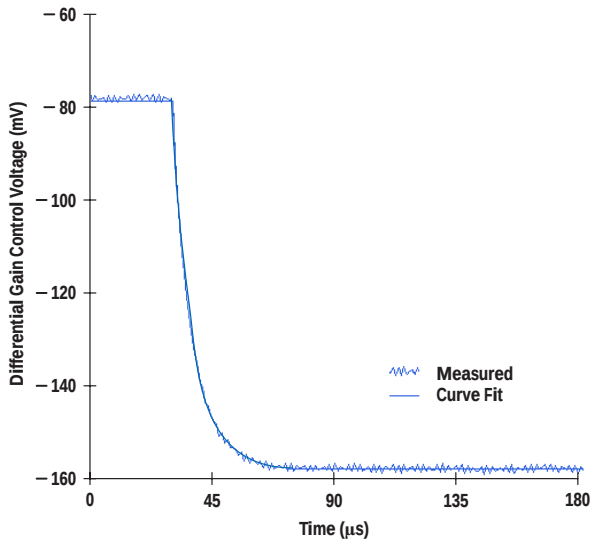
The decay rate of the peak follower output is an important parameter because it determines how the AGC loop will respond to the varied and sometimes sparse peaks of digital audio tape (DAT) data. For this reason, a specific test was written to extract the decay rate from a digitized peak follower output with the AGC loop locked to a 1-MHz sine wave. Another key parameter for the DAT read channel is the accuracy of the AGC loop bandwidth

settings, especially in the low-bandwidth mode, which is the primary mode of operation during a read cycle. The loop bandwidth is most easily measured by monitoring the VGA control voltage when a step in input amplitude is applied to the VGA input. A low-frequency (1-MHz), high-input-impedance (1-MΩ) digitizer was used for this task. Since the AGC loop bandwidth is directly proportional to the gain control sensitivity of the VGA, the measurement was performed three times with minimum, nominal, and maximum VGA input amplitudes. The input signal chosen was a 9-MHz sine wave (same frequency as the DDS3 format preamble) with a 2-dB amplitude step after the loop was initially settled. **Figure 3** shows the differentially digitized gain control voltage during an input step, as displayed by the HP 9490 waveform editor. Also plotted is the exponential curve fit extracted from the digitized data by a simple C routine in the test program. The curve fit is performed to approximate the loop time constant and hence the loop bandwidth.

As previously mentioned, the AGC loop bandwidth is programmable by selection of different values of transconductance of the loop transconductance amplifier. The faster-bandwidth modes are selected by on-chip state machines at the beginning of each track read when the AGC must quickly acquire lock from the absence of signal to a preamble segment at the beginning of each track. A test was written that simulates this condition by driving the VGA input with a low-amplitude noise signal followed by a maximum-amplitude preamble signal with an exponential turn-on envelope. This is the most taxing situation for the AGC loop because it must go from a condition in which the VGA gain control is railed to being settled in the minimum-gain condition in a short period of time (before the end of the preamble). The preamble detector block and on-chip state machines are enabled during this test so that the loop bandwidth switching occurs as it does in normal use. The gain control voltage is digitized and then processed by C code to verify that the gain has settled to within the acceptable limit before the end of the minimum length preamble.

Figure 3

Measured AGC gain control voltage during a 2-dB step in input amplitude.



Additional tests are implemented that fully exercise the reference DAC, the gain step adaption comparator, and the analog signal path from the VGA through the on-chip ADC.

Testing the Read Channel Phase-Locked Loop

The read channel IC includes a mixed analog and digital phase-locked loop block, which recovers the clock signal from the DDS-format data stream. The recovered clock period is quantized in increments of one-sixteenth the external system clock. The phase-locked loop maintains the phase relationship between the recovered clock and the data stream by interspersing short (15/16) or long (17/16) clock periods with nominal clock periods. Taking advantage of the capabilities of the HP 9490 timing interval analyzer, a test was written that measures the period of each recovered clock cycle with the phase-locked loop locked to a sine wave having a period 2.5% shorter than the nominal data period. **Figure 4** shows the resulting histogram of recovered clock periods (as displayed in the HP 9490 waveform editor). The overall mean clock period is calculated to verify that the recovered clock frequency is 2.5% higher than the system clock frequency. The standard deviation of the short clock periods is tested against pass/fail limits as a measure of the uniformity of the delay elements of the 16-tap analog delay line within the clock recovery block. Additional tests were written that (1) individually verify the thresholds of the 32 comparators in the phase-locked loop phase sampler, (2) verify that the phase-locked loop can acquire lock to sine waves with the

Tester Description

At the HP Integrated Circuit Business Division, HP 9490 mixed-signal testers are nominally equipped with the following resources:

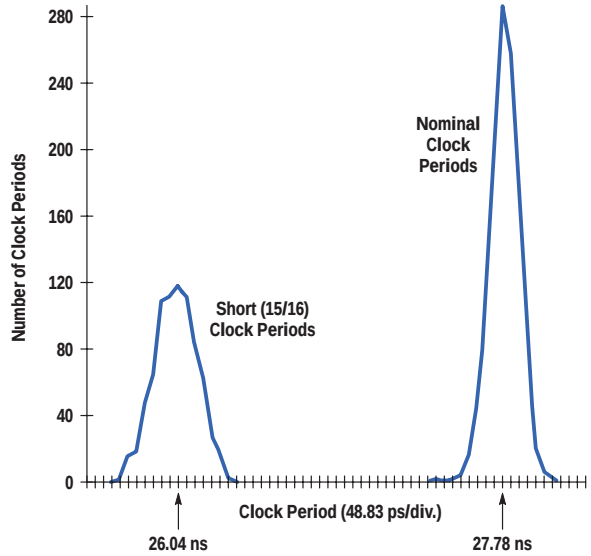
- Two 128-MHz dual-channel 12-bit arbitrary waveform generators (AWG)
- Two 1-MHz dual-channel 18-bit AWGs
- Two 20-MHz dual-input 12-bit digitizers
- Two 1-MHz dual-input 16-bit digitizers
- Two 1-GHz-bandwidth, 1-MHz-rate samplers
- One multiplexable dual-channel time measurement unit (TMU)
- One multiplexable dual-channel timing interval analyzer
- One precision voltage measurement unit
- One precision voltage source
- Two fixed and one multiplexed universal dc precision measurement units (PMU)
- Four dual-output DUT power supplies (DPS).

The test head includes 128 pins with per-pin dc function control. The maximum digital test frequency is 64 MHz (128 MHz with pin multiplexing) with edge and format changing on the fly. Vector depth is 4M bytes per pin. The digital test subsystem includes debugging tools such as shmoo plots, sequence debugger with fail mapping, and digital waveform display. Especially useful for testing of ADCs is the digital data capture capability with 500K-byte depth and special hardware for high-speed digital signal processing.

maximum expected frequency offset, and (3) measure the accuracy of the phase-locked loop phase offset setting by examining the phase at which the on-chip ADC samples a sine wave to which the phase-locked loop is locked.

Figure 4

Histogram of 2000 recovered clock periods.



Read Channel Test Summary

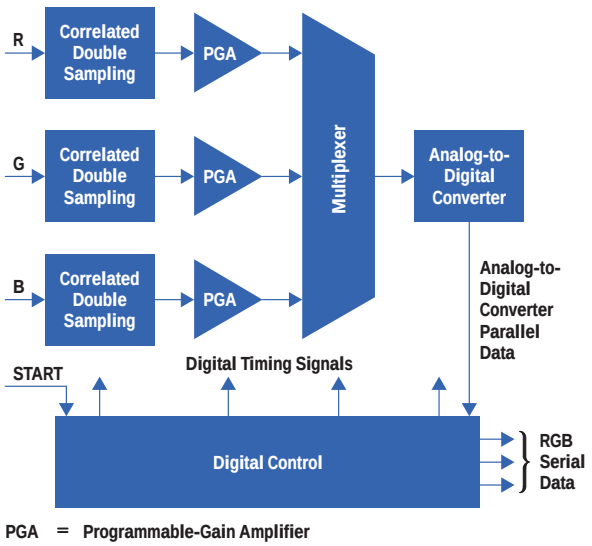
The final read channel production test is composed of 22 analog subtests, a digital scan subtest, 18 functional digital subtests, and three additional subtests for continuity, pad leakage, and static current. The overall test execution time is just under 7.5 seconds, with approximately 5.5 seconds for the analog tests, 0.5 second for the digital tests, and 1.5 seconds for the remainder.

Testing the CCD Signal Processor IC

The CCD signal processor is a CMOS-based monolithic IC that interfaces color (RGB) signal outputs from a CCD to a main ASIC.[5] The major components of this IC are three switched-capacitor 8-bit programmable gain amplifiers (PGAs), a 10-bit successive approximation ADC, and a 6-bit utility DAC (**Figure 5**, DAC not shown). The three PGAs perform 8-bit programmable offset compensation and 8-bit programmable amplification on the correlated double-sampled CCD signal. The ADC digitizes each of the PGA outputs in sequence, and the 10-bit converted codes for the RGB signals are serially output on three I/O pins. The correlated double sampling and amplification stage can be pipelined with ADC conversion and serial data output to maximize throughput.

Figure 5

CCD (charge-coupled device) processor signal path block diagram.



Signal Path

A typical CCD signal sampling sequence with this IC is as follows. The R (or G or B) signal is first held by the CCD at its black level, corresponding to the voltage output from the CCD pixel under no illumination. Then the CCD outputs transition to the video level, corresponding to the integrated illumination on that pixel. This complete single-pixel output cycle is initiated by the START pulse from the main controller IC.

To perform correlated double sampling, the black level from each pixel is sampled and subtracted from the sampled video level by the IC. The positions of the black sample point and the video sample point are 8-bit programmable in terms of the number of cycles from the end of the START pulse. The difference between the black and video levels for each pixel is amplified by the PGAs and then sampled and converted by the ADC.

Testing the CCD Signal Path

Because of test time limitations, we employed simplified versions of ramp and sinusoidal tests to test the IC signal path. We will describe the sinusoidal test here. It is assumed that the reader is familiar with concepts of ADC quantization noise.

Theory of Sinusoidal Test. The interested reader is referred to several excellent publications on ADC testing.[6-10] Briefly, the quantization noise of an ADC with a truly random input can be shown to have a mean square variance (or noise power) of $\Delta^2/12$, where Δ is the least-significant bit. By selecting a sine wave frequency that is not harmonically related to the sampling frequency, we can achieve quasirandom sampling over several cycles of the sine wave, and the ADC quantization noise power will approximate $\Delta^2/12$. We also assume that the sine wave exercises the full ADC range, that is, its peak amplitude is $2^N\Delta/2$, where N is the number of bits. Then:

$$\text{Signal Power} = 2^{2N-3} \times \Delta^2 \quad (1)$$

$$\text{Noise Power} = \frac{\Delta^2}{12} \quad (2)$$

$$\text{SNR (dB)} = 6.02N + 1.76. \quad (3)$$

The signal-to-noise ratio (SNR) provides a quantitative measure of the performance of the ADC. For example, an ideal quantization noise limited 10-bit ADC should yield an SNR of 61.96 dB. The practical IC signal path, however, will have its SNR limited by impairments such as random noise (fundamental and circuit-induced), distortion (from device nonlinearities), component mismatches, sampling time jitter, and so on. A measure of the actual performance of the IC signal path can be derived by calculating the effective number of bits (ENOB) from the measured signal-to-noise + distortion ratio (SNDR) as follows:

$$\text{ENOB} = \frac{\text{SNDR (dB)} - 1.76}{6.02}. \quad (4)$$

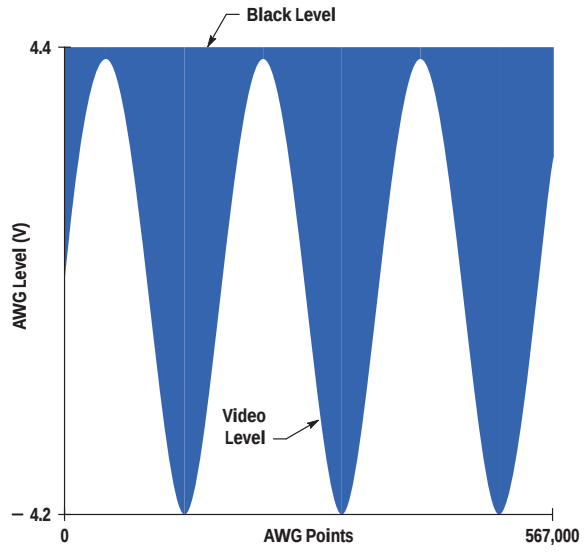
Alternatively, the ENOB can also be calculated by comparing the measured noise + distortion power, ND_{meas}, to its ideal value, $N_{ideal} = \Delta^2/12$:

$$\text{ENOB} = N - \log_2\left(\frac{ND_{meas}}{N_{ideal}}\right). \quad (5)$$

This method is chosen for calculating ENOB because it does not require the signal path to be driven over its full range, eliminating the possibility that the PGA and ADC might be overdriven and clipped, yielding an inaccurate SNDR.

Figure 6

Sinusoidal test AWG (arbitrary waveform generator) waveform.



Test Signal Generation. It is assumed that the black and video sampling positions are chosen such that all transients associated with the black and video level transitions are settled. As such, the signal path is insensitive to the frequency of the input signal (up to the Nyquist rate). A 128-MHz 12-bit arbitrary waveform generator (AWG) was used to generate a sine wave created from data points generated by a custom program. The AWG rate and the digital clock were set to 20 MHz, and a sine wave of about 1 kHz was used. The number of points digitally captured was limited to 1024 to reduce test execution time. This number must be a power of 2 to use the HP 9490's built-in FFT routines effectively.

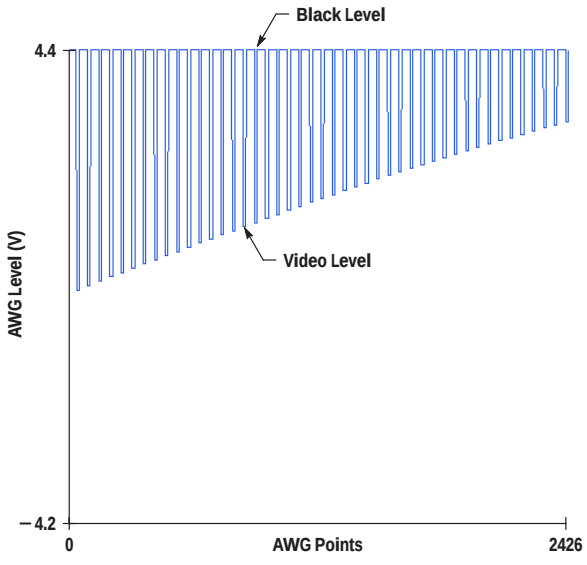
The IC's signal path range is 0 to 2.5V (ac coupled), while the AWG range is −4.4V to +4.4V. To maximize the resolution of the AWG waveform, the sine wave was generated over the full AWG output range, with the AWG internal attenuator set to −10.93 dB. This results in a maximum-resolution AWG signal that is within the input range. However, to avoid inadvertent clipping, which may result from PGA or ADC gain errors or offsets, we limited the sine wave amplitude to 95% of the full AWG range. In the initial stages of test development, we monitored the SNDR of the AWG waveform and found that its ENOB was nearly 11 bits. The noise input power of the AWG was subtracted from the measured signal path noise power to yield the effective measured noise power ND_{meas}, which was then used to calculate the ENOB. We assumed that the AWG noise was independent of the signal path noise.

Various low-pass filters (up to 132 MHz) are available to improve the SNR of the AWG output waveform, but they were not used in this test because of the sharp transitions required between black and video levels. **Figure 6** illustrates the 1-kHz waveform created for the AWG, while **Figure 7** shows the details of the waveform near its start. The difference between the black level (4.4V) and the sine wave envelope constitutes the input sinusoidal signal. The maximum rate of change of this waveform is about 8.6V/50 ns = 172V/μs, which is well within the slew rate of the AWG (600V/μs).[11]

Test and Data Analysis. The START pulse, which initiates the CCD signal processor conversion cycle, must be synchronized to the AWG waveform. The AWG must be started at the same time as the first START pulse, and subsequent START pulses must be synchronized with the beginning of each black level in the AWG waveform. The HP 9490 tester allows synchronization between the AWG, the digital pattern generator, and other mixed-signal

Figure 7

Zoomed-in sinusoidal test AWG waveform.



resources to within 1 ns when one master clock is used. This resolution limit increases to the master clock period (7.8 ns) when two master clocks are required to implement the test. This synchronization feature is fully exploited in the test. The serial data output of the IC is read into the HP 9490 digital capture memory and retrieved into the test workstation memory for analysis. A typical retrieved waveform and its Fourier spectrum are shown in **Figure 8**.

Fourier analysis of the retrieved waveform is performed by built-in digital signal processing (DSP) algorithms. The fundamental amplitude, phase, dc offset, SNDR, total harmonic distortion (THD), second-harmonic distortion (2HD), and third-harmonic distortion (3HD) are extracted by customized routines that call upon built-in discrete Fourier transform (DFT) routines using FFT methods. It is not necessary to capture an integral number of cycles, since the custom routine has a built-in Hanning windowing function.[8]

The total noise + distortion power is calculated from the fundamental amplitude and SNDR value, and is corrected for the noise power of the AWG. The ENOB is calculated using equation 5. The ENOB for the case shown in **Figure 8** is approximately 8.4 bits, corresponding to a PGA and ADC SNDR of about 52.3 dB. The THD measured is −53.1 dB, while the 2HD is −56.6 dB (**Figure 8**). This particular IC's PGA and ADC performance is thus distortion-limited. Although THD, 2HD, and 3HD are not tested parameters, they provided invaluable insight into the source of SNDR limitations during the debug phase. The integral nonlinearity (INL) error profile can be obtained by subtracting the retrieved waveform from the fundamental, and the maximum and root mean square INL error can be derived. A typical INL error profile is shown in **Figure 9**. We did not test all of the 1024 ADC codes. Differential nonlinearity (DNL) errors can be calculated from similar INL profiles obtained from high-resolution ramp tests.

The parameters tested in the sinusoidal production test are fundamental amplitude, ENOB, and maximum INL error. The dc offset, THD, 2HD, and 3HD are used for debugging purposes only, and are saved into diagnostic files during nonproduction debug modes together with fundamental amplitude, ENOB, maximum INL error, and the various waveforms illustrated here (e.g., **Figures 8 and 9**).

The HP 9490 mixed-signal tester allows optimization (minimization) of test time by pipelining digital pattern execution times with data analysis. The benefit of doing this in our case was minimal, since pattern execution

Figure 8

A waveform retrieved from the ADC and its spectrum.

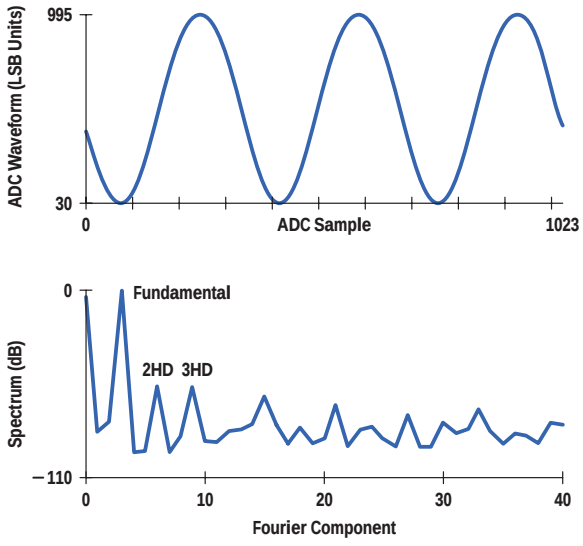
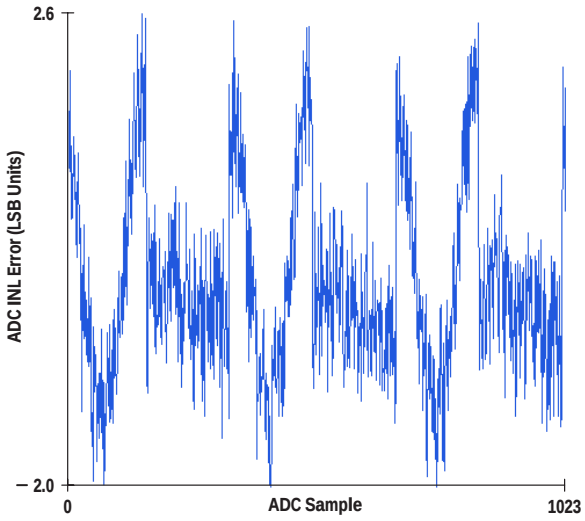


Figure 9

Sinusoidal test INL (integral nonlinearity) error.



times were extremely fast compared to data analysis times. The total production test time of this IC on the HP 9490 tester was about two seconds.

Conclusion

Mixed-signal test is a developing field within ICBD with many interesting challenges and room for advances in theory, methodologies, and standardization. The HP 9490 tester has been proven to be a very capable platform for testing complex analog circuitry as demonstrated by both the PRML read channel and CCD signal processor projects. Provisions made for controllability and observability of analog signals during the design process can yield highly testable designs. However, the development of mixed-signal tests continues to be a custom process requiring detailed knowledge of both the tester and the circuit under test.

Acknowledgments

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