Theory and Design of CMOS HSTL I/O Pads

Gerald L. Esch, Jr.

Robert B. Manley

To control reflections, the impedance of integrated circuit output pad drivers must be matched to the impedance of the transmission lines to which the pads are connected. HP's HSTL (high-speed transceiver logic) controlled impedance I/O pads use an on-chip impedance matching network that compensates for process, voltage, and temperature (PVT) variations.

Transmission line reflections are one of the major factors limiting high-speed I/O performance. These reflections can be controlled by matching the driver output impedance to that of the transmission line. Traditional solutions require the use of off-chip components to implement matching termination networks. This adversely impacts board density, reliability, and cost. Integration of the termination network on-chip removes these negative attributes while providing additional advantages.

In this paper, we review a solution for an on-chip impedance matching network. Our HSTL (high-speed transceiver logic) family of controlled impedance I/O pads includes single-ended and differential drivers and receivers, along with compensation circuitry for process, voltage, and temperature (PVT) variations. Measured HSTL signal integrity in a large, complex board environment is presented.

Parallel versus Series Termination

When I/O signal integrity and speed are of utmost importance, many pad designers turn to parallel termination networks. Parallel termination eliminates transmission line reflections. However, parallel termination exacts a costly toll on power dissipation because a dc component is added to power consumption. An alternative termination approach is source series termination. In a point-to-point environment, series termination provides an output driver with a means to absorb incident waves, effectively damping any reflections in the transmission line. Matching a driver's output impedance to that of the board impedance increases signal integrity and speed while keeping power dissipation to a minimum.

Gerald L. Esch, Jr.
Jerry Esch is a hardware design engineer with the HP Integrated Circuit Business Division, specializing in high-speed graphics ASIC design, high-speed CMOS I/O pad design, and real-time MPEG encoding. Born in Kearney, Nebraska, he received his BSEE degree in 1992 from New Mexico State University and joined HP in 1994. He is a volunteer with the Special Olympics.

Robert B. Manley
Bob Manley is a VLSI design engineer with the HP Integrated Circuit Business Division. He holds BS degrees in physics (1975) and electrical engineering (1979). He joined HP in 1979. Born in South Bend, Indiana, he is married, has two children, and is a pilot and a competitive rifle and pistol shooter.

Source series termination is easily implemented with two components: a low-impedance output driver and a precision series resistor. To decrease factory costs and conserve board space, it is desirable to replace the printed circuit board precision series resistor with an on-chip, PVT-compensating resistor.

Output Driver

The single-ended output driver, shown in **Figure 1**, has two major components: a push-pull driver and an on-chip series termination resistor. The three components that form the termination resistor are the driver NFET resistance R_{DS}, an n-well resistor R_{ESD} for ESD protection, and R_{PROG}, a programmable resistor between the nodes PRE and POST. Controlled by on-chip calibration circuitry, the programmable resistor takes on a range of resistances to ensure that the driver's output impedance R_o matches the transmission line impedance Z_o. This allows reflections to be completely absorbed in the driver regardless of process, temperature, and voltage fluctuations. Thus:

$$R_o = R_{DS} + R_{PROG} + R_{ESD} = Z_o.$$

R_{PROG} is tuned by turning on and off various combinations of transfer NFETs with a six-bit binary word. Each bit in the binary word, PROG[5:0], controls a transfer gate in the programmable resistor array. The NFETs have conductances corresponding to their binary weighted bit positions in PROG[5:0]. For example, if PROG[0] controls a transfer gate with conductance of G, then PROG[1] controls a transfer gate with a conductance of 2G. The resistance of R_{PROG} decreases as the binary count PROG[5:0] increases. In effect, as the binary count increments, more resistors are added in parallel in the NFET array.

Calibration Circuitry

The calibration circuitry (**Figure 2**) is designed to program all HSTL output driver impedances, R_o, to match that of an external precision resistor, R_{EXT}. During normal operation, an enable signal, CAL, causes an NFET equivalent in size to an HSTL output driver pull-up NFET to conduct. Current begins to flow through the I/O pad through R_{EXT}. This current path forms a voltage divider, where:

$$V_{PAD} = V_{DDQ}\frac{R_{EXT}}{R_{EXT} + (R_{DS} + R_{PROG} + R_{ESD})},$$

or

$$V_{PAD} = V_{DDQ}\frac{R_{EXT}}{R_{EXT} + R_o}.$$

Figure 1

Single-ended output driver.

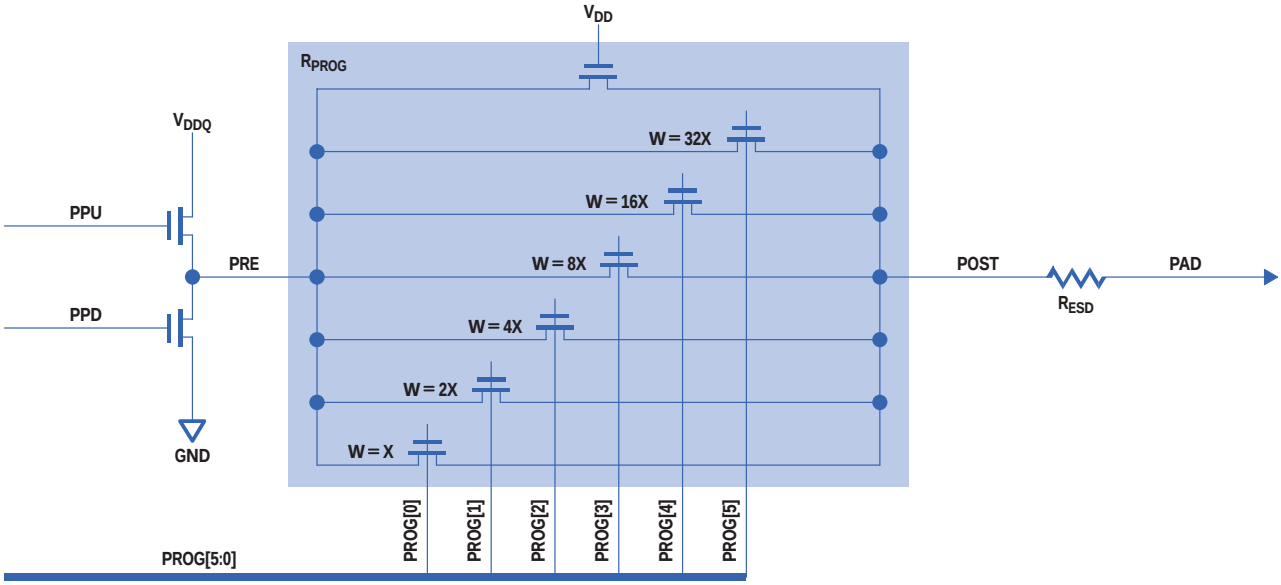
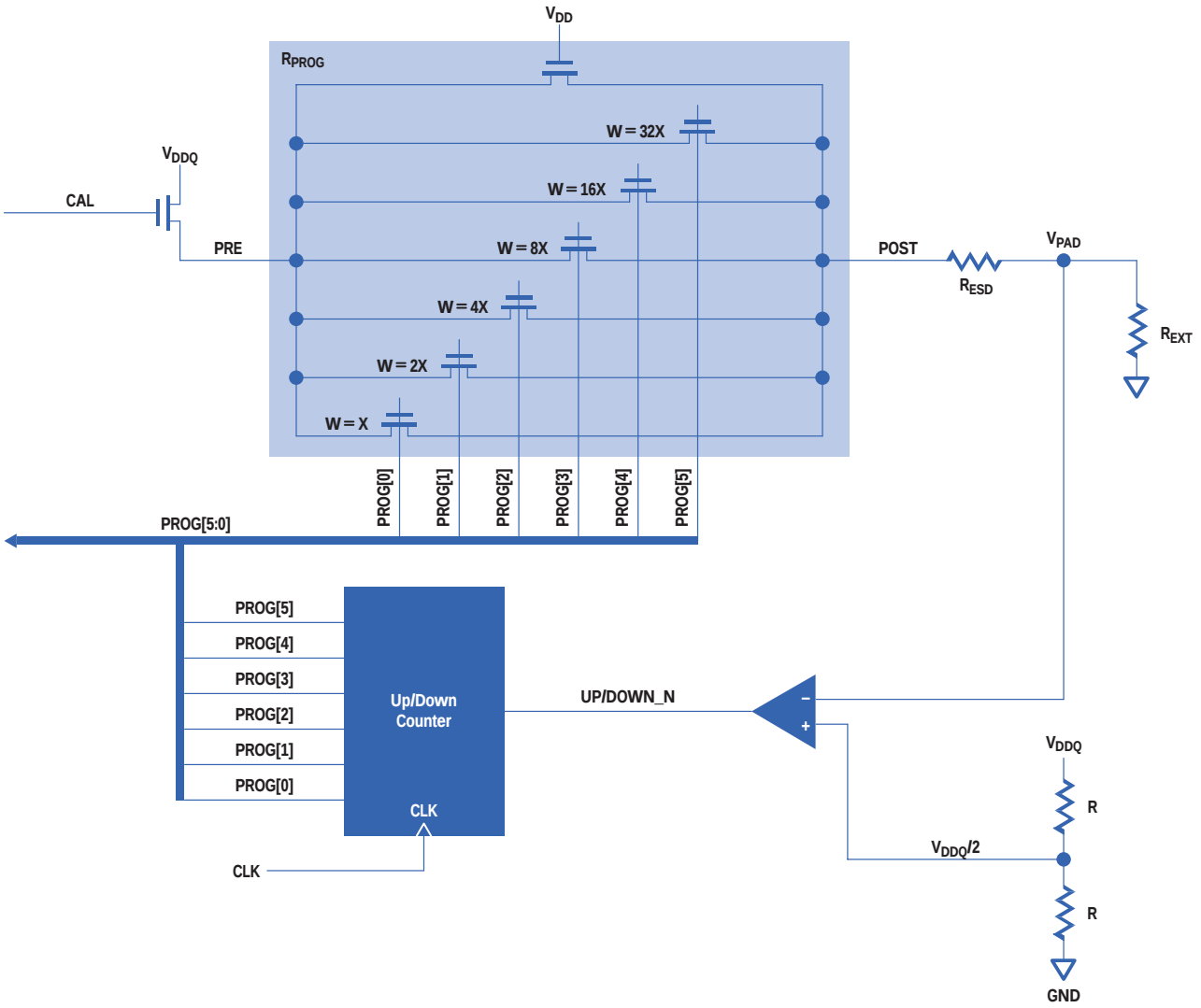


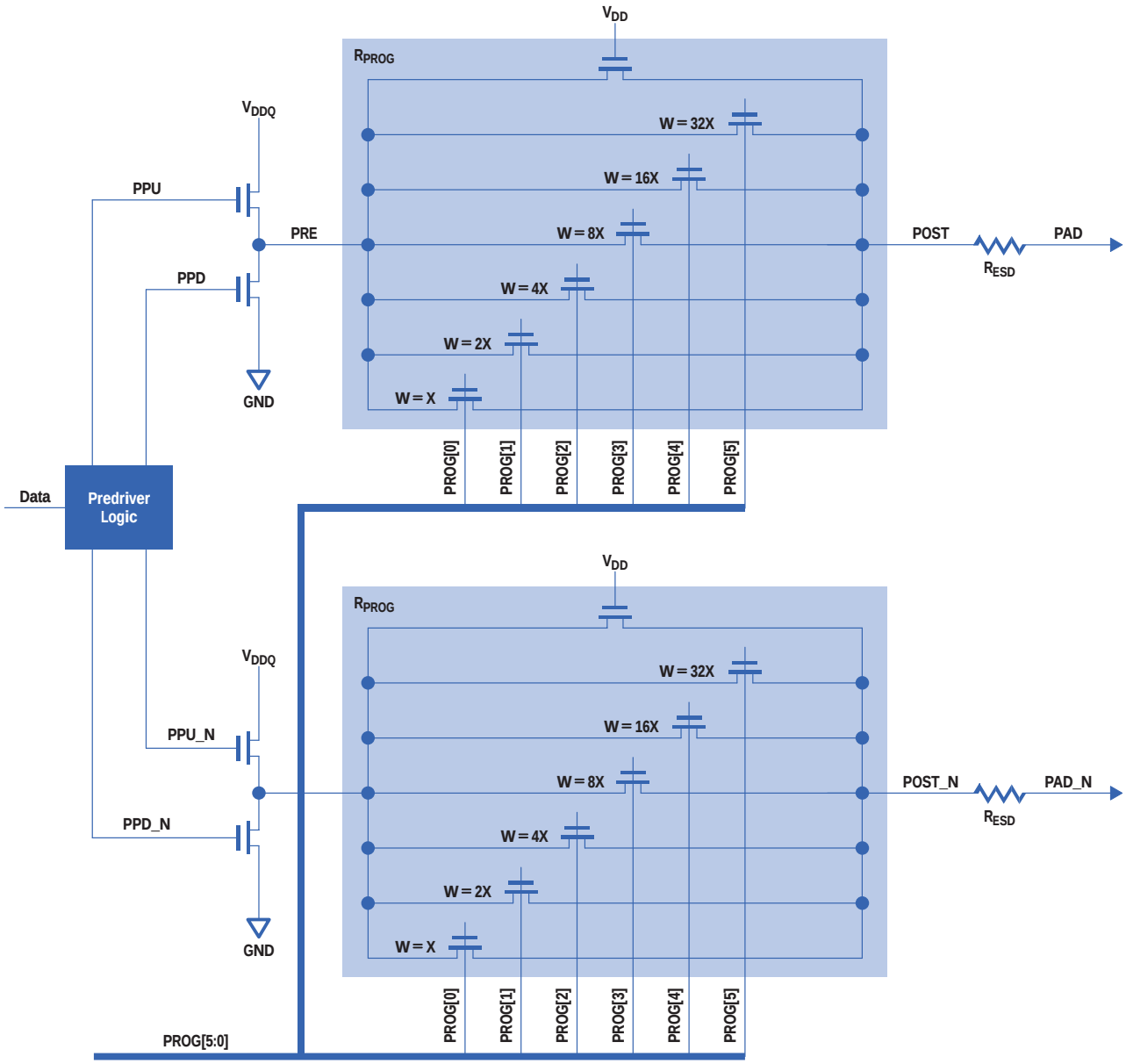
Figure 2
Calibration circuitry.



V_{PAD} serves as an input to the inverting terminal of the differential amplifier. The noninverting terminal's input voltage is $V_{DDQ}/2$. This reference voltage is generated on-chip via a voltage divider. Any difference between the input voltages of the differential amplifier is perceived as a resistance mismatch between R_o and R_{EXT}. The ΔV causes the differential amplifier's output to program an up/down counter to increment or decrement its six-bit output. Upon receiving a clock edge, the up/down counter drives a new six-bit binary count, PROG[5:0]. This calibration word is used by the calibration circuitry's programmable resistor and distributed to other HSTL driver programmable resistors. Incremental binary changes in PROG[5:0] cause incremental resistance changes in the programmable resistor. Because R_{PROG} is now programmed to a new value, V_{PAD} obtains a new analog value. V_{PAD} again acts as an input to the differential amplifier and the impedance matching process starts over. The calibration action is continuous and transparent to normal chip operation.

Figure 3

Differential driver.



Differential Driver

The differential driver in **Figure 3** is the combination of two HSTL drivers. By knowing the driver's output resistance, an external parallel termination network can set the dc operating points to comply with the HSTL differential specification. The predriver logic is responsible for keeping the differential clock signals in conformance with the ac specification.

The predriver logic also performs two other important tasks. The single-ended-to-differential conversion preserves the input duty cycle while minimizing transients in the supply currents.

Figure 4

Single-ended waveform.

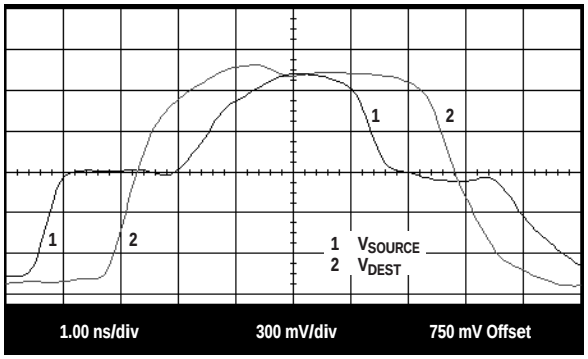
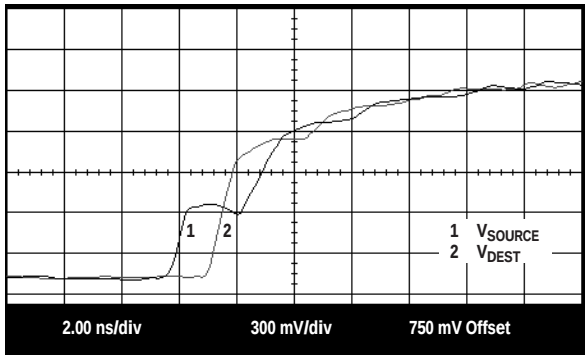


Figure 6

Overdamped signal.



Measured Results

Figure 4 depicts a single-ended signal traversing a 6-inch transmission line. V_{DEST} is the signal received at the end of the line. Signal integrity can be monitored by examining the location of the inflection point at the driver (V_{SOURCE}). An inflection point near half the high logic level ($V_{DDQ}/2$ for HSTL) indicates that the driver output impedance matches the transmission line impedance.

Figure 5 shows a differential signal after traveling down a 6-inch transmission line. V_{DEST} is consistently contained within the tight HSTL differential specifications because of the known differential driver output resistance.

Figures 6, 7, and 8 illustrate the effects of varying the driver's output impedance by changing the external calibration resistor, R_{EXT}. In **Figure 6** $R_{EXT} > Z_o$, in **Figure 7** $R_{EXT} = Z_o$, and in **Figure 8** $R_{EXT} < Z_o$. Signal integrity is maintained when the driver output resistance matches the transmission line impedance.

Future Work

One potential shortcoming of implementing a parallel NFET array to mimic a source series termination resistor is the variation in driver output resistance R_o. **Figures 9 and 10** show driver output resistance as a function of output voltage V_o. Ideally, R_o should be constant over the

Figure 5

Differential waveform.

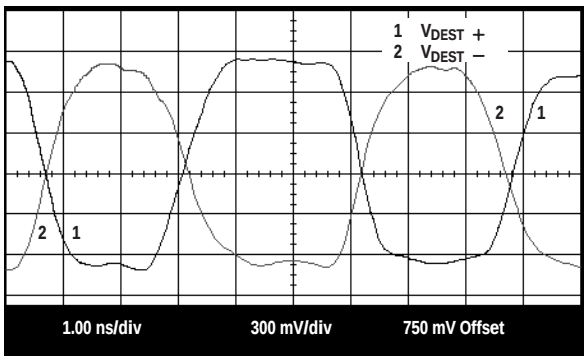


Figure 7

Critically damped signal.

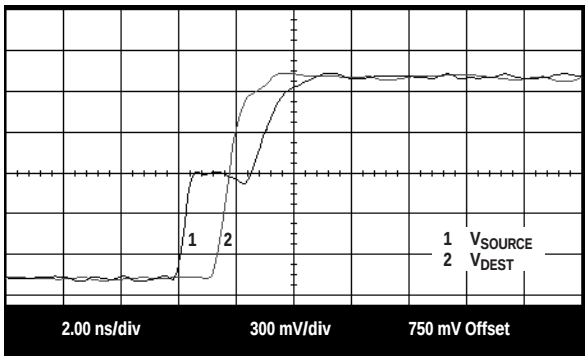
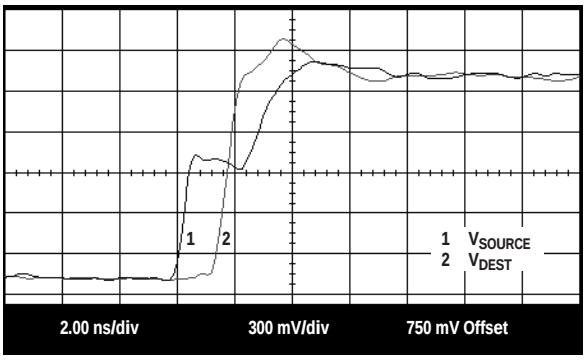


Figure 8

Underdamped signal.



range of V_o. However, R_o changes with variations in the values of V_{GS}, V_{DS}, and the back gate voltage of the transfer and driver NFETs. **Figure 9** shows the output resistance changing as the output voltage swings from 0.1V to 1.4V (10% to 90%). **Figure 10** illustrates the output resistance as a function of the output voltage swing from a logic high to a logic low. Notice in **Figure 9** that the point at which $R_o = Z_o$ (50Ω) occurs when $V_o = V_{DDQ}/2$. This is because the calibration circuitry tunes the programmable resistor with the pull-up portion of the output driver at $V_{DDQ}/2$. With proper driver width ratioing, the pull-down driver NFET would also have $R_o = 50\Omega$ at $V_o = V_{DDQ}/2$.

Figure 9

R_o as a function of V_o as V_o goes from a logic low to a logic high.

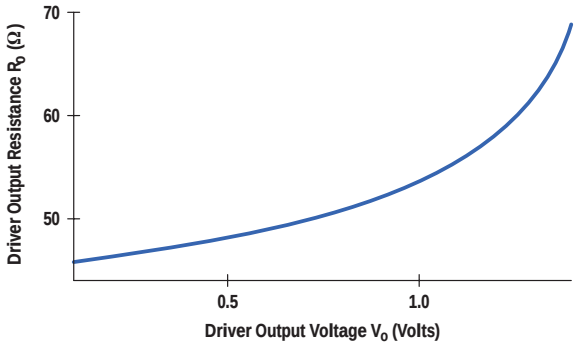
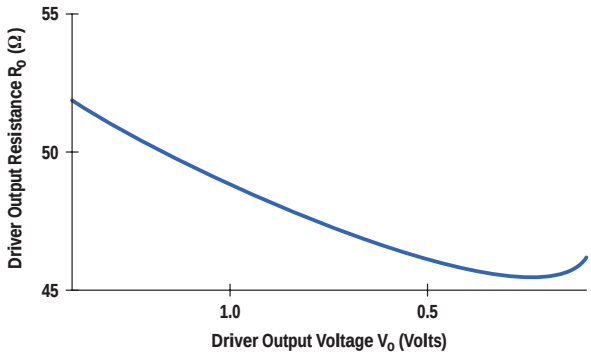


Figure 10

R_o as a function of V_o as V_o goes from a logic high to a logic low.



However, to help reduce variations in R_o, the crossover point was shifted towards the high logic level of V_o. For HSTL I/O applications, this inherent deviation in output resistance minimally affects signal integrity. For future applications, it may be worthwhile to investigate alternative series termination schemes for tighter impedance matching environments.

Conclusion

A parallel NFET array can be a simple and effective way of controlling a driver's output resistance. With an on-chip source series termination resistor, a chip can communicate at higher frequencies and board space that would normally contain termination networks is freed. Our family of HSTL pads has been proven to work at 200 MHz in large, complex board environments.

Acknowledgments

The authors wish to thank Gordon Motley for his valuable pad design and ESD advice, Rick Luebs for offering the original design concept, Rob Martin for his technical support, Ron Larson and Wally Wahlen for their characterization effort, Holly Manley for making the paper readable and Amy Jahnke for supplying direction. We also thank Gary Wetlaufer for his support.

Bibliography

1. G. Esch, Jr. and R. Manley, "HSTL CMOS I/O Pads for 200-MHz Data Rates." *Proceedings of the 1996 Hewlett-Packard Design Technology Conference*, pp. 51-58.

2. R. Canright, Jr., "The Impact of Driver Impedance upon Transmission Line Impedance," *Proceedings of the 44th Electronic Components and Technology Conference*, pp. 669-674.

3. *HSTL (High-Speed Transceiver Logic)*, JEDEC Standard 16.3, Draft Revision 3, JEDEC Council, July 14, 1994.

4. R. Wilson, "JEDEC ready to approve very-high-speed I/O spec," *Electronic Engineering Times*, December 5, 1994, p. 1.

▶ Go to Next Article

▶ Go to Journal Home Page