# On-Chip Cross Talk Noise Model for Deep-Submicrometer ULSI Interconnect

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A simple closed-form model for calculating cross talk noise on signal lines in deep-submicrometer interconnect systems has accuracy comparable to SPICE for an arbitrary ramp input rate. Interconnect resistance, interconnect capacitance, and driver resistance are all taken into account. The model is suitable for rapid cross talk estimation and signal integrity verification.

Interconnect geometry in deep-submicrometer integrated circuit technologies is being aggressively scaled down for wiring density, leading to high aspect ratios in metal lines.[1-3] For example, according to the Semiconductor Industries Association roadmap, metal aspect ratio is expected to reach 2:1 in the 0.25-μm technology generation and 3:1 by the year 2004. As a result of the increasing metal aspect ratio, capacitive coupling between neighboring signal lines increases and more cross talk noise is generated. With increasing edge rates and ground bounce in advanced technologies, cross talk will become a pervasive signal integrity issue.

Traditionally, SPICE simulations have been used to estimate cross talk noise in the signal lines. Although accurate, these simulations are time-consuming. When the number of signal lines easily exceeds one million as it does in today's advanced microprocessors, SPICE simulations are too inefficient to carry out for each line. A rapid and accurate cross talk noise estimation alternative is needed to ensure acceptable signal integrity in a limited design cycle time. In reference 4, a closed-form model based on RC transmission line analysis is presented. However, the driver modeling is not discussed and the analysis is limited to step response. Another model approximates the driver with a resistor and a ramp voltage source,[5] but signal line resistance is neglected. These approaches lack the accuracy needed in deep-submicrometer interconnect analysis.

In this paper we present a closed-form cross talk noise model with accuracy comparable to that of SPICE for an arbitrary ramp input rate. Interconnect resistance, interconnect capacitance, and driver resistance are all taken into account.

### Model for Timing-Level Analysis

First, we derive a closed-form expression for cross talk noise when the rise time at the aggressor *output* is known. A circuit schematic of this model is shown in **Figure 1**. In a typical electronic design automation environment, circuit timing simulators can provide a rapid and accurate estimate of the signal rise time at the output of a driver. This information significantly simplifies our driver modeling. An aggressor transistor is treated as a ramp voltage source, $V_s$ ($=V_{dd}/T_r$). A victim transistor is modeled as an effective resistance, $R_{vd}$. This value is taken to be the linear resistance for the p- or n-channel MOSFET, depending on the victim line's logic state. This driver resistance and the victim line resistance, $R_{vi}$, are lumped into a single resistance, $R_v$. $R_a$ is the line resistance of the aggressor. $C_a$ and $C_v$ are the lumped capacitance for the aggressor line and victim line, respectively, and $C_c$ is the coupling capacitance between the lines (**Figure 2**).

Based on the circuit in **Figure 1**, the cross talk noise voltage $V_x$ as a function of time t is expressed as:

$$V_x = \frac{R_v C_c V_{dd}}{\tau_0 T_r}\left(\tau_0 + \tau_1 e^{-t/\tau_1} - \tau_2 e^{-t/\tau_2}\right) \quad (1)$$

for $0 \le t \le T_r$, and as:

$$V_x = \frac{R_v C_c V_{dd}}{\tau_0 T_r}\left\{\tau_1\left[e^{-t/\tau_1} - e^{-(t-T_r)/\tau_1}\right]\right\} - \frac{R_v C_c V_{dd}}{\tau_0 T_r}\left\{\tau_2\left[e^{-t/\tau_2} - e^{-(t-T_r)/\tau_2}\right]\right\} \quad (2)$$

for $T_r \le t$, where $V_{dd}$ is the supply voltage, $T_r$ is the rise time at the output of the aggressor driver, and

$$\tau_0^2 = \left[R_a(C_a + C_c) + R_v(C_v + C_c)\right]^2 - 4R_vR_a(C_vC_c + C_vC_a + C_cC_a) \quad (3)$$

$$\tau_1 = \frac{\left[2R_vR_a(C_vC_c + C_vC_a + C_cC_a)\right]}{\left[R_a(C_a + C_c) + R_v(C_v + C_c) + \tau_0\right]} \quad (4)$$

$$\tau_2 = \frac{\left[2R_vR_a(C_vC_c + C_vC_a + C_cC_a)\right]}{\left[R_a(C_a + C_c) + R_v(C_v + C_c) - \tau_0\right]}. \quad (5)$$

The peak voltage, $V_{x,max}$, always occurs when $T_r \le t$. Therefore, by differentiating equation 2 with respect to t, we obtain:

$$V_{x,max} = \frac{R_v C_c V_{dd}}{\tau_0 T_r}\left[\varphi_1\tau_1\left(\frac{\varphi_1}{\varphi_2}\right)^{\tau_2/(\tau_1-\tau_2)} - \varphi_2\tau_2\left(\frac{\varphi_1}{\varphi_2}\right)^{\tau_1/(\tau_1-\tau_2)}\right], \quad (6)$$

Figure 1

*A circuit diagram for the cross talk models in this paper. In the timing-level model, the aggressor driver is modeled as a ramp input, $V_S$ ($=V_{dd}/T_r$), and $R_a$ is the line resistance of the aggressor. In the transistor-level model, $V_S$ is the ramp input to the aggressor driver, and $R_a$ is the sum of aggressor driver resistance $R_{ad}$ and the aggressor line resistance $R_{ai}$. In both models $R_v$ is the sum of the line and driver resistances. $C_a$ and $C_v$ are the lumped ground capacitances for the aggressor line and victim line, respectively, and $C_c$ is the lumped coupling capacitance.*

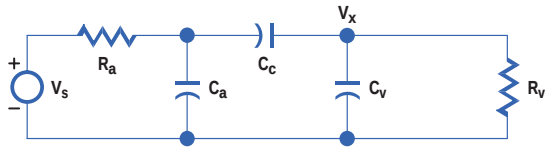



Figure 2

*A cross-sectional view of two lines above a ground plane considered in this study. The coupling capacitance $C_c$ is the source of on-chip cross talk noise. It is a significant fraction of total interconnect capacitance in deep-submicrometer interconnect technology.*

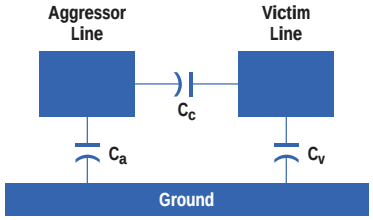
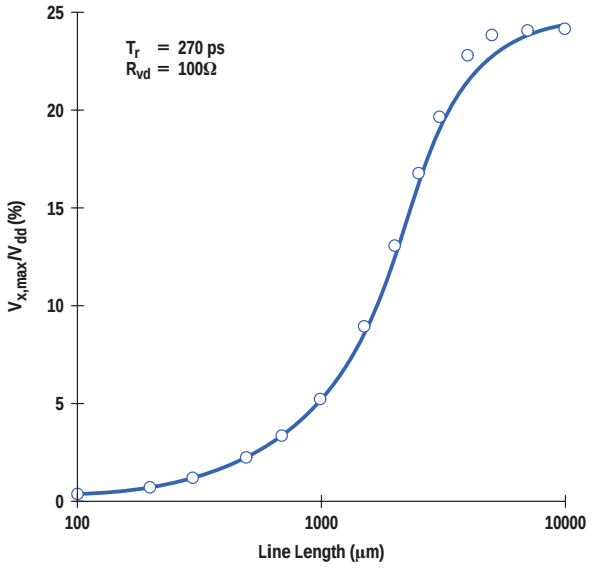


Figure 3

*Normalized cross talk noise voltage as a function of interconnect length. The model prediction is represented by a solid line and the SPICE simulations are represented by circles. The error of the model compared with SPICE is less than 10%. Cross talk noise increases sharply for line lengths over 1000 μm before reaching a saturation value.*




where $\varphi_1 = \exp(-T_r/\tau_1) - 1$ and $\varphi_2 = \exp(-T_r/\tau_2) - 1$. For a sufficiently slow rise time ($T_r \gg \tau_2$), $V_{x,max}$ approaches the limit of $R_v C_c V_{dd}/T_r$. Also, for a special case where $R_a = R_v$, $C_a = C_v$, and $T_r = 0$, equation 6 reduces to a simple model presented by Sakurai:[4]

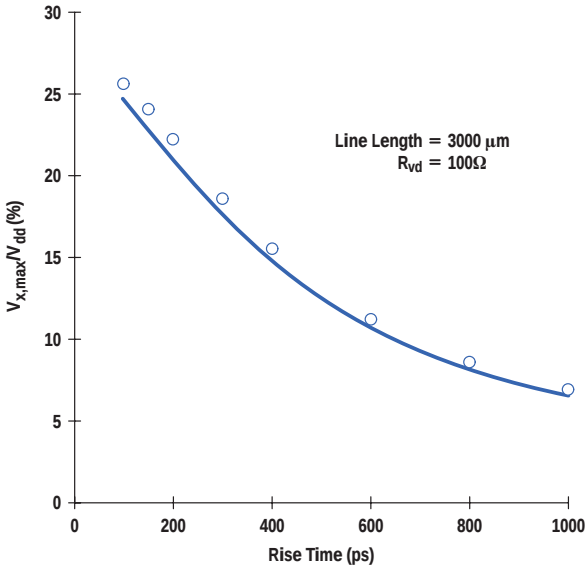
$$V_{x,max} = \frac{V_{dd}}{2}\frac{C_c}{C_a + C_c}. \quad (7)$$

The accuracy of the model of **Figure 1** is demonstrated in **Figure 3** and **Figure 4** for a representative cross-sectional geometry of a global line in 0.25-μm technology.[6] To account appropriately for the distributed nature of the interconnect RC network, the lumped ground capacitances $C_a$ and $C_v$ are scaled by a factor of 0.5 based on the Elmore delay model.[7] The lumped coupling capacitance $C_c$, on the other hand, is scaled by a semi-empirical, technology independent factor, $\alpha = (1-\beta)[\exp(-T_r/\tau_0)] + \beta$. The parameter β accounts for the presence of the victim driver resistance, and is given by $\beta = 0.5[1 + R_{vd}/(R_{vi} + R_{vd})]$. β is unity for a device-dominated case in which shielding resulting from interconnect resistance is negligible, and it decreases monotonically to 0.5 as interconnect becomes more dominant. The scaling factor α is equal to β for a slow rise time, but monotonically approaches unity for a sufficiently fast rise time. In **Figure 3** line length is varied to cover both the device-dominated case (interconnect length ≤ 1000 μm) and the interconnect-dominated case (interconnect length ≥ 3000 μm). The model prediction matches the SPICE results very well. The agreement is also excellent in **Figure 4**, where the rise time varies over a wide range.

Since all parameter values in equations 1 through 7 are readily available from the timing analysis tools, this model forms an excellent basis for a cross talk screening tool at the timing level. The nonproblematic signal lines can be quickly identified and filtered with this model. Only those lines that potentially violate noise margin need further detailed simulations. The efficiency of signal integrity verification can be significantly improved by this scheme.

Figure 4

*Normalized cross talk noise voltage as a function of rise time. The model prediction is represented by a solid line and the SPICE simulations are represented by circles. The error of the model compared with SPICE is less than 10%. Cross talk noise is a strong function of rise time and is a serious concern when rise time becomes less than 200 ps in deep-submicrometer technologies.*



### Model for Transistor-Level Analysis

Next, we consider a case in which the rise time to the *input* of the aggressor transistor is known. In this case the rise time at the *output* of the aggressor transistor is first computed as a function of the input rise time using a technology dependent function. Then equation 6 is used to calculate the maximum cross talk noise.

The rise time at the output of the aggressor transistor, $T_r$, is expressed as:

$$T_r = T_{ri} + T_{rw} + T_{rc}, \quad (8)$$

where $T_{ri}$, $T_{rw}$, and $T_{rc}$ account for the intrinsic delay, input slope, and interconnect loading dependencies, respectively.

**Intrinsic Delay Dependency.** The intrinsic delay dependency of the aggressor output rise time, $T_{ri}$, is empirically expressed as:

$$T_{ri} = k_i \frac{V_{dd}}{I_{d,sat}} C_j, \quad (9)$$

where $V_{dd}$ is the supply voltage, $I_{d,sat}$ is the saturation source-to-drain current, and $C_j$ is the junction capacitance. The $T_{ri}$ term is usually small ($\sim$5 ps) and is independent of the aggressor input rise time. It is also independent of device size; both $I_{d,sat}$ and $C_j$ increase as the driver size increases, canceling each other. The term $k_i$ is a fitting parameter. Our study shows that $k_i = 0.4$ for many different technology generations. The $T_{ri}$ term is important only for the following cases:

- Older technology generations for which the RC of a device is significant
- A transistor with extremely small loads
- Very fast input rise time ($<$35 ps).

None of these cases is of practical interest in deep-submicrometer technologies.

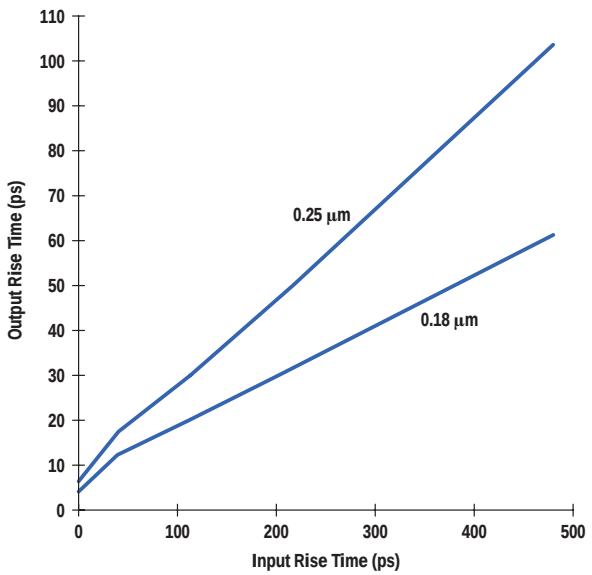
**Input Slope Dependency.** The input slope dependency of the aggressor output rise time, $T_{rw}$, is a linear function of the aggressor input rise time, $T_{ra}$:

$$T_{rw} = k_w T_{ra}, \quad (10)$$

where $k_w$ is a technology dependent fitting parameter and is typically between 0.1 and 0.2 for deep-submicrometer technologies. This linear relationship holds extremely well for the practical values of $T_{ra}$ ranging from 50 ps to 500 ps, as shown in **Figure 5**.

Figure 5

*Unloaded output rise time as a function of input rise time of the aggressor driver for 0.25-μm and 0.18-μm technologies. A linear relationship holds well for input rise time above 50 ps.*




This input slope dependency term can be very significant, especially for slower input signals and small load capacitances. For instance, for a 1-mm line with $T_{ra} = 160$ ps, $T_{rw}$ can be as high as 30% of $T_r$.

**Interconnect Loading Dependency.** The third term in equation 8 results from the charging and discharging of the interconnect through the aggressor driver. Since the driver goes through both the saturation and linear modes of operation during the charging and discharging, $T_{rc}$ has two corresponding terms:[8]

$$T_{rc} = \gamma \xi C_i \left[ \frac{V_t - 0.1V_{dd}}{I_{d,sat}} \right] + \gamma \xi C_i \left[ \frac{1}{k(V_{dd} - V_t)} \ln\left( \frac{19V_{dd} - 20V_t}{V_{dd}} \right) \right], \quad (11)$$

where $C_i$ is the interconnect capacitance, $V_t$ is the threshold voltage of the driver, and k is the device transconductance, which is given by:

$$k = \frac{2I_{d,sat}}{(V_{dd} - V_t)^2}. \quad (12)$$

The term $\gamma$ is an empirical expression to account for capacitance shielding caused by interconnect resistance, and is given by:

$$\gamma = 1 - \left[\frac{R_{ai}}{R_{ai} + R_{ad}\sqrt{3}}\right]^4, \quad (13)$$

where $R_{ai}$ and $R_{ad}$ are the aggressor line resistance and driver resistance, respectively. The term $\xi$ is an empirical constant accounting for the loss due to short-circuit current and is typically equal to 1.2. Short-circuit current does not serve to charge or discharge the line.

The first term in equation 11 describes the transient in the saturation region, but is typically much smaller than the second term because of the large current drive and the small voltage swing in the saturation region. The second term is for the transient in the linear region, and is technology dependent only on the ratio of $V_t/V_{dd}$.

Figure 6

*Comparison of rise time estimates. The model in this paper is in excellent agreement with SPICE results. A model in reference 9, which neglects $T_{ri}$ and $T_{rw}$ in equation 8 as well as interconnect capacitance shielding and short-circuit current in equation 11, exhibits large error over a wide range of interconnect lengths.*

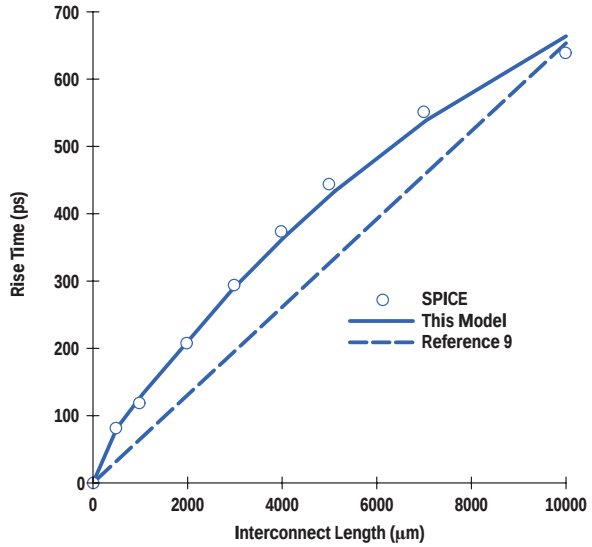
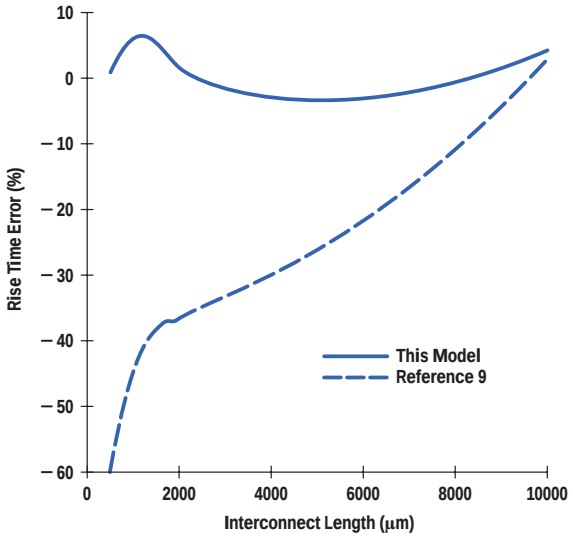



Figure 7

*Rise time estimation error of models compared with SPICE. Error for the model in this paper is ±10%. A model based on reference 9 produces a significant error.*




Benchmark of Model. Rise time values at the output of the aggressor driver calculated based on equations 8 through 13 for a wide range of interconnect lengths are compared with SPICE simulations in **Figure 6**. The model predictions are in good agreement with SPICE simulations. The modeling error compared with SPICE is shown to be less than 10% in **Figure 7**.

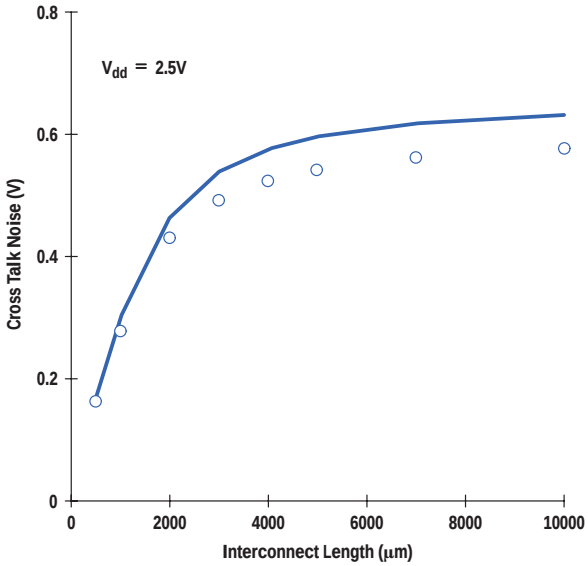
As a comparison, the rise time estimation based on a previously published model[9] is also shown in **Figure 6**. This model neglects $T_{ri}$ and $T_{rw}$. Also, interconnect capacitance shielding and short-circuit current in $T_{rc}$ are not considered. As a result, this model significantly underestimates $T_r$ for short lines and overestimates $T_r$ for long lines.

Once the rise time at the output of the aggressor driver is calculated, the corresponding peak cross talk noise can be computed based on equation 6. In **Figure 8**, modeled and SPICE peak cross talk noise values are plotted as a function of interconnect length. Our model provides a very smooth curve and matches the SPICE result within 10% over a wide range of interconnect lengths.

The technology dependent fitting coefficients in equations 9 through 11 can be found easily by running SPICE for

Figure 8

*Estimated cross talk noise voltage as a function of interconnect length. The model prediction is represented by a solid line and the SPICE simulations are represented by circles. The model is accurate (less than 10% error) over a wide range of interconnect lengths.*




several calibration cases. With the calibrated coefficients, this model rapidly generates accurate cross talk noise estimation for various driver sizes, interconnect loads, and rise times. The model is an attractive alternative to SPICE when many transistor-level simulations for cross talk noise are needed, including the case of quick screening mentioned earlier.

## Conclusion

In this paper we have analyzed the accuracy and applicability of a simple closed-form model for calculating cross talk noise on signal lines in deep-submicrometer interconnect systems. With appropriate scaling and calibration of the model coefficients, it was shown that the model is sufficiently accurate for cross talk analysis. All model parameters and coefficients are readily available. Therefore, the model is suitable for rapid cross talk estimation and signal integrity verification.

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