Data Transmission Schemes for Higher-Speed IEEE 802 LANs Using Twisted-Pair Copper Cabling

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Transmission at 424.8 Mbits/s using Category 5 cable can meet both industrial and the more stringent domestic emissions regulations. The design is robust in operation and the complexity is not much greater than that used for the 100-Mbit/s rate.

In October 1995, two new 100-Mbit/s local area network standards were published by the Institute of Electrical and Electronics Engineers: IEEE 802.12, based on a demand priority (DP) access method, and IEEE 802.3u, based on a collision sense multiple access/collision detection (CSMA/CD) access method. Subsequently, there has been much interest in increasing the operating speed of these standards beyond 100 Mbits/s.[1] This imposes design challenges for the two media involved: optical fiber and copper cabling. Optical-fiber-based approaches are discussed elsewhere in this issue. Here we will examine schemes that are designed to use existing copper cable installations, specifically data-grade cable, Category 5. This cable is already installed in locations that have followed building wiring standards.

A critical objective for the copper solution was to cost less than the fiber solution and this meant low complexity was required. We show that transmission at 424.8 Mbits/s using Category 5 cable can meet both industrial and the more stringent domestic emissions regulations. Furthermore, the design is robust in operation and of a complexity not greatly in excess of that used for the 100-Mbit/s rate.[2] The data rate of 424.8 Mbits/s is equivalent to the Fibre Channel rate of 531 Mbits/s before 8B10B coding (mapping 8 bits to 10 bits) and was chosen in anticipation of other IEEE 802 physical layers (PHYs) also following the route of compatibility with Fibre Channel speeds to leverage existing components.

Compared with fiber, a copper system has a number of problems peculiar to it. A long metallic conductor is prone to act as a radio antenna, and this could lead to interference with other equipment (emissions) and unwanted pickup from other equipment (susceptibility). In addition, the copper cables are isolated by transformer coupling to avoid ground loops and other undesirable dc effects. These properties together with the transfer characteristic of the cable determine what can be successfully transmitted over the cable in a real-world environment.

Architectural Requirements: Speed, Bidirectionality

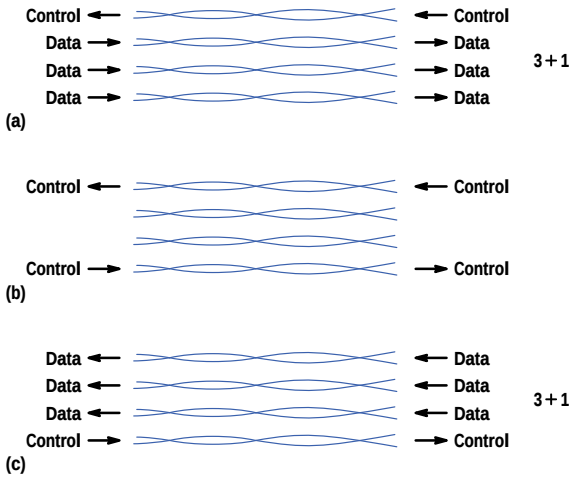
In a shared-medium access method such as DP or CSMA/CD, full-duplex data transmission is not possible, since only one station (or none) has access to the shared channel at any point in time. However, half-duplex data transmission is suitable and an important refinement is possible. Network control traffic, including, for example, requests for access to the shared media, can be allowed to travel upstream when data flow is downstream, or vice versa. This helps the efficiency of the network, making it into a hybrid duplex scheme in which data and control can flow simultaneously in opposite directions, but neither is full-duplex.[3]

Having four pairs in one Category 5 cable means that there are alternative duplexing schemes to the traditional single-channel frequency-division multiplexing (FDM) or hybrid-plus-echo-canceller approach. The bandwidth of one pair can be dedicated to a reverse control-signaling channel with the remaining three pairs for the forward data channel. This 3+1 scheme creates an asymmetric duplex scheme in terms of the bandwidth available in each direction. Having the still relatively high bandwidth of a single pair for control signaling is useful not because control traffic is high-bandwidth but because prompt detection of control codes is advantageous in terms of network performance. Asymmetric duplexing using selected pairs is notably less complex than FDM or hybrid plus echo canceller because of the lower component count. As shown in **Figure 1**, only two of the four pairs need be half-duplex; the other two can be simplex. Near-end crosstalk (NEXT) is no longer the dominant noise source in this Category 5 system as it was in the Category 3 100-Mbit/s systems.[5] Externally induced noise is dominant. Having a solution without FDM, echo cancellation, or NEXT cancellation is the pivotal step in forming a low-complexity system design.

Speeds greater than 100 Mbits/s are of interest for extending the existing standards, and in particular, speeds matching the Fibre Channel rates offer the possibility of leveraging existing components including drivers and clock recovery

Figure 1

The 3+1 hybrid duplex scheme.[4] (a) Data transmission to the right. (b) No data transmission. (c) Data transmission to the left.



circuits. The first two Fibre Channel rates offering a marked speed increase over 100 Mbits/s are 531 Mbits/s and 1062.5 Mbits/s. However, these include the overhead of an 8B10B code designed assuming a single serial transmission medium. Since the copper solution divides the data among three pairs, the 8B10B code could be replaced with something more appropriate for this application. The raw data rates for the two Fibre Channel rates then become 424.8 Mbits/s and 849.6 Mbits/s. Extending these rates to the 3+1 asymmetric duplex scheme gives per-pair rates of 141.6 Mbits/s and 283.3 Mbits/s.

Signaling: Multilevel Signaling, Coding, Control

Earlier work[6] had shown that transmitting basic NRZ data at 155 Mbits/s was unlikely to satisfy domestic emissions regulations (e.g., FCC B) and might even prove problematical in meeting the less stringent industrial regulations (e.g., FCC A). Regulations begin at 30 MHz, so reducing transmitter spectral energy above this frequency is an obvious approach to reducing emissions. Thus, a per-pair rate of 283.3 Mbits/s immediately seems far less suitable for a copper implementation than 141.6 Mbits/s. Several bandwidth compressing modulation schemes were studied, including quadrature amplitude modulation (QAM), partial response (PR) classes I and IV, and pulse amplitude modulation (PAM).[7,8] QAM is a two-dimensional scheme requiring complex in-phase and quadrature filters, and while PR has good bandwidth compression, this comes at the expense of clock recovery. PAM requires dc balancing but is a relatively straightforward scheme to implement and when m levels are used reduces bandwidth requirements by $\log_2(m)$. If excess bandwidth α is also reduced below 100% then an extra factor $(1+\alpha)/2$ is gained to give the overall relationship:

$$\text{Transmitter bandwidth} = \frac{\text{bit rate}}{\log_2(m)}(0.5 + \alpha/2).$$

Using the measured external noise level (discussed later), noise margin was calculated for PAM systems from 2 to 16 levels with 80% excess bandwidth, 100-m Category 5 worst-case attenuation, and a per-pair bit rate of 141.6 Mbits/s. **Figure 2** shows the noise margin plotted against baud rate, or equivalently, PAM index at the given data rate. For these calculations, equal peak transmitter voltage was assumed regardless of number of levels. Also shown are the maximum receiver gain and the symbol separation that were used to calculate the margin. A comparison of the transmitter spectra for 2-level, 4-level, and 8-level PAM are shown in **Figure 3**, where a fair comparison has been introduced by adjusting the

Figure 2

PAM noise margin as a function of PAM index (m) for a data rate of 141.6 Mbits/s.[8]

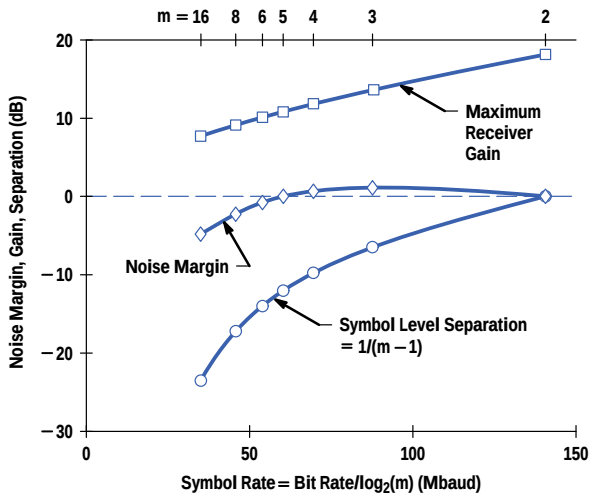
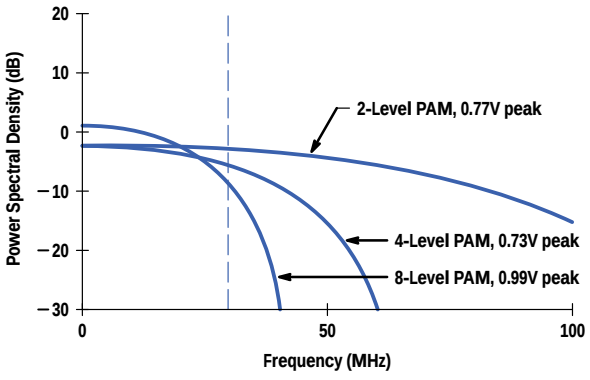


Figure 3

2-level, 4-level, and 8-level PAM transmitter spectra for equal noise margin.[8] *Only the first lobes of the spectra are shown.*



transmitter output voltage to yield the same noise margin at the receiver in each case. The start of emissions regulations is marked by the dotted line at 30 MHz. Clearly, 8-level PAM has lower energy above this frequency. To determine if the transmitters will actually pass the regulations, EMC measurements are required, which must also include the cable.

The absence of a dc response is a problem for a baseband system such as PAM, but can be solved by the addition of a balancing block code having the property of reducing the running digital sum (RDS, the sum of transmitted symbol levels), which reduces low-frequency components. A block code that has more codewords than data words— that is, redundancy—allows control signaling to be readily incorporated into the transmitted symbol stream. Block coding can also ensure a high transition density, which aids clock recovery schemes.

Table I shows five possible block codes.[4] The best all-around codes are 8B3N (mapping 8 bits to 3 nonary or 9-level symbols) and 16B6O (mapping 16 bits to 6 octary or 8-level symbols) since, in addition to good bandwidth compression and redundancy, the inputs are multiples of eight bits, which can lead to implementation convenience. Additionally, in the 8B3N case, the RDS at a codeword boundary is constrained to be between −4 and 5. Choosing a subset of the 8B3N code for data allows inband control signaling, and if the subset is suitably constrained, the spectral magnitude of the control codes does not greatly exceed that of the data (see **Figure 4**). Finally, by ensuring that the control codewords have a Hamming distance of two with respect to data codewords, then single error events will always be detected in the control codewords. When 8B3N is encoded, the per-pair rate of 141.6 Mbits/s equates to a symbol rate of 53.1 Mbaud.

Table I
Properties of Possible Block Code Options[4]

Code	Output Levels	Bandwidth Compression Factor	Redundancy Factor	Baud Rate (Mbaud) for Bit Rate of 141.6 Mbits/s	Comments
3B1O	8	3	1	47.2	Cannot balance
8B3O	8	2.67	2	53.1	Byte aligned
10B4O	8	2.5	4	56.6	
8B3N	8	2.67	2.85	53.1	Byte aligned
16B6O	8	2.67	4	53.1	Word aligned

* Redundancy factor = number of output permutations divided by number of input permutations.

Electromagnetic Compatibility (EMC)

Electromagnetic compatibility was one of the first areas to be investigated and measurements were performed before the 8B3N code had been chosen for the system. To evaluate the general effectiveness of PAM bandwidth compression with respect to emissions, uncoded 8-level PAM was used for the measurements at 50 Mbaud.[10,11]

European (EN) and U.S. (FCC) emissions regulations limit the radiation level that the system can be allowed to generate (see **Figure 5**). The industrial Class A levels are 10 dB less stringent than the domestic Class B levels shown. 100VG-AnyLAN[5] used all four pairs of the cable to good effect by sending only 30 Mbaud on each pair, hence staying below the emissions limits. However, at higher rates this is not enough; even using all four pairs for data, the per-pair rate is 125 Mbits/s for 500 Mbits/s total, and using the 3+1 scheme, 141.6 Mbits/s is required. This would require a bandwidth in excess of 30 MHz using 100VG-AnyLAN signaling. Bearing in mind that some balancing overhead would be required, 155 Mbits/s NRZ and 50 Mbaud 8-level PAM were convenient rates to be investigated in terms of emissions.

EMC measurements were made to ascertain the levels of radiation and susceptibility of the Category 5 cable so that the results could be used to examine the trade-off between bandwidth improvement and increased noise susceptibility when moving to a multilevel system. A 100-m length of Category 5 cable including short patch cords and a punchdown block (connector block) was tested with 150-Mbit/s and 50-Mbit/s binary data and a prototype 50-Mbaud, 8-level PAM source.

Figure 4

Spectra of 8B3N data and control signaling.[9]

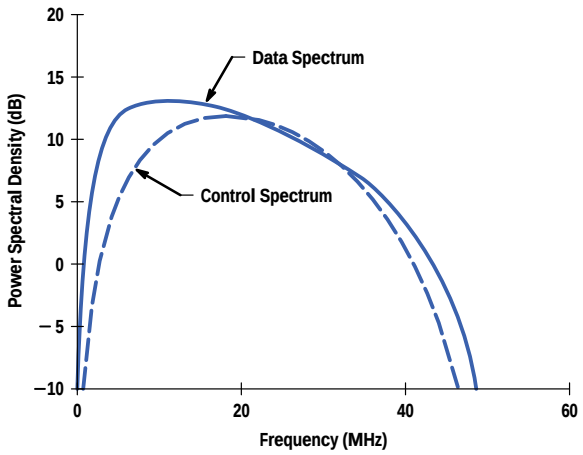
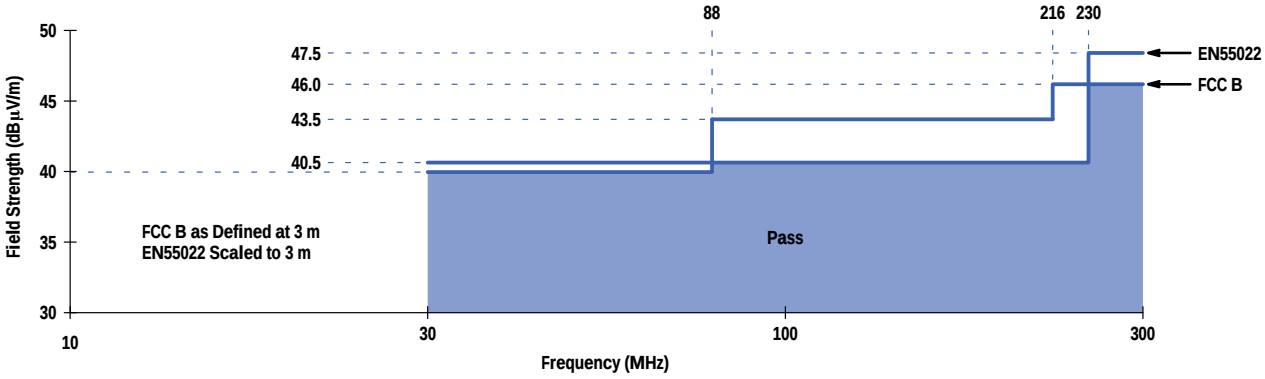


Figure 5

FCC and EN emissions regulations.[6]



Transmitter output level was 1V peak-to-peak into 50 ohms and 1.4V peak-to-peak when matched to the 100-ohm Category 5 transmission line using a balun. In each case the free cable was wound noninductively on a 1-m-by-1-m wooden frame. Emissions were measured at 3 meters with each transmitter and susceptibility was measured when the cable was subjected to a standard 3V/m field. The field strength was leveled at each of 11 spot frequencies using a pair of optically coupled field probes before each measurement. The results are shown in **Figure 6**.

Note that externally induced noise is the major noise source in the Category 5 half-duplex system under consideration, principally due to the low level of cross talk. **Figure 7** shows that the 155-Mbit/s case breaks the FCC B emissions mask (barely), whereas **Figure 8a** shows that the 50-Mbit/s case does not. The emissions mask has been adjusted to account for the EMC measurement site attenuation and is thus no longer flat with frequency.

The prototype 50-Mbaud trace (**Figure 8b**) shows some clock breakthrough, but otherwise meets the mask. The breakthrough is a result of prototype construction rather than a feature of the code. Development of the prototype would

Figure 6

Measured induced noise levels in a 3V/m field.[12]

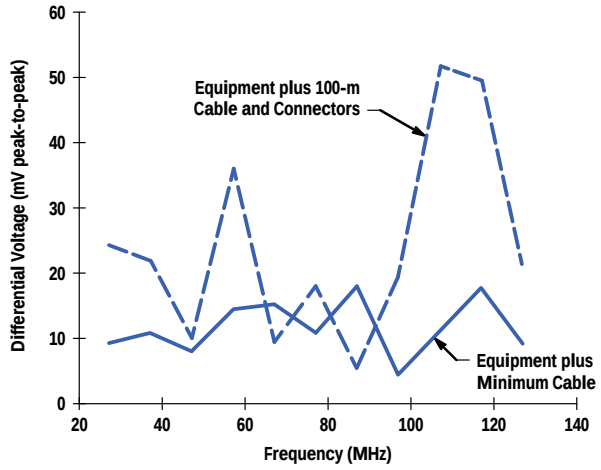
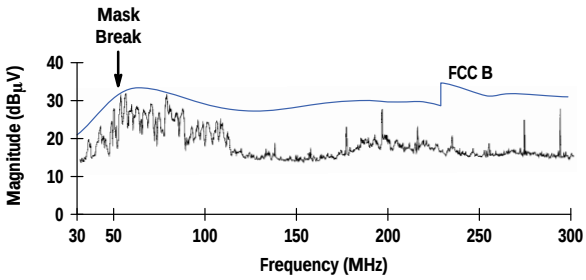


Figure 7

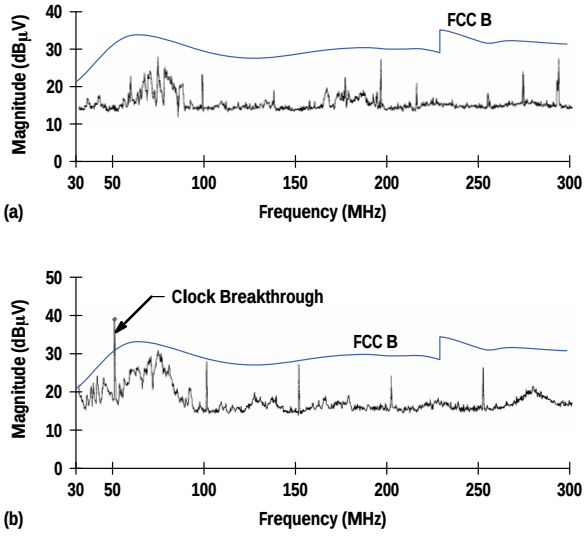
Measured 155-Mbit/s emissions with FCC B limit overlay.[8]



enable the spectrum to approach the 50-Mbit/s trace from the test instrument (**Figure 8a**), which is shown for comparison purposes. The 155-Mbit/s EMC data was within 1 dB of emissions measurements made a few years earlier for presentation to the ATM Forum.[6]

Figure 8

Measured emissions with FCC B limit overlay.[8] *(a) 50-Mbit/s NRZ. (b) 50-Mbaud 8-level PAM.*

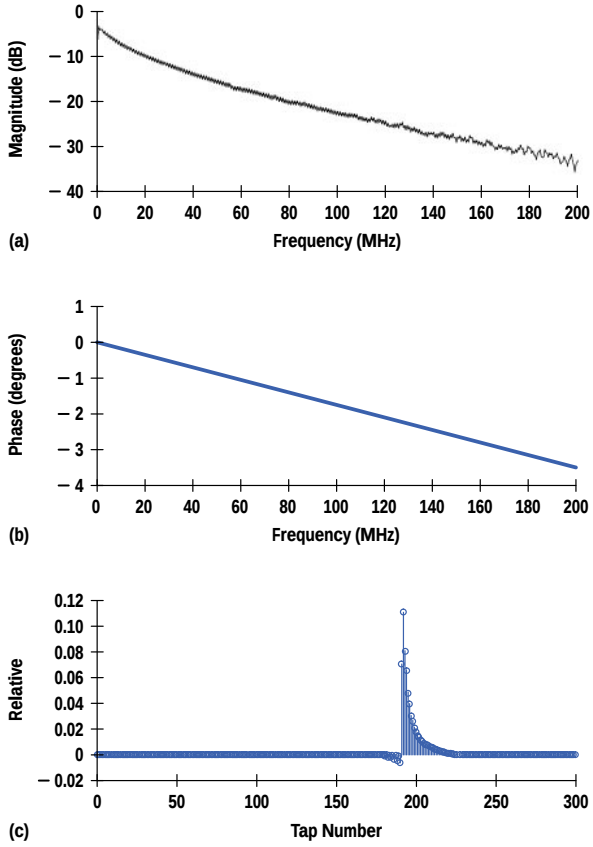


The Channel: Cable and Transformers

The measured frequency and phase responses of a sample 100-m Category 5 channel and transformers are shown in **Figures 9a and 9b**. Note the increasing attenuation with frequency, the absence of a dc response, and the nearly linear phase slope. The phase slope equates to a time delay of 0.486 μs which, as expected, is equal to the transit time of 100 meters of cable assuming a propagation velocity of 0.7c. Oversampled FIR (finite impulse response) models of the measured and EIA/TIA 568 worst-case channels were generated for simulation purposes, and the measured case is shown in **Figure 9c**. The rather long delay to the punctual tap of this impulse response is 192 taps × 1/400 MHz = 0.48 μs, equal to the cable delay as before. The decay after the punctual tap is the result of the low-pass nature of the cable and the very small final tail, which is offset below zero, is a result of the low-frequency corner introduced by the transformers.

Figure 9

Measured (a) frequency and (b) phase response of 100-m typical Category 5 cable to 200 MHz. (c) 305-tap FIR filter model.



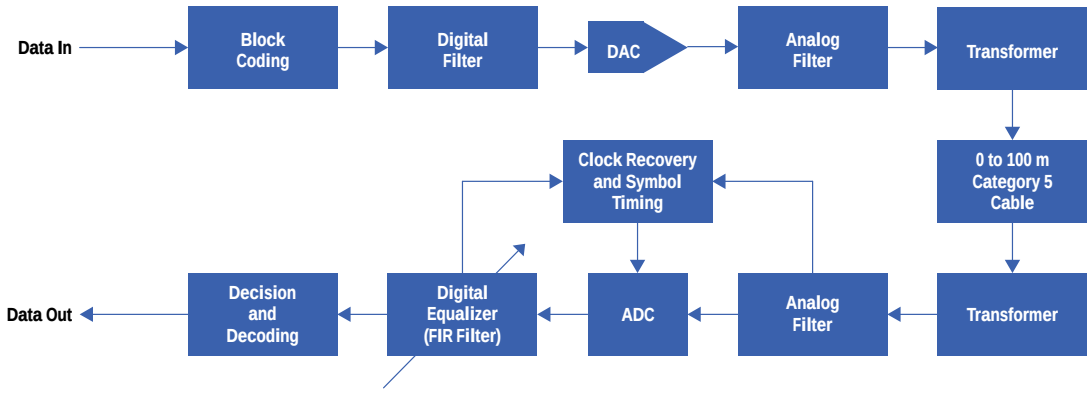
Simulation

Figure 10 shows the simulated data transmission path. The functional blocks were written using the MATLAB package. Transmitter block coding was 16B6O or 8B3N, finite precision was used for the signal conversion blocks, and the receiver was configured to use a reference clock. Both T-spaced (baud-spaced or synchronous) and T/2-spaced FIR filter

equalizers were used, using the gradient LMS (least mean squares) algorithm in reference-directed mode for convergence and including finite-precision effects.

Figure 10

Simulated transmission path.[13]



A T/2 fractionally spaced equalizer was preferred for its insensitivity to timing phase (due to the absence of aliased band-edge components). If a lower sampling rate had been preferred, a T-spaced equalizer could have been used at the expense of slightly more clock recovery complexity. The simulation was used to study the performance of the block codes for varying degrees of transformer low-frequency loss.

The 3 + 1 scheme was used with a bit rate of 141.6 Mbits/s on each pair, giving a bandwidth over the three data pairs of 424.8 Mbits/s, which corresponds to the 531-Mbit/s Fibre Channel rate without 8B10B encoding as described above. Mapping 16 bits to 6 octary (8-level) symbols or mapping 8 bits to 3 nonary (9-level) symbols results in the same bandwidth compression factor (2.65) and yields a symbol rate of T = 53.1 Mbaud in each case. Transmit filtering was root raised cosine with $\alpha = 0.8$, followed by a fifth-order analog Butterworth filter with a cutoff at 40 MHz.The channel was simulated by the cascade of transformers modeled as first-order high-pass filters with a cutoff at 100 kHz and cable modeled as an FIR filter with a transfer function approximating the worst-case propagation loss as set out in EIA/TIA 568.

At the receiver a fifth-order Butterworth filter at 40 MHz provided anti-aliasing and out-of-band noise rejection. The analog-to-digital converter (ADC) had variable resolution and the effect of an AGC circuit was modeled by ensuring that the applied signal occupied the full scale of the converter. The equalizer structure was T/2 and used the well-known gradient LMS adaptation algorithm. Internal accuracy was maintained at 12 bits although the coefficient resolution and the number of taps were variable.

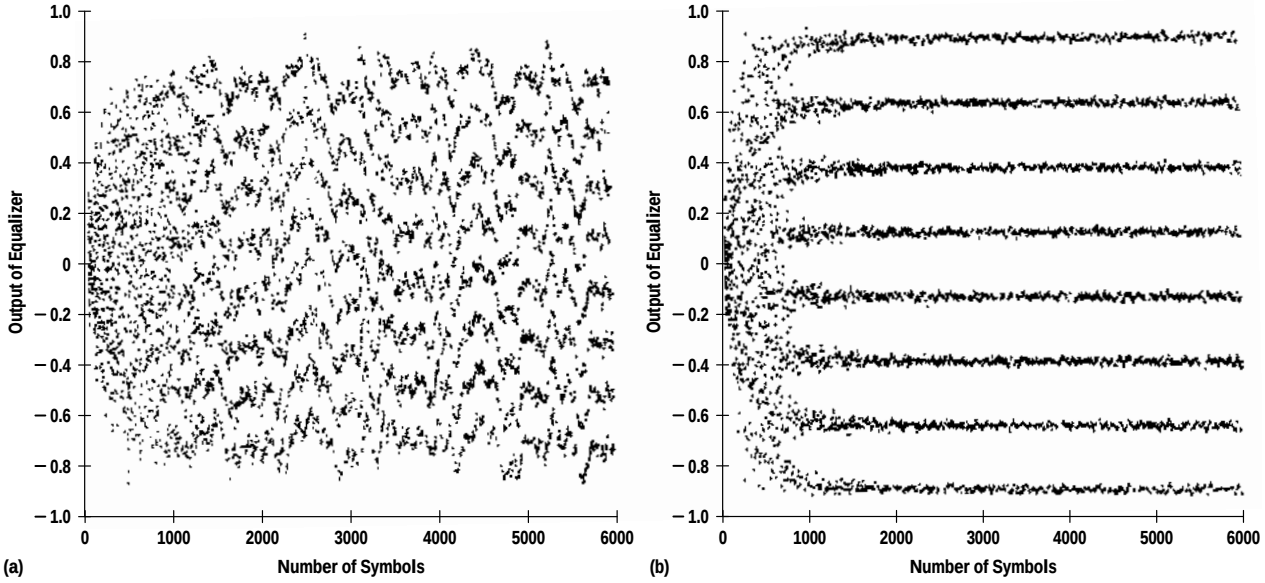
Figure 11 shows the effect of transformer coupling in terms of baseline wander. The system output level diagram is shown with and without a block code. Clearly the baseline wander in the first case is intolerably high.

To compare the results obtained with different numbers of taps and resolutions, the metric of SNR margin over $BER = 10^{-10}$ was used. A positive margin of x dB indicates that the system has exceeded the signal-to-noise ratio (SNR) required to obtain a bit error rate (BER) of 10^{-10} by x dB. Below the roll-off region the equalizer adapts to whiten the incoming signal spectrum, effectively inverting the cable response as seen in **Figure 12**.

Figure 13 clearly shows that positive margins begin to be achieved for systems using at least a 6-bit ADC and at least 7 T/2 taps. More important, practical margins are possible for quite low-complexity systems. As an example, a 7-bit ADC used with a 25-tap T/2 fractionally spaced equalizer offers a 7.3-dB margin beyond a BER of 10^{-10}. Preliminary designs

Figure 11

Output level diagram (a) without and (b) with 16B6O block code.[1]



targeting HP's CMOS14 process used an 8-bit ADC and a 27-tap filter for each channel to yield a total power consumption

Figure 12

Frequency responses of cable, digital transmit filter, analog transmit filter, and equalizer.

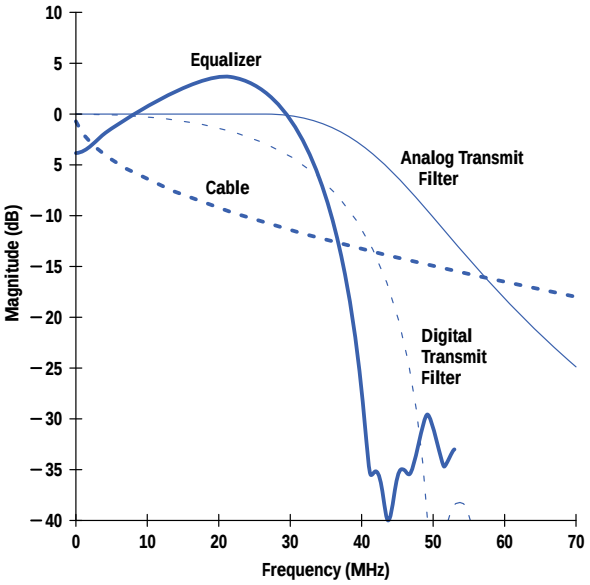
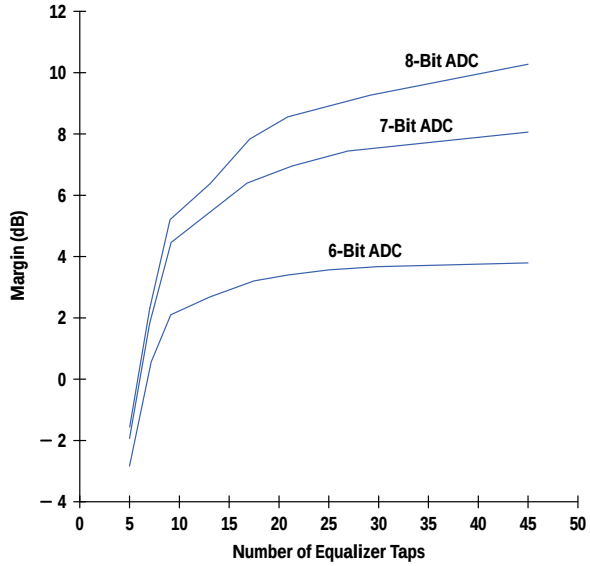


Figure 13

Margin as a function of T/2 equalizer length with 10-bit coefficients (12 internal) for 6-bit, 7-bit, and 8-bit ADCs.



of approximately 4 watts. Because the ADC and FIR elements are critical blocks in the design, reducing to a 7-bit data path as in the simulation above would help area and power performance markedly. For example, reducing the resolution of a flash ADC by one bit halves the area and power consumption.

Hardware Demonstration

A basic hardware proof-of-concept demonstrator was constructed using off-the-shelf components following the block diagram shown in **Figure 14**. A balanced 8-level transmitter using a basic 5B2O code was written in VHDL and synthesized into an Altera 7K CPLD (complex programmable logic device) and used to drive a digital-to-analog converter (DAC) clocked at the symbol rate of 50 Mbaud. After traversing the channel of 100 meters of Category 5 cable and transformers, the resulting signal was clocked into an analog-to-digital converter by a delayed version of the transmitter symbol clock. Seven-tap and 15-tap FIR (finite impulse response) filter equalizers were produced in the Altera Hardware Description Language by modifying parameterized macros to accommodate limited-precision effects and odd-order symmetric filters. To make the demonstrator much faster than serial FIR implementations, lookup tables containing precomputed partial products were used in a pipelined manner, assuming variable input data but fixed coefficients. The partial product method is also called distributed arithmetic (www.xilinx.com) and vector multiplication (www.altera.com). The FIR device was synthesized into an Altera 8K part having 12K usable gates.

Figure 14

Hardware demonstrator block diagram.

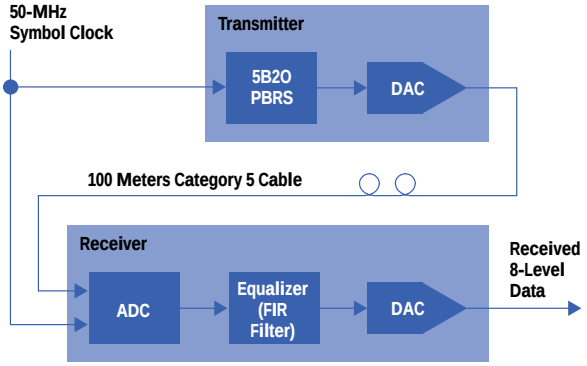
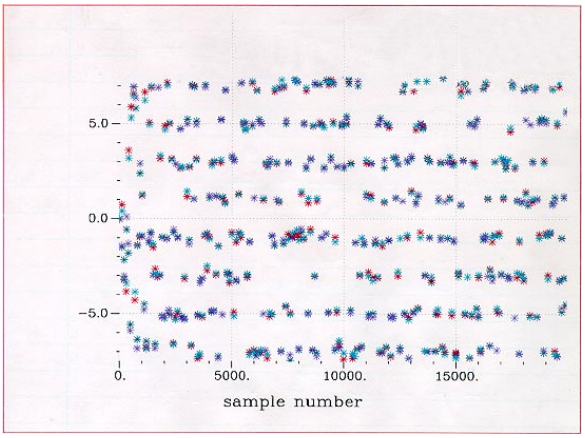


Figure 15

Eye diagram using the simulated equalizer. The vertical scale is voltage in arbitrary units. The graph shows rapid convergence of the output signal to the quantized levels of 8-level PAM.



The demonstrator had a T-spaced filter whose coefficients were calculated offline using the COSSAP analysis package with measured cable data. An eye diagram using the converged simulated equalizer described above is shown in **Figure 15** and the taps are shown in **Figure 16**. When running, the demonstrator had no feedback or trimming of coefficient values and relied wholly upon the accuracy of the simulation. This method was adequate for a demonstration, but clearly a feedback algorithm such as LMS would be employed in a practical implementation to cope with changes in cable frequency response, delay, temperature, and other parameters. The transmitter clock source was delayed and used to clock the receiver, phasing being critical because of the synchronous equalizer. Moving to fractional spacing would largely remove this dependence on clock phase.[14]

Figure 16

Taps for the filter used in the demonstrator. Heavy line: assymetric taps. Light line: forced symmetry in taps (used in demonstrator).

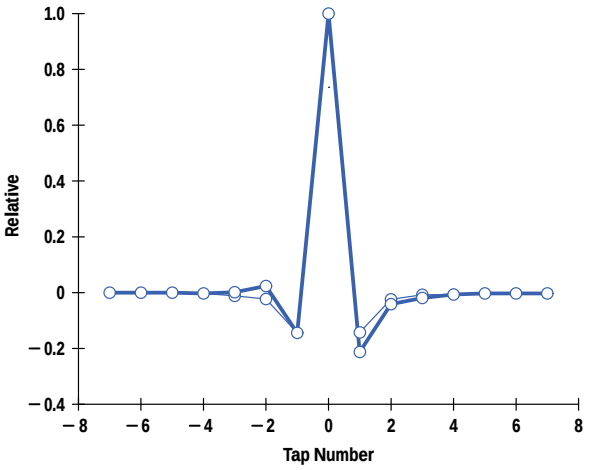
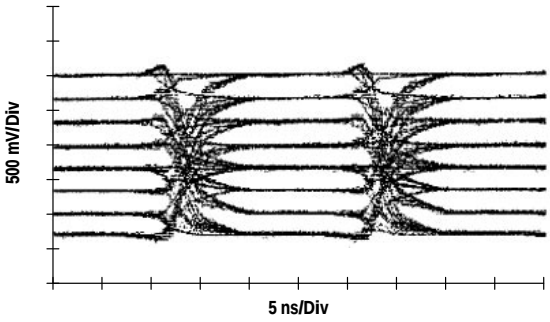


Figure 17

Eye diagrams of the received 8-level data.



While the open-loop nature of the system precluded long-term BER testing, the resulting eye diagrams (**Figure 17**) confirmed the operation of the hardware.

Conclusion

At a rate of 424.8 Mbits/s it has been shown that a low-complexity solution exists for a higher-speed shared-medium IEEE 802-style physical layer using Category 5 cable. Neither echo nor NEXT cancellers are required and the overall complexity is only slightly greater than current 100-Mbit/s systems. The system is designed to work on the installed base of Category 5 cable and is capable of meeting both industrial and domestic EMC regulations. The data rate facilitates interworking with other physical layers using Fibre Channel bit rates.

Acknowledgments

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