Flip-Chip Photodetector for High-Speed Communications Instrumentation

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A family of 7-GHz-bandwidth optical receivers and a nine-channel optical receiver with a gigabit-per-second data rate per channel have been developed for multigigabit lightwave test systems for long-haul fiber-optic telecommunications links and gigabit optical interconnects for computer systems. A new micro-flip-chip process, featuring liftoff-based small-diameter solder bumps, is incorporated with HP high-speed InP p-i-n photodetectors to minimize parasitic capacitance and inductance and enhance responsivity.

Ultrahigh-performance optical receivers to convert optical signals into electrical impulses require very careful packaging of photodetector and electronic amplifier ICs. Very high-performance photodetector and amplifier ICs can be individually fabricated, but when packaged by conventional methods that employ wire bonds, the system performance falls short of the desired goal. This is a result of parasitic capacitance and inductance introduced by large bonding pads and long bond wires. A 7-GHz-bandwidth optical receiver composed of a 26-GHz InP photodetector and a 12-GHz GaAs amplifier requires package-related parasitic capacitance and inductance of less than 50 fF and 10 pH, respectively. To minimize the parasitic components introduced by packaging, we have developed a hybrid flip-chip integration approach that bonds a photodetector directly onto a GaAs or Si receiver IC by means of very small-diameter solder bumps.

The packaging of high-speed optoelectronic components requires coupling of light into a small photosensitive area of the photodetectors, 10 to 15 μm in diameter. This is usually accomplished by precise alignment of the optical fiber or the transmitter (laser) to the photosensitive area of the detector. The flip-chip die attachment technique allows precise placement of the detector and the transmitter on the prealigned and prefabricated solder bump pads. To further ease the alignment tolerance and reduce the packaging cost, we have

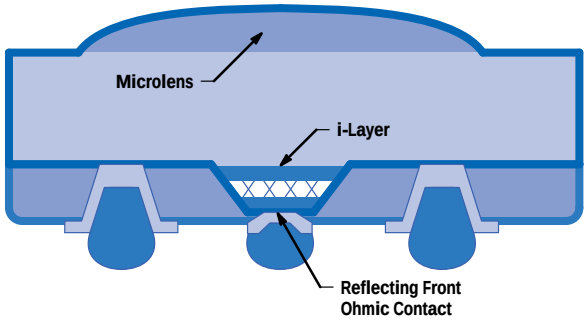
integrated a microlens with the detector to increase its effective light acceptance aperture. The combination of low parasitics and self-alignment of the flip-chip die attachment with an integrated microlens has allowed us to realize a family of 7-GHz optical receivers for lightwave test systems and a gigabit nine-channel optical receiver for optical interconnect applications.

Flip-Chip Photodetector with Microlens

Designing a photodetector that simultaneously satisfies the criteria of high bandwidth, high responsivity, small parasitic capacitance, and high optical coupling efficiency is a challenging task. A p-i-n photodetector with a thin i-layer has a very high bandwidth but fails to satisfy the responsivity and low parasitic capacitance requirements. It is possible to meet the bandwidth, low parasitic capacitance, and responsivity criteria by designing a detector with a small geometry and a moderate i-layer thickness. However, an expensive package that employs precision optics is required to meet the coupling efficiency requirement.

Figure 1

Flip-chip photodetector cross section.



By a combination of the flip-chip packaging concept and device geometry optimization we can meet the required system goal. The flip-chip die attachment technique provides the following advantages to the design and performance of a high-speed photodetector:

1. The p-i-n photodetector in a flip-chip configuration, as shown in **Figure 1**, allows the incident optical signal to traverse twice, or make a double pass through the light-absorbing i-layer. This is made possible by the close proximity of the reflecting front ohmic contact to the i-layer and by allowing most of the reflected signal to be converted again to the electrical signal. This gives the designer an extra degree of freedom to satisfy the conflicting requirements of high bandwidth and high responsivity.
2. In a flip-chip configuration, all the electrical contacts are made through the solder bumps, which are located on the front side of the detector. The backside of the detector, where the incident optical signal enters, is free of any metallized contacts. This allows an integral microlens[1] to be fabricated on the back surface of the photodetector. The microlens increases the effective acceptance aperture, thereby increasing the optical coupling efficiency while enabling the use of small-geometry devices. This significantly reduces parasitic capacitance.
3. A micro-flip-chip die attachment technology can be used. Very small-diameter solder bumps allow precision placement of a photodetector directly on top of a receiver IC while adding negligible parasitic capacitance and inductance.

Micro-Flip-Chip Technology

The conventional hybrid integration and packaging approach, which wire-bonds active components to a common substrate, requires bonding pads at least 0.003 inch by 0.003 inch in size. The parasitic capacitance of a bonding pad alone amounts to 80 fF, and the wire-bond inductance is typically a few hundred nH.

There are several integration approaches, both monolithic and hybrid, that can reduce the extent of parasitic component loading. Optoelectronic integration technologies that monolithically combine the photodetector and electronic transistors, although the most effective, are still in their infancy, and are not the most cost-effective methods today. Flip-chip bonding the photodiode and the receiver IC to a thin-film substrate using conventional solder bump technology eliminates the parasitic capacitance and inductance of the wire bonds but still suffers from interconnect trace loading between the photodetector and the amplifier. The total capacitance due to the interconnect and the bump pads amounts to 100 to 200 fF. Flip-chip bonding a photodiode directly onto a receiver IC eliminates nearly all unwanted parasitics. However, the size of the solder bumps must be kept small to meet the 50-fF goal. Simulations indicate that solder bumps less than 40 μm in diameter are necessary to meet the performance goal.

Based on our system performance goals, we have chosen to develop a micro-flip-chip technology that features solder bumps 30 μm in diameter. During the course of our effort, we have addressed the following technical challenges:

- A process for depositing and defining 30-μm-diameter solder bumps
- A solder bump process that does not induce significant stress or contaminants on the photodetector to cause degradation of its performance
- An underfill process that makes the micro-flip-chip die attachment mechanically rugged
- Precision placement of very small die (350 μm by 350 μm) onto a 1-mm-by-1-mm integrated circuit.

Fabrication Process

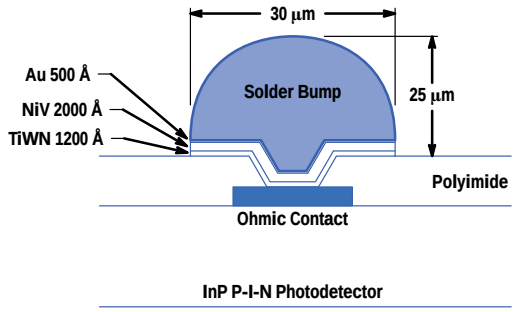
The fabrication of a flip-chip photodetector with an integrated microlens involves the following process steps. Undoped InGaAs optical absorption layers and p^+ doped InP epitaxial layers are grown on the S-doped n^+ InP substrate using an organometallic vapor phase epitaxial (OMVPE) system. The active region of the detector is defined by mesa etching. The p-ohmic and n-ohmic contacts, which consist of Ti/Pt/Au layers, are fabricated on the front side of the diode. The device is then passivated with polyimide. A microlens is defined on the polished backside by reflowing a circular photoresist pattern at 250°C to form a hemispherical surface, which is subsequently transferred into the InP substrate by means of ion milling. The result is a smooth lens surface with an acceptance aperture of 90 μm and a radius of curvature of 115 μm. A Si_3N_4 film, which serves as an antireflective coating for the lens, is deposited using PECVD (plasma enhanced chemical vapor deposition). Reactive ion etching opens up the vias in the polyimide to provide electrical contact to the ohmic metal underneath. The base metal stack is deposited by magnetron sputtering following a sputter etch cleaning step. The base metal stack consists of 1200Å of TiWN, 2000Å of NiV, and 500Å of Au.[2] **Figure 2** shows the cross section of the base metal after deposition and patterning.

The TiWN layer promotes adhesion and acts as a metallurgical barrier to solder. Since the interconnect metal on the InP photodetectors is gold-based, it is imperative to have a metallurgical barrier. Otherwise, upon reflow, the solder will consume the interconnect metal on the photodiode. Cr is another possible choice as the base metal; however, early experiments indicated that Cr etchant attacks InP substrates. NiV provides good solderability, while Au preserves the solderability of Ni when exposed to air. After deposition, the base metal pattern of 30 dots is defined on top of the vias with photoresist patterning and wet etching.

To create 30-μm-diameter, 25-μm-high hemispherical bumps after reflow, we have chosen to define solder pancakes. The tight alignment tolerance and small aperture required make the conventional shadow mask-based evaporation unsuitable. This necessitated the development of a liftoff-based solder deposition and definition process. In the micro-flip-chip

Figure 2

Micro-solder bump cross section.



process, 40-µm-diameter holes are photolithographically defined in a 14-µm-thick layer of positive photoresist. The exposure and the development time of the resist are controlled so that the sidewalls of the 40-µm-diameter openings are vertical, which is paramount to a successful liftoff. The solder layer is 60%wtPb/40%wtSn and is deposited by evaporation. This composition of solder was chosen to ensure that the reflow temperature is sufficiently low that it will not induce any thermal stress on the p-i-n photodetector. The diameter of the bumps is set at 40 µm and their height at 14 µm after the liftoff, which gives the optimum aspect ratio of the bumps after the solder is reflowed. **Figure 3** shows an SEM micrograph of the solder pancakes after liftoff.

Before solder reflow, the bumps are coated with no-clean water-based flux. Once fluxed, the bumps are reflowed at 240°C for 45 seconds. The diameter of the reflowed bumps is 30 µm. In contrast to the conventional shadow mask technique, our liftoff process allows uniform and precise definition of solder bumps with diameters less than 50 µm. It also eliminates the halo ring normally observed with shadow masks. **Figure 4** is an SEM micrograph of reflowed solder bumps.

Flip-Chip Assembly

To reduce parasitic capacitance, the dimensions of both the die and the detector active area must be minimized. A typical high-speed InP photodetector has a 10-µm diameter and its die dimensions are 350 by 350 µm. This detector is die-attached to a transimpedance amplifier to realize an optical receiver as shown in ***Figure 5***.

The major elements of the die-attach process consist of fluxing the solder bumps, aligning, and reflowing the solder. A precisely controlled amount of flux is applied to the solder bumps of the detector using a microsyringe. It is important to limit the volume of the flux to approximately 1 nl to facilitate the alignment and to minimize the amount of solid residue left on the surface of the detector and the circuit. To increase the mechanical robustness of the attachment, an epoxy underfill composed of 65%wt silica is used to fill the gap between the die and the substrate. The solder bumps on the detector are aligned to the bump pads of the amplifier. Because of the small dimensions of both the chips and the solder bumps, a high-precision flip-chip aligner is used for the alignment. The aligner allows simultaneous viewing of both its lower and upper chucks by means of split optics. Before alignment, the amplifier is loaded on the lower chuck and the detector on the upper chuck. The lower chuck is moved until the image of the bumps and the image of the amplifier contacts are superimposed. A sharp image of both chips, necessary for precise alignment, can be obtained only when the layer of flux coating the solder bumps is very thin. After the alignment both chips are brought into proximity and tacked with a precisely controlled force. Because of the small number and size of the bumps the tacking force should not exceed 10 grams; otherwise, the bumps become deformed and the surface tension is not strong enough to lift the chip during the reflow.

Figure 3

SEM micrograph of solder pancakes after liftoff.

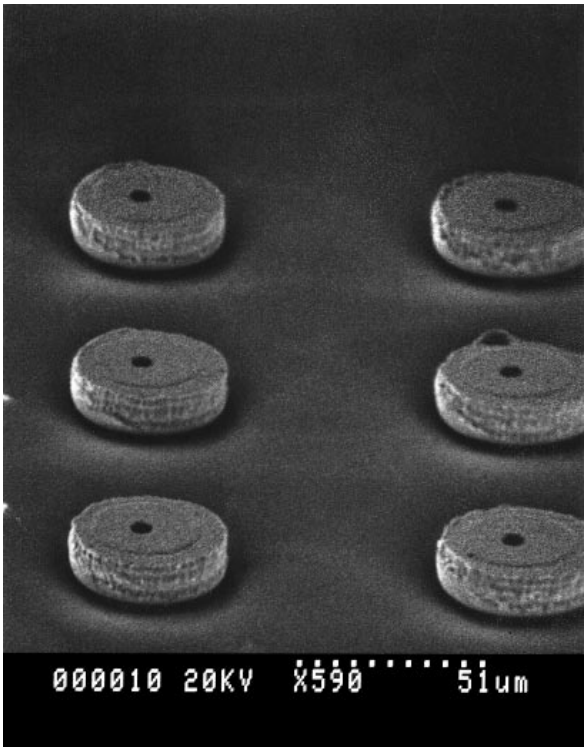


Figure 4

SEM micrograph of microbumps after reflow.

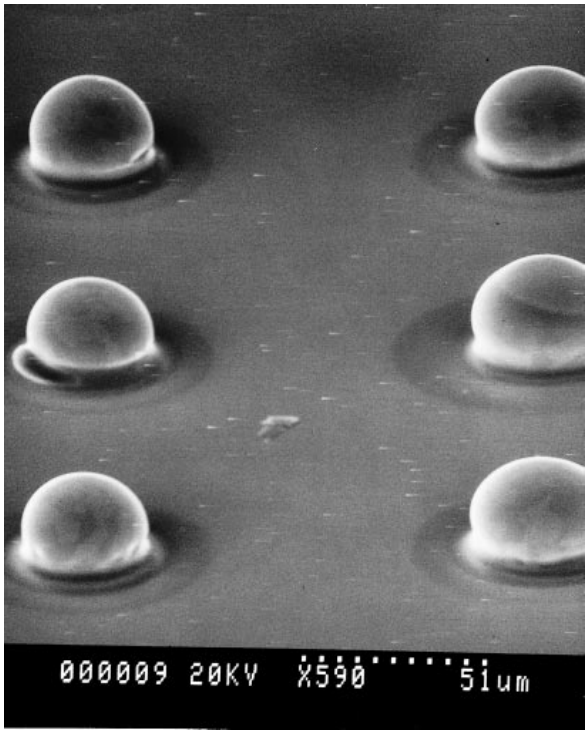
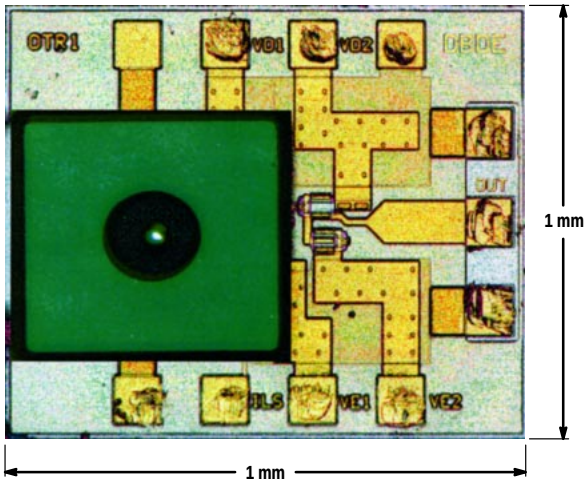


Figure 5

Optical receiver consisting of a flip-chip photodetector attached to a transimpedance amplifier.



The solder bump interconnection is completed by solder reflow at 240°C in a nitrogen atmosphere using a clamshell type oven. The oven provides very stable and repeatable annealing conditions from run to run. The reflow time is 45 seconds, which includes 15 seconds of ramp time and 30 seconds of dwell time.

Mechanical Characterization

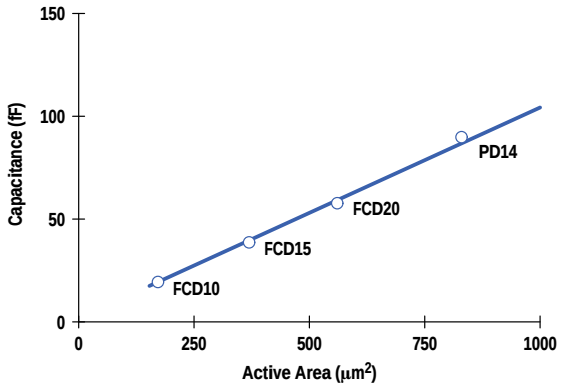
The mechanical strength of the microbumps without the underfill has been tested in shake and shear force tests. Several optical receivers were mounted on a chuck, and shear force applied to the detector was steadily increased until the bumps failed. An average shear force that caused complete die separation was 6 grams, or 2 grams per bump, which corresponds to an equivalent of 25,000g acceleration. The bumps sheared in the middle, which is the optimum situation. The measured shear force agrees well with the predicted value. The shake test subjected our optical receivers to accelerations of 1000g in three axes for a total of 18 hits. All samples have passed this test. When the gap between the die and the substrate is filled with the epoxy underfill material, the attachment becomes so strong that it is impossible to separate the die from the substrate without destroying one or both of them.

Electrical Characterization

One of the key features of our flip-chip detector is its low total capacitance. **Figure 6** shows the measured capacitance for standard and flip-chip photodetectors. FCDxx and PDxx designate the flip-chip and standard devices and xx denotes the diameter of the photosensitive area of the photodiode. FCD15 and PD14 have nearly identical photosensitive areas, while the total active area of the former is one-third that of the latter. As a result, the total capacitance of FDC15 is one-half that of PD14. This is made possible by the micro-solder-bump technology, which allows a reduction in the size of the p-ohmic contact.

Figure 6

Capacitance of p-i-n photodetectors.

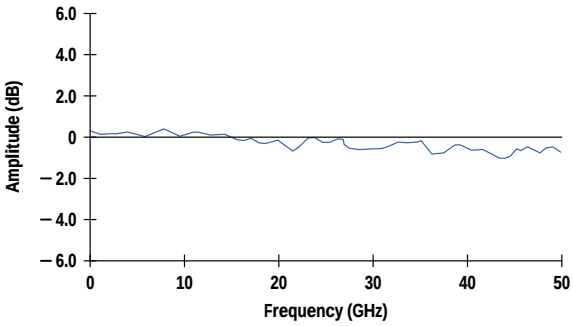


Dc and frequency-domain measurements are made by solder bumping individual photodiodes onto specially designed GaAs-based chip carriers whose interconnect patterns maintain a characteristic impedance of 50 ohms. An optical heterodyne system[3] illuminates the lensed surface of the packaged device (***Figure 5***), and the converted signal is measured by a 50-GHz network analyzer.

Figure 7 shows a typical frequency response of a 7-μm-diameter flip-chip detector. Its −3-dB electrical bandwidth is in excess of 50 GHz, which is in good agreement with our simulations. This state-of-the-art frequency performance is the result of careful minimization of the parasitic capacitance and inductance made possible by the micro-flip-chip technology.

Figure 7

Frequency response of a 7-μm-diameter flip-chip photodetector.



Experiments were done to eliminate concern that the stress induced on the detectors in the flip-chip bonding process might degrade the performance of the photodetectors. The dark current of the InP p-i-n photodetector is one of the parameters that is most sensitive to stress-induced damage. To determine the effect of induced stress, the dark current of a very large population of flip-chip-mounted photodetectors was monitored. On the average, the increase in dark current is insignificant and under 200 pA. The typical final dark current of a flip-chip-mounted photodetector is under 1 nA.

Typical dc responsivity of a 10-μm-diameter flip-chip detector with a 0.7-μm-thick i-layer or active layer is 0.8A/W. In comparison, the responsivity of standard (non-flip-chip) detectors with the same i-layer thickness is 0.55A/W. The enhanced responsivity of the flip-chip detector is a result of the incident light beam bouncing off the top metal contact and passing twice through the absorbing i-layer.

The InP microlens integrated at the back of the flip-chip detector significantly increases the effective light acceptance area of the detector. **Figure 8** shows the normalized optical responses of lensed and unlensed 25-μm flip-chip photodetectors. The lensed photodetector has an effective collection surface that is four times larger than the unlensed device. The advantage of having a microlens becomes more evident for smaller diameters.

Optical Receiver Performance

An optical receiver was designed and assembled employing a transimpedance amplifier based on a GaAs MODIC (modulation doped integrated circuit) and a 15-μm flip-chip photodiode as shown in **Figure 5**. The schematic diagram of the receiver circuit is shown in **Figure 9**.This transimpedance design was chosen to focus on the effect of die attaching techniques on the performance of the receiver. The measured frequency response of the receiver is shown in **Figure 10**. The −3-dB electrical bandwidth of the flip-chip optical receiver was 7.2 GHz and the conversion gain was 560V/W. The input referred noise current spectral density was 10 $pA/Hz^{1/2}$. In comparison, a similar optical receiver composed of the same GaAs MODIC-based amplifier and a wire-bonded 15-μm photodiode had a bandwidth of 4.2 GHz and an input referred noise current spectral density of 20 $pA/Hz^{1/2}$. The performance of the receiver is consistent with the improved bandwidth, smaller capacitance, and higher responsivity of the flip-chip detector.

Nine-Channel Optical Receiver

The flip-chip die attachment provides a capability for precise placement of the chip on predefined bump pads. During the reflow process, the surface tension of the molten solder will pull the chip to within a few micrometers of the predefined pads. This feature is very useful in the assembly of a multichannel optical receiver, which requires each detector element to be placed precisely at a predefined location to facilitate optical coupling and reduce cross talk.

Figure 8

Responses of unlensed (left) and lensed (right) 25-μm-diameter flip-chip photodetectors.

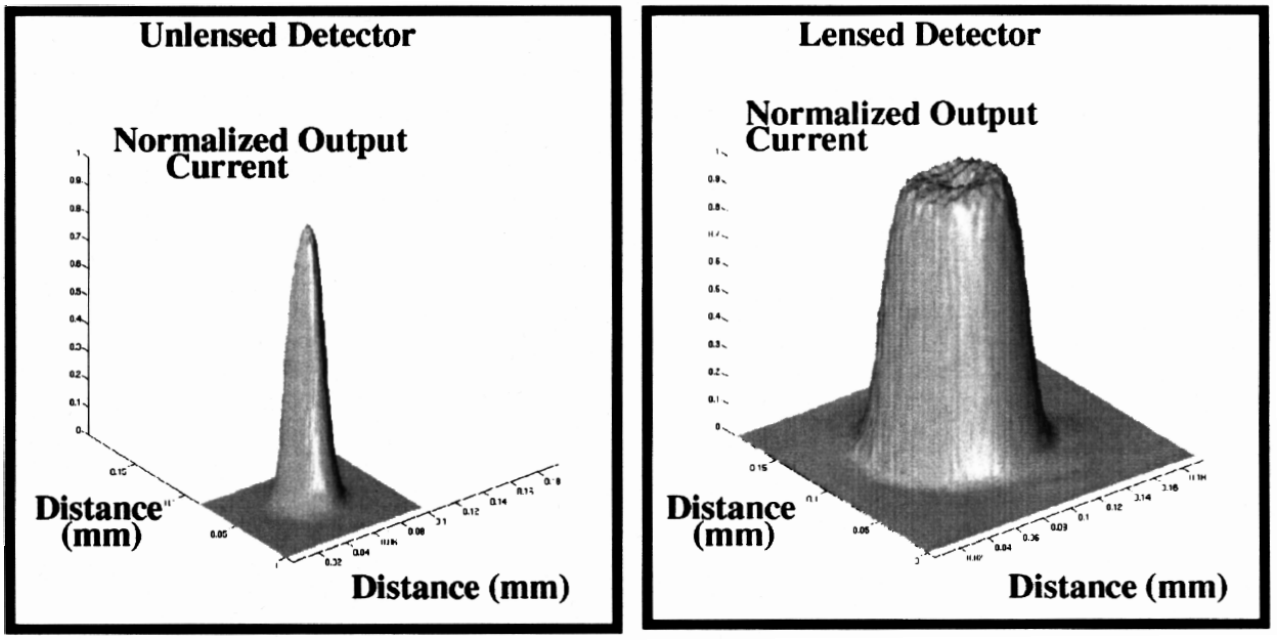


Figure 9

Schematic diagram of the optical receiver circuit.

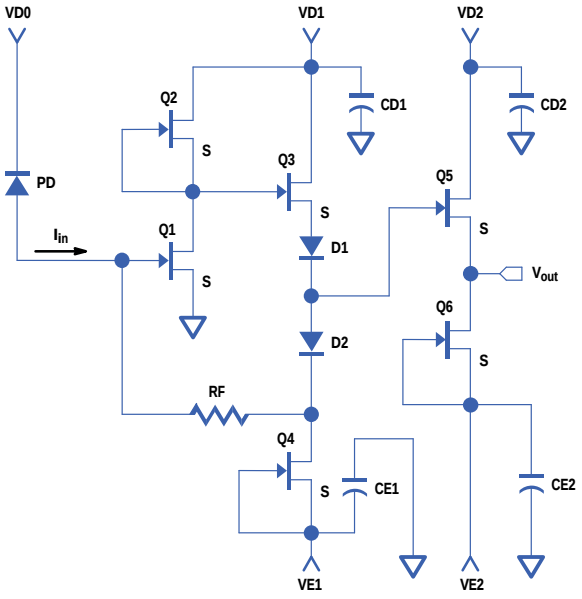
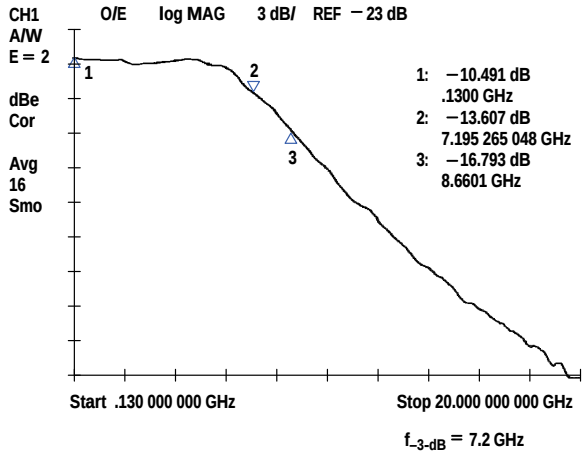


Figure 10

Measured frequency response of the optical receiver.



We have designed and fabricated a nine-channel silicon bipolar receiver IC that has nine sets of solder bump pads with nine photodetectors flip-chip bonded on them as shown in **Figure 11**. The electrical performance of each channel is tested by supplying a 1-Gbit/s NRZ pseudorandom optical input signal. The electrical output, as represented by the eye diagram shown in **Figure 12**, indicates 1-Gbit/s performance per channel.

Figure 11

Nine-channel optical receiver.

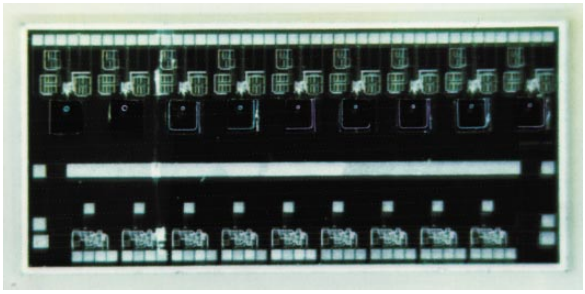
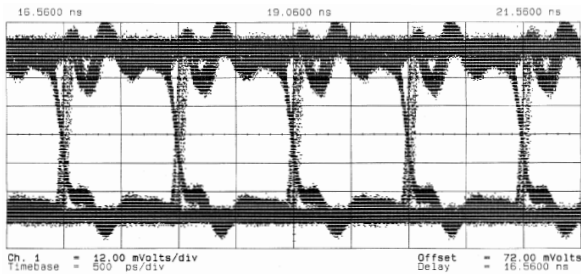


Figure 12

Output eye diagram of one channel of the nine-channel optical receiver with a 1-Gbit/s input signal.



Conclusion

We have successfully incorporated a micro-flip-chip technology with our optoelectronic components. In the flip-chip die attached form, a p-i-n photodetector with an i-layer thickness of 0.75 μm has an average responsivity of 0.8A/W at 1300 nm and a dark current of less than 1 nA. A 7-μm-diameter flip-chip photodetector has a −3-dB electrical bandwidth in excess of 50 GHz. The flip-chip optical receiver with a 15-μm detector has a measured −3-dB electrical bandwidth of 7 GHz while a wire-bonded version has a −3-dB bandwidth of 3.9 GHz. The self-aligning feature of the flip-chip die attachment is very useful in the assembly of a nine-channel optical receiver that operates at speeds in excess of 1 Gbit/s per channel. The same flip-chip technology can be easily combined with a vertical-cavity surface emitting laser (VCSEL) transmitter to realize a flip-chip optical transceiver.

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