Global Routing—A Block-Level Problem

For a given level within a chip hierarchy, the routing plane is generally occupied by a number of blocks with ports that need to be connected by physical wires on nets. The blocks are usually restricted to be rectilinear in shape but are allowed to vary in size. The space between the blocks is generally reserved for routing and is usually subdivided into adjacent routing *regions* or *channels* so that the routing problem can be solved with a divide-and-conquer approach. Within each region, a certain number of layers are reserved for routing the signals at the given level. Global routing is the first step in the routing process. Its job is to generate a routing plan in which each signal is assigned to a number of routing regions. The objectives for the global router are to achieve 100% assignment of signals to available routing regions, to minimize the overall chip size, and to ensure that the timing requirements of the signals are met.

The global routing problem is generally represented by a *global routing graph*, which depicts the relationships between routing regions and ports to be connected. The edges of a global routing graph represent the routing regions and the nodes represent the intersections between regions and the ports. The edges are assigned *weights*, which can be the distance between two region intersections, the distance between a port and the nearest region, the cost for using a particular layer in the region, a penalty for switching routing layers, or a penalty for overflowing a region. Global routing is accomplished by implementing a lowest-cost path-finding algorithm on the global routing graph.

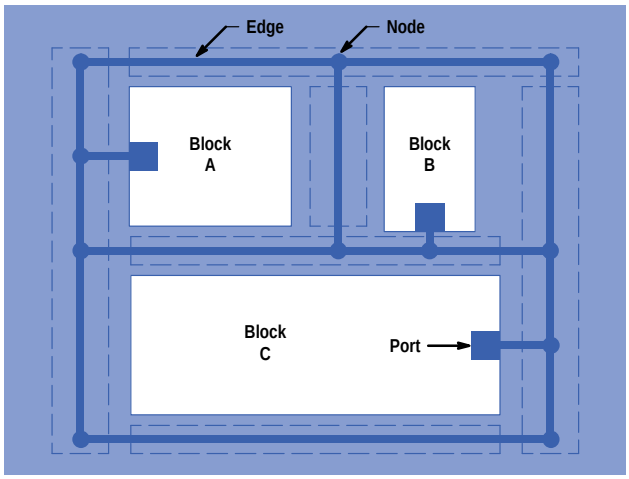

Fig. 1. *Global routing graph. Regions are indicated by dashed outlines.*

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