

General-Purpose 3V CMOS Operational Amplifier with a New Constant-Transconductance Input Stage

Design trade-offs for a low-voltage two-stage amplifier in the HP CMOS14 process are presented and some of the issues of low-voltage analog design are discussed. The design of a new constant-transconductance input stage that has a rail-to-rail common-mode input range is described, along with the rail-to-rail class-AB output stage. The performance specifications and area of this amplifier are compared with a similar design in a previous process, CMOS34.

by **Derek L. Knee and Charles E. Moore**

Experience gained over the last few years within the design centers of the HP Integrated Circuit Business Division (ICBD) has shown that a general-purpose operational amplifier is a fundamental building block for many mixed-signal integrated circuits. These general-purpose operational amplifiers are typically used in support functions and not in the high-frequency differential signal paths.

With the recent process release of AMOS14TB, the analog version of the HP CMOS14TB IC process, the logical step was to design a general-purpose operational amplifier for use with mixed analog/digital chips using AMOS14TB. However, from an analog standpoint, the technology change from CMOS34, the most recent process in which analog circuits had been implemented, to CMOS14 was quite severe because of the power supply reduction from 5V to 3.3V. Because of the lower supply voltage specification, new circuit design techniques needed to be developed and the general-purpose operational amplifier was chosen as one of the test vehicles to achieve this goal. The amplifier was also integrated onto an AMOS14 test chip.

Design Objectives

Because of the usefulness of the previous CMOS34 general-purpose operational amplifier, the electrical specifications for the AMOS14 version were derived from the CMOS34 amplifier. The power supply range was altered because of the technology change. Other parameters such as input offset voltage, input referred noise, and size were to be minimized, while open-loop voltage gain, gain margin, phase margin, and power supply rejection ratio were to be maximized. A list of the design objectives is shown in Table I.

Configuration

Based on the design objectives shown in Table I and the experience of the authors in the design of previous general-purpose operational amplifiers, a two-stage configuration

with a class-AB output stage was chosen. This configuration is capable of satisfying the power and load requirements. An added constraint for the AMOS14 version (based on limitations of the previous versions) is the specification for constant small-signal bandwidth, independent of the common-mode input range, CMIR. The amplifier has a differential input, and the common-mode input voltage is the average value of the two input voltages. CMIR is the range over which the common-mode input voltage is expected to vary. A small-signal bandwidth that is independent of CMIR implies that the input differential stage has a constant small-signal input transconductance, g_m , over the full CMIR, even if the CMIR is as large as the difference between the power supply rails.

Leveraging the new AMOS14 circuit design from the existing CMOS34 design was difficult because the power supply voltage range is reduced while the PMOS and NMOS transistor thresholds, V_{ip} and V_{tn} respectively, are essentially unchanged. The power supply range for AMOS14 is reduced by 33% from that of CMOS34. This power supply reduction is fairly significant for analog designs in which devices are connected in series. The outcome was that new low-voltage design techniques had to be employed to implement the equivalent operational amplifier in AMOS14 technology.

Table I
Design Objectives for AMOS14 Operational Amplifier

Parameter	Target Value
Single-supply operation	$2.7V \leq AV_{DD} \leq 3.6V$
Temperature range T_{op}	$0^\circ C \leq T_{op} \leq 110^\circ C$
Outputs	Single-ended
Low quiescent power consumption	$I_{DD} \leq 1 \text{ mA}$
Small-signal bandwidth f_o (unity gain)	$1 \text{ MHz} \leq f_o \leq 5 \text{ MHz}$
Small-signal bandwidth	Independent of CMIR
Slew rate SR	$1V/\mu s \leq SR \leq 5V/\mu s$
Output voltage range	$AV_{SS} + 0.2V \leq V_{out} \leq AV_{DD} - 0.2V$
Common-mode input range CMIR	$AV_{SS} \leq CMIR \leq AV_{DD}$
Load capacitance range	$C_{load} \leq 100 \text{ pF}$
Load resistance range	$R_{load} \geq 300\Omega$

Constant-Transconductance Differential Input Stage

To obtain a differential input stage that operates over a rail-to-rail input voltage range requires an NMOS and PMOS pair driven in parallel. Because of complementary biasing requirements, special circuit design precautions need to be taken to ensure that the overall g_m , or the sum of the individual transistor g_m s, remains constant over the CMIR. Without this added circuitry, the frequency compensation could not be optimized over the CMIR.

The requirements for the constant- g_m input stage are:

- A simple circuit with a minimum number of components
- Low-voltage operation
- Input devices operating in the square-law region where g_m is highest.
- Constant- g_m control circuitry operating in a closed-loop mode with the input differential devices to exhibit smooth transition regions over the CMIR
- Constant- g_m control circuitry that does not use reference voltage trip levels to control the differential bias currents, thus avoiding coupling supply noise into the input stage.

An extensive search of the literature¹⁻¹⁴ could not locate a circuit that met this list of requirements. Therefore, a new constant- g_m input stage was needed.

If I_{tn} and I_{tp} are the tail currents of the NMOS and PMOS differential pairs respectively, then the following relationship is required for any common-mode input voltage:

$$\sqrt{2K_n I_{tn}} + \sqrt{2K_p I_{tp}} = g_m = \text{Constant}, \quad (1)$$

where

$$K_n = \mu_n C_{ox} \frac{W_n}{2L_n} \quad (2a)$$

and

$$K_p = \mu_p C_{ox} \frac{W_p}{2L_p}. \quad (2b)$$

In equations 2a and 2b, μ is the carrier mobility under the channel, C_{ox} is the transistor gate capacitance per unit area, W is the transistor gate width, and L is the transistor gate length.

If the PMOS and NMOS transistors are sized so that $K_n = K_p$ then equation 1 can be rewritten as:

$$\sqrt{I_{tn}} + \sqrt{I_{tp}} = \text{Constant}. \quad (3)$$

A new feedback control loop circuit was designed that controls the bias currents in the NMOS and PMOS differential pair transistors so that equation 3 holds for all common-mode input voltages. This new circuit is shown in Fig. 1. It uses what the authors refer to as the 4I/I principle.

In Fig. 1, transistors N0A, N0B, N1A, and N1B form the NMOS input section. Devices P0A, P0B, P1A, and P1B form the PMOS input section. These two sections together form the input stage to an operational amplifier. The output currents from these sections— I_{OPP} , I_{OPN} , I_{ONP} , and I_{ONN} —are summed in the first gain stage, described below. It is the overall g_m of these NMOS and PMOS input devices that is held constant over the CMIR.

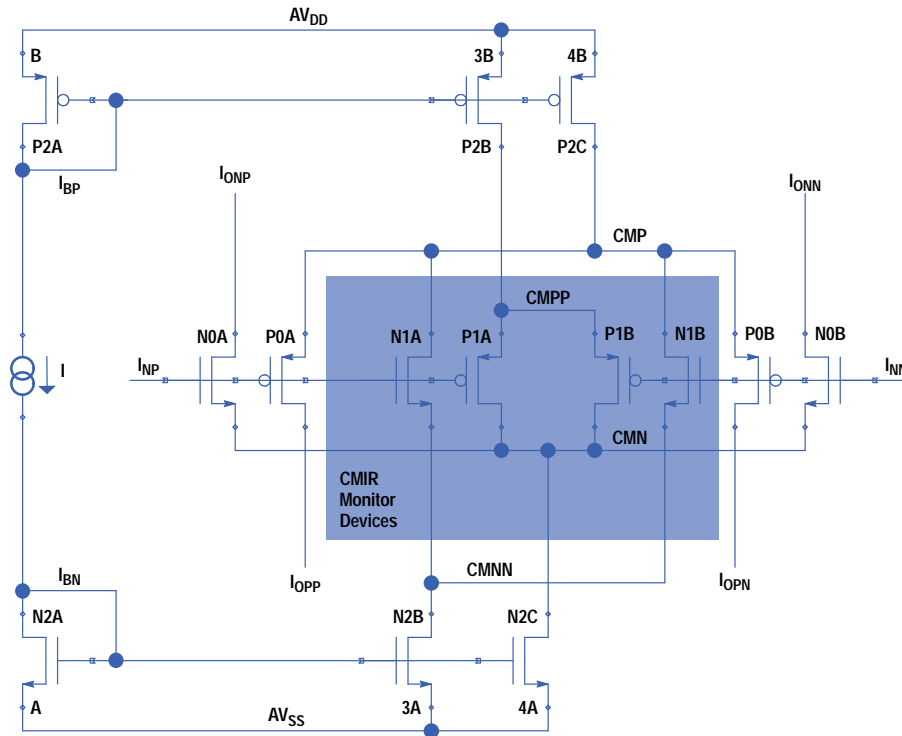


Fig. 1. Constant-transconductance amplifier input stage.

The current mirror N2C biases the NMOS input pair and the current mirror P2C biases the PMOS input pair. The NMOS CMIR monitor devices, N1A and N1B, are biased by N2A and N2B at a current of $3I$. The PMOS CMIR monitor devices, P1A and P1B, are also biased by P2A and P2B at a current of $3I$.

For midsupply common-mode input range, both the NMOS input section and the PMOS input section are biased on. The PMOS CMIR input monitor devices, P1A and P1B, source a current of $3I$ to the node CMN. This $3I$ source current is added algebraically to the $4I$ current sink of N2C, resulting in the NMOS differential pair, N0A and N0B, being biased at a current I . Similarly, the NMOS CMIR input monitor devices, N1A and N1B, sink a current of $3I$ from the node CMP. This $3I$ current is added algebraically to the $4I$ source current of P2C, resulting in the PMOS differential pair, P0A and P0B, being biased at a current I . Therefore the NMOS and PMOS input sections are both biased at I for the midsupply common-mode input.

For common-mode inputs near AV_{DD} , the NMOS input section is biased correctly, but the PMOS input section is off. The current source devices P2B and P2C are also off and the PMOS CMIR monitor devices, P1A and P1B, supply no current. Since no current is added to the current source N2C, the NMOS differential pair, N0A and N0B, is now biased at a current of $4I$. A similar argument holds for the PMOS devices when the common-mode input is close to AV_{SS} , and the PMOS transistors are biased at $4I$.

The differential input sections will be biased in one of the following modes:

1. The NMOS devices biased at $4I$ and the PMOS section with no bias current for low CMIR:

$$\sqrt{4I} + \sqrt{0I} = \text{Constant.} \quad (4a)$$

2. The PMOS devices biased at $4I$ and the NMOS section with no bias current for high CMIR:

$$\sqrt{0I} + \sqrt{4I} = \text{Constant.} \quad (4b)$$

3. Both sections biased at I when the CMIR is such that both N2B and P2B are biased correctly:

$$\sqrt{1I} + \sqrt{1I} = \text{Constant.} \quad (4c)$$

The closed-loop CMIR monitor circuitry smoothly controls the transition between these three modes of operation. This is demonstrated in Fig. 2. The x-axis of Fig. 2 represents the CMIR from AV_{SS} to AV_{DD} (rail to rail). The upper curve shows the overall g_m or the sum of the NMOS and PMOS input stage g_m s, while the lower curves show the individual g_m s of the input sections as a function of CMIR. The overall g_m has a total variation of only 5%. This number includes the second-order effects of subthreshold operation and output conductance.

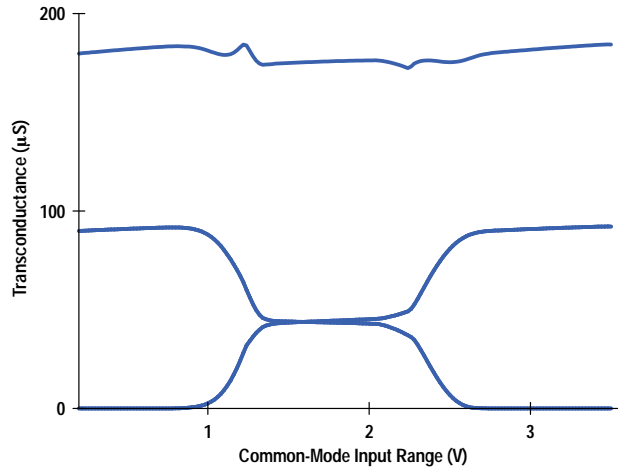


Fig. 2. The x-axis represents the common-mode input range (CMIR) of the circuit of Fig. 1 from AV_{SS} to AV_{DD} (rail to rail). The upper curve shows the overall g_m . The lower curves show the individual g_m s of the input sections as a function of the CMIR.

Fig. 3 shows the simulated variation of the intrinsic input offset voltage, V_{os} , as a function of the CMIR. This curve shows one of the limitations of a complex input differential pair input structure: the input offset voltage varies as each of the input differential pairs is activated or deactivated. During the transitions between modes, the common-mode rejection ratio, CMRR, is reduced.¹⁻¹² Therefore, the design of Fig. 1 attempts to minimize the width of these transition regions with respect to CMIR.

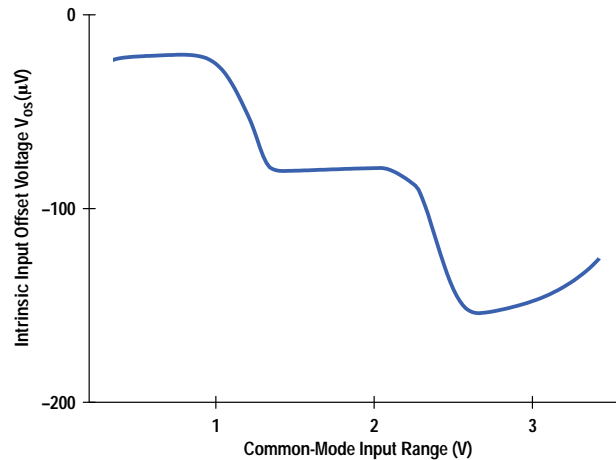


Fig. 3. Simulated variation of the intrinsic input offset voltage, V_{os} , as a function of the CMIR.

First Gain Stage

The first gain stage sums the four output currents from the input differential stage: I_{OPP} , I_{OPN} , I_{ONP} , and I_{ONN} . The criteria for selecting the best gain stage were:

- The stage should use wide-swing cascode current sources.
- It should interface easily with the following class-AB output stage or second gain stage.
- It should not add any additional noise or offset to the input stage.

The gain and current summing stage selected is shown in Fig. 4.¹⁴ This stage reduces the transistor count considerably because of its compact integration with the class-AB output stage (see next section).

Second Gain Stage

The criteria used in the selection of the class-AB output stage implementation were:

- Simple and high-speed design
- No complex active or amplifier feedback paths in the AB control circuitry
- Low- V_{DD} operation

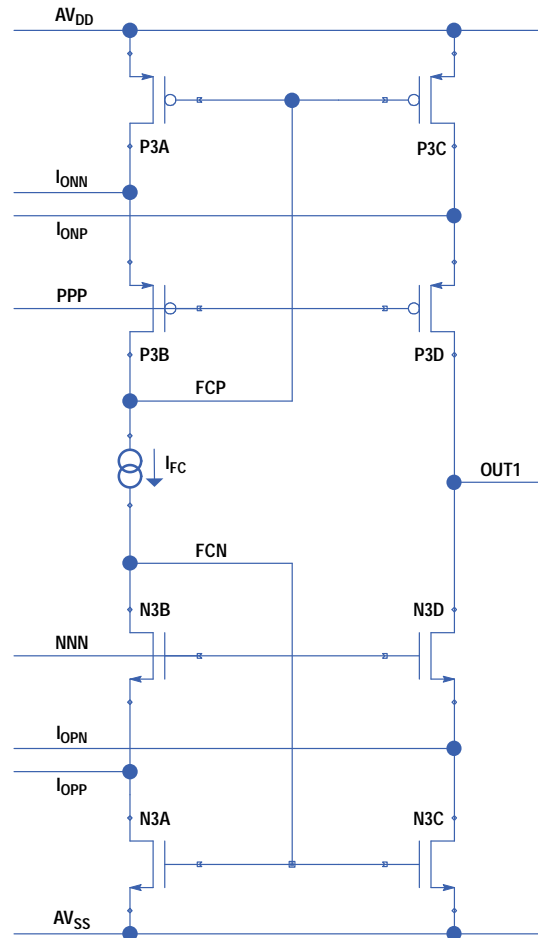


Fig. 4. Schematic diagram of the first gain stage, which sums the four output currents from the input stage.

- Good power supply rejection ratio
- No direct dependence on supply voltage for bias current setup
- No noise or offset to be added to the first stage of the amplifier.

The output stage chosen is shown in Fig. 5. The circuit shown in Fig. 5a is a simplified version of the output stage. The schematic in Fig. 5b shows the implementation of the AB output stage integrated together with the first gain stage. This output stage was first developed for 5V operation¹⁵ and later modified for an all-digital process.¹⁶

The output stage uses common-source output devices for low-voltage operation. The theoretical minimum supply voltage is twice the MOS threshold voltage plus a saturation voltage. The complementary output devices PDR and NDR are driven by complementary common-gate level shifters, PAB and NAB. The first-stage input signals are fed into the output stage at nodes PDRV and NDRV. During quiescent operation, PAB and NAB are biased in the conducting state. The potentials at PDRV and NDRV are established to minimize the quiescent current through the large output driver devices, PDR and NDR. This biasing arrangement is established through two translinear loops. The loop that biases PDR consists of P5A, P5B, PAB, and PDR. Similarly, NDR is biased by the loop consisting of N5A, N5B, NAB, and NDR. For a short tutorial on translinear theory see [reference 17](#).

During a negative slew at the output, the gate voltage of NDR is pulled high. Since the bias voltage ABN is fixed, the device NAB will shut off. The device PAB will be then conducting the full bias current, I_{FC} , which will result in an increase in the gate-to-source voltage of PAB and consequently a reduction in the gate-to-source voltage of PDR. A similar operation occurs during positive sourcing when the bias voltage for NDR is reduced.¹⁵

The integration of the class-AB stage and the first gain stage has two major advantages. The first advantage is the floating current source, I_{FC} , which is set up through two additional translinear loops: N5A, N5B, NFC, N3A and P5A, P5B, PFC, P3A. Because of the floating nature of the bias devices NFC and PFC and NAB and PAB, this current source contributes much less to the noise and offset of the amplifier. Secondly, the variation of the output quiescent current is reduced because the floating current source of PFC and NFC tracks the AB current source of NAB and PAB.

Final Circuit and Results

The complete schematic for the AMOS14 operational amplifier is shown in Fig. 6. This figure shows in detail the cascode current source implementation.

Fig. 7 shows the open-loop small-signal frequency response and phase characteristics of the amplifier driving four different load combinations. These are $10\text{ M}\Omega\|1\text{ pF}$, $10\text{ M}\Omega\|100\text{ pF}$, $300\Omega\|1\text{ pF}$, and $100\Omega\|100\text{ pF}$. Fig. 8 shows the small-signal frequency response and phase characteristics of the amplifier for different CMIR values ranging from AV_{SS} to AV_{DD} . Note that the unity-gain frequency f_o is essentially independent of CMIR.

The small-signal step response is shown in Fig. 9 for the same load combinations as Fig. 7. The large-signal step response, indicative of the amplifier's slew rate, is shown in Fig. 10. The artwork layout for the operational amplifier is shown in Fig. 11.

Table II illustrates the overall similarities of the AMOS14 operational amplifier to the CMOS34 version. In summary, the AMOS14 design achieved a $2\times$ improvement in bandwidth, a $2.5\times$ increase in class-AB output drive, and a $3\times$ improvement in slew rate in a third of the area while at the same time including the additional constant- g_m circuitry.

Table II
Amplifier Process Comparison

Parameter	AMOS14	CMOS34
Supply voltage	2.7 to 3.6V	4.5 to 5.5V
Supply current	625 μ A	750 μ A
Common-mode input range CMIR	AV_{SS} to AV_{DD}	AV_{SS} to AV_{DD}
Constant- g_m input stage	Yes	No
Input stage g_m variation, $AV_{SS} \leq \text{CMIR} \leq V_{DD}$	$< \pm 5\%$	50%
Intrinsic input offset voltage, $\text{CMIR} = AV_{DD}/2$	$-80\ \mu\text{V}$	$-120\ \mu\text{V}$
Resistive load	300 Ω min	300 Ω min
Capacitive load	100 pF max	100 pF max
Maximum output drive current I_{max}	$\pm 5\text{ mA}$	$\pm 2\text{ mA}$
Maximum output swing at I_{max}	$AV_{DD} - 0.25$	$AV_{DD} - 0.3$
Minimum output swing at I_{max}	$AV_{SS} + 0.25$	$AV_{SS} + 0.3$
Open-loop gain (no load)	$> 100\text{ dB}$	$> 100\text{ dB}$
Slew rate	6V/ μ s	0.5V/ μ s*
Unity-gain bandwidth, f_o	4 MHz	0.5MHz*
Phase margin **	55 degrees	49 degrees
Gain margin **	-19 dB	-8 dB
PSRR +, $AV_{SS} \leq \text{CMIR} \leq AV_{DD}$	$> 70\text{ dB}$	$> 80\text{ dB}$
PSRR -, $AV_{SS} \leq \text{CMIR} \leq AV_{DD}$	$> 70\text{ dB}$	$> 80\text{ dB}$
Cell size	251 $\mu\text{m} \times 141\mu\text{m}$	460 $\mu\text{m} \times 210\ \mu\text{m}$

* Depends on CMIR.

** Absolute worst-case conditions for I_{bias} , AV_{DD} , R, C, models. See Fig. 7.

CMIR = common-mode input range.

PSRR = power supply rejection ratio.

Acknowledgments

The authors thank their project manager, Rajeev Badyal, for his encouragement during the development of this amplifier.

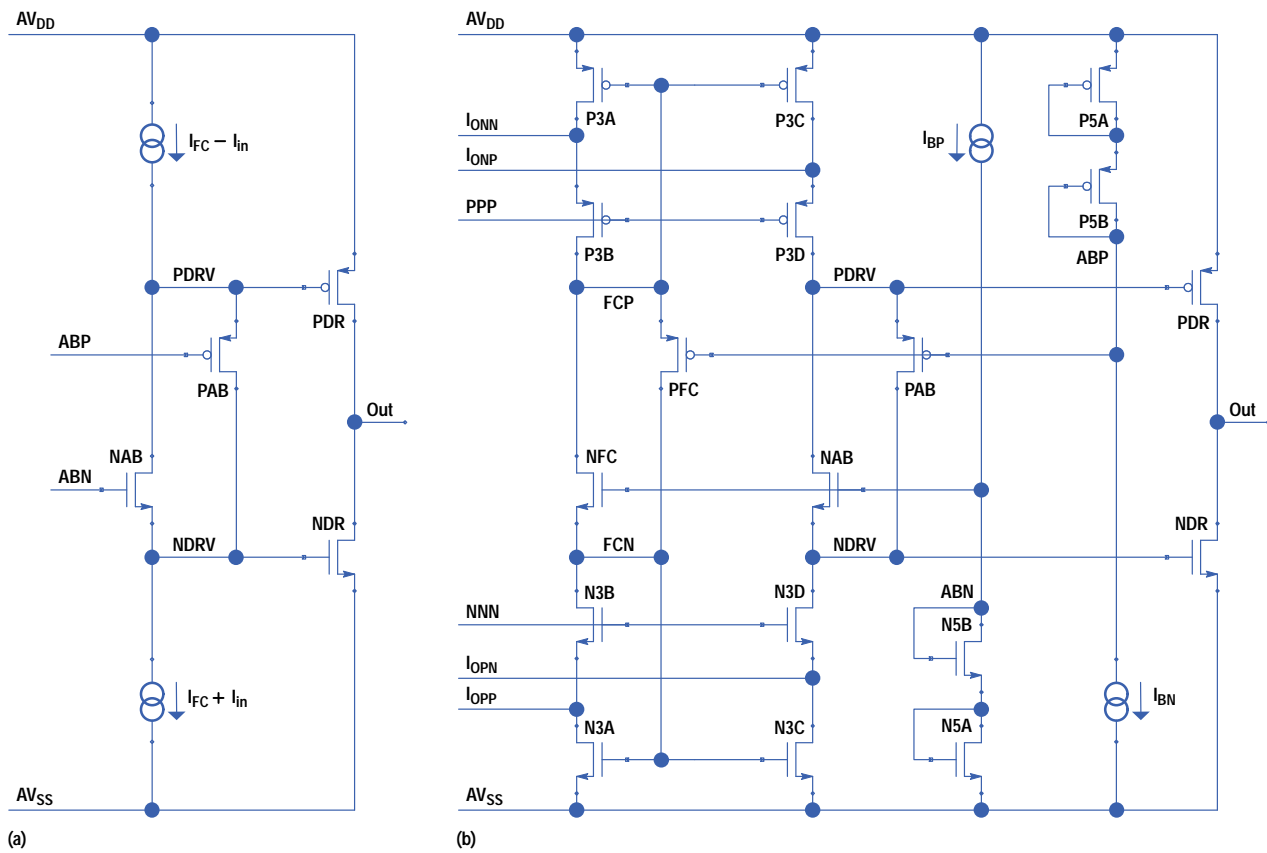


Fig. 5. (a) Simplified schematic diagram of the output stage.
 (b) Integration of the output stage with the first gain stage.

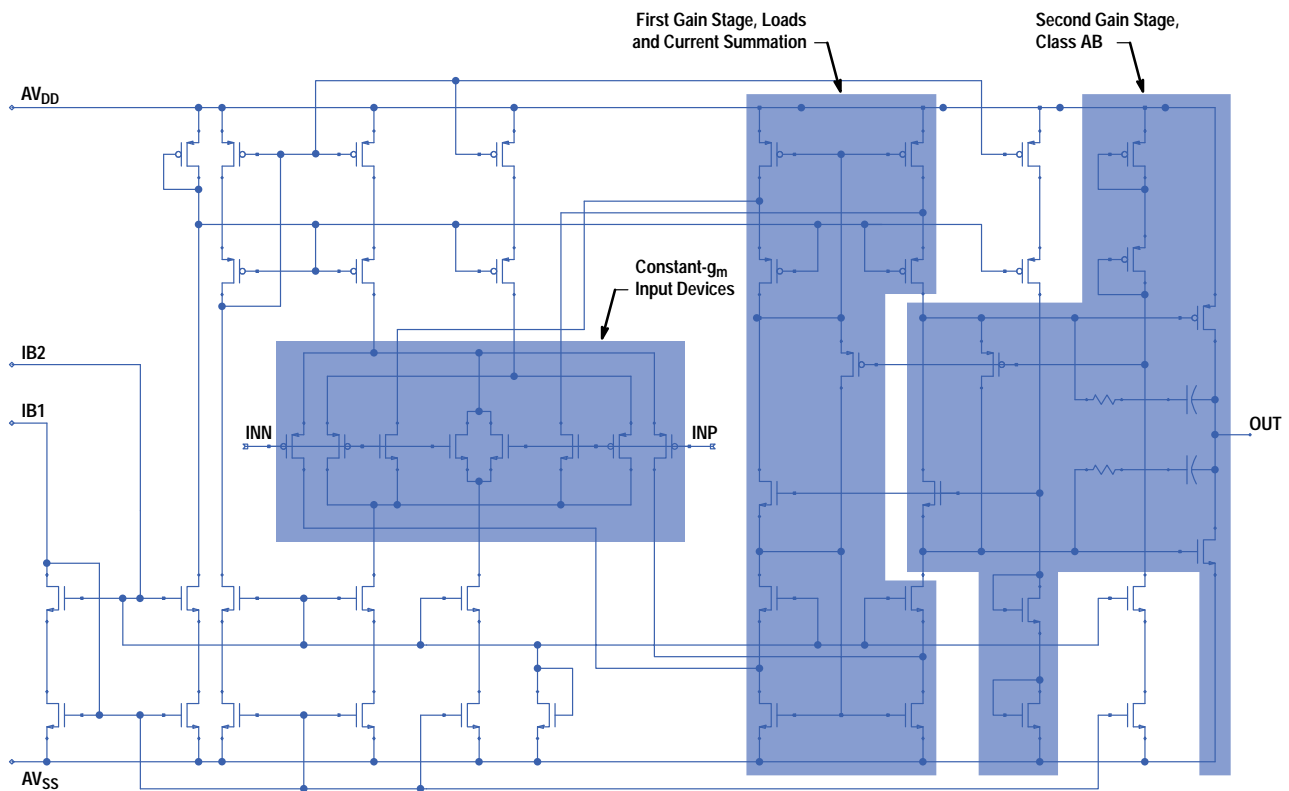


Fig. 6. Complete schematic diagram of the AMOS14 operational amplifier. The unshaded area contains bias support circuitry.

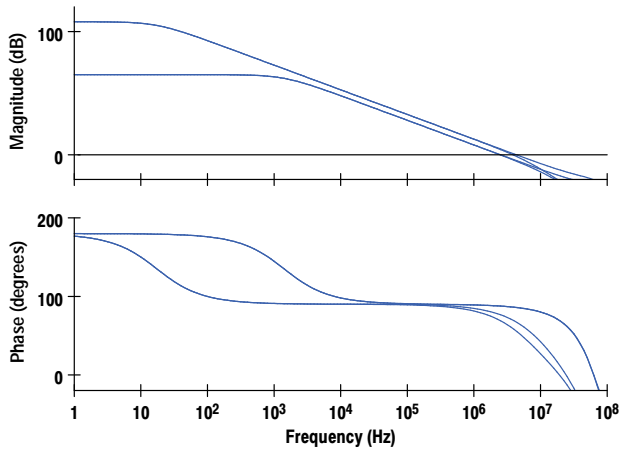


Fig. 7. (top) Open-loop small-signal frequency response for different load conditions. (bottom) Phase response.

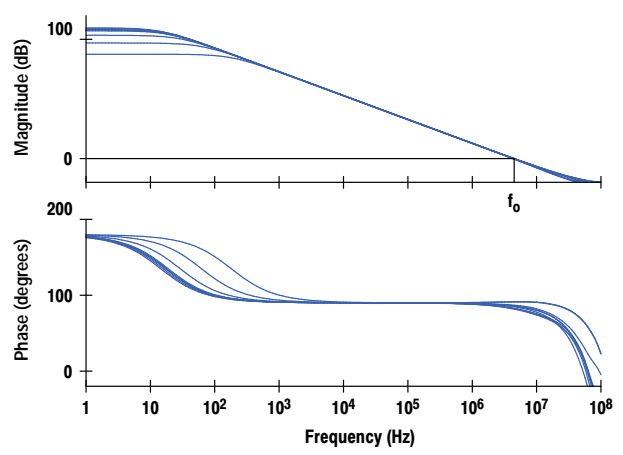


Fig. 8. (top) Small-signal frequency response for different CMIR values. (bottom) Phase response.

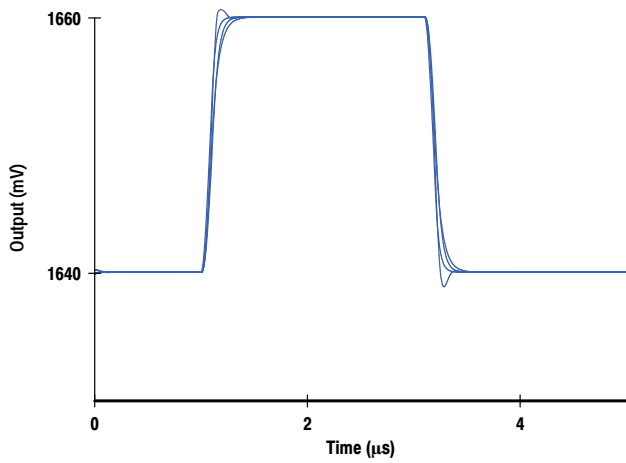


Fig. 9. Small-signal step response for different load conditions.

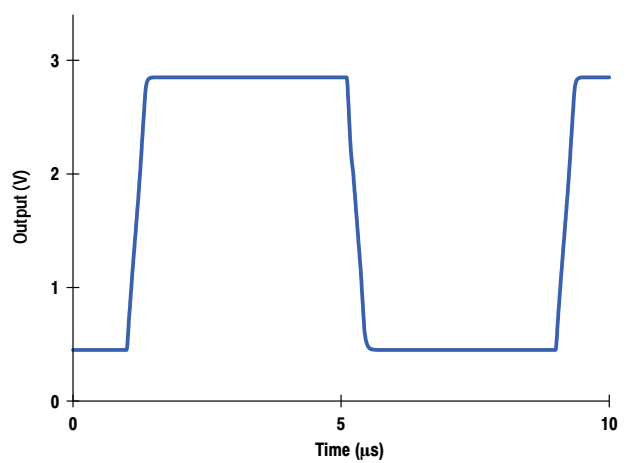


Fig. 10. Large-signal step response, indicative of slew rate.

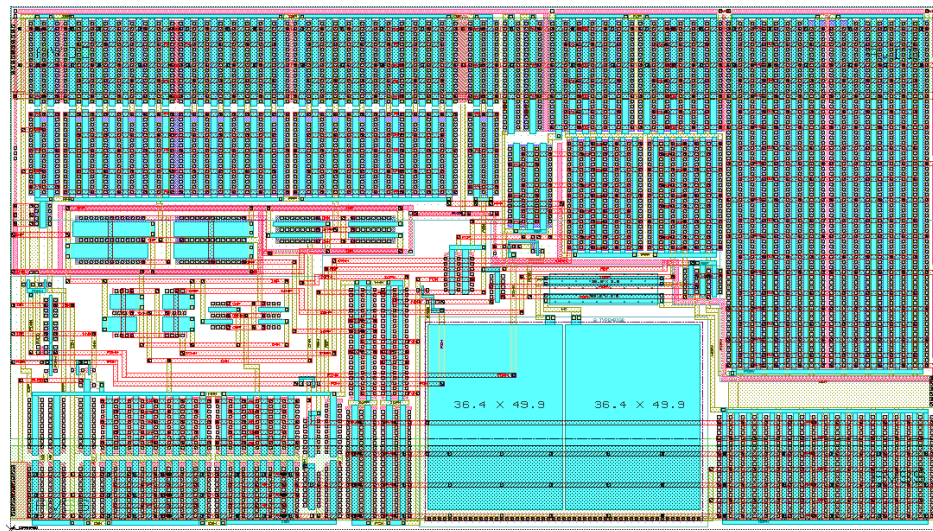


Fig. 11. Operational amplifier layout.

References

1. J.H. Huijsing and D. Linebarger, "Low-voltage operational amplifier with rail-to-rail input and output ranges," *IEEE Journal of Solid-State Circuits*, Vol. SC-20, December 1985, pp. 1144-1150.
2. M.J. Fonderie and J.H. Huijsing, *Design of Low-Voltage Bipolar Operational Amplifiers*, Kluwer Academic Publishers, 1993.
3. J. Fonderie, M.M. Maris, and E.J. Schnitger, "1-V operational amplifier with rail-to-rail input and output ranges," *IEEE Journal of Solid-State Circuits*, Vol. SC-24, December 1989, pp. 1551-1559.
4. J.A. Fisher and R. Koch, "A highly linear CMOS buffer amplifier," *IEEE Journal of Solid-State Circuits*, Vol. SC-22, June 1987, pp. 330-334.
5. M. Steyaert and W. Sansen, "A high-dynamic-range CMOS op amp with low-distortion output structure," *IEEE Journal of Solid-State Circuits*, Vol. SC-22, December 1987, pp. 1204-1207.
6. J.N. Babanezhad, "A rail-to-rail CMOS op amp," *IEEE Journal of Solid-State Circuits*, Vol. 23, December 1988, pp. 1414-1417.
7. T.S. Fiez, H.C. Yang, J.J. Yand, C. Yu, and D.J. Allstot, "A family of high-swing CMOS operational amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. 24, December 1989, pp. 1683-1687.
8. M.D. Pardoen and M.G. Degrauwe, "A rail-to-rail input/output CMOS power amplifier," *IEEE Journal of Solid-State Circuits*, Vol. 25, April 1990, pp. 501-504.
9. R. Hogervorst, R.J. Wiegierink, P.A. de Jong, J. Fonderie, R.F. Wassenaar, and J.H. Huijsing, "CMOS low-voltage operational amplifiers with constant- g_m rail-to-rail input stage," *Proceedings of the IEEE International Symposium on Circuits and Systems*, 1992, pp. 2876-2879.
10. J.H. Botma, R.F. Wassenaar, and R.J. Wiegierink, "A low-voltage CMOS op amp with rail-to-rail constant- g_m input stage and a class-AB rail-to-rail output stage," *Proceedings of the IEEE International Symposium on Circuits and Systems*, 1993, pp. 1314-1317.
11. R. Hogervorst, R.J. Wiegierink, P.A.D. Jong, J. Fonderie, R.F. Wassenaar, and J.H. Huijsing, "CMOS low-voltage operational amplifier with constant- g_m rail-to-rail input stage," *Analog Integrated Circuits and Signal Processing*, Vol. 5, Kluwer Academic Publishers, 1994, pp. 135-146.
12. J. Huijsing, R. Hogervorst, J. Fonderie, B. van der Dool, K.-J. de Langen, and G. Groeneveld, "Low-voltage signal processing," *Analog VLSI: Signal and Information Processing* (Ismail and Fiez, editors), Chapter 4, McGraw-Hill, 1994.
13. S. Sakurai and M. Ismail, *Low-Voltage CMOS Operational Amplifiers: Theory, Design and Implementation*, Kluwer Academic Publishers, 1995.
14. R. Hogervorst, J.P. Tero, R.G. Eschauzier, and J.H. Huijsing, "A compact power-efficient 3V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE Journal of Solid-State Circuits*, Vol. SC-29, December 1994, pp. 1505-1513.
15. D. M. Montecelli, "A quad CMOS single-supply op amp with rail-to-rail output swing," *IEEE Journal of Solid-State Circuits*, Vol. SC-21, December 1986, pp. 1026-1034.
16. W.-C.S. Wu, W.J. Helms, J.A. Kuhn, and B.E. Byrnett, "Digital-compatible high-performance operational amplifier with rail-to-rail input and output ranges," *IEEE Journal of Solid-State Circuits*, Vol. SC-29, January 1994, pp. 63-66.
17. J.H. Botma, R.J. Wiegierink, A.J. Gierkink, and R.F. Wassenaar, "Rail-to-Rail Constant- g_m Input Stage and Class-AB Output Stage for Low-Voltage CMOS Op Amps," *Analog Integrated Circuits and Signal Processing*, Vol. 6, Kluwer Academic Publishers, 1994, pp. 121-133.

▶ [Go to Next Article](#)

▶ [Go to Journal Home Page](#)