High-Sample-Rate Multiprocessor-Based Oscilloscopes

The HP 54615B and 54616B oscilloscopes blend proprietary high-speed sampling technology with the power of digital signal processing and a proven user interface to deliver usable advanced characterization capability.

by R. Scott Brunton

The design of the HP 54615B and 54616B oscilloscopes (Fig. 1) focused on adding higher sample rate and extended memory depth to the attributes of the HP 54600 product family.[1] Increasing the sample rate to 1 GSa/s and 2 GSa/s, respectively, broadens the confidence that narrow signal transients will be acquired and, combined with very responsive front-panel controls, presents a visually dense image of the acquired waveform. To provide reliable acquisitions over even the slowest time base settings, special hardware can be engaged to detect and capture peaks as narrow as 1 ns in width.

Successful development depended on retaining the personality of the HP 54600 family by projecting "the feel of analog and the power of digital" along the many dimensions of the customer use model.

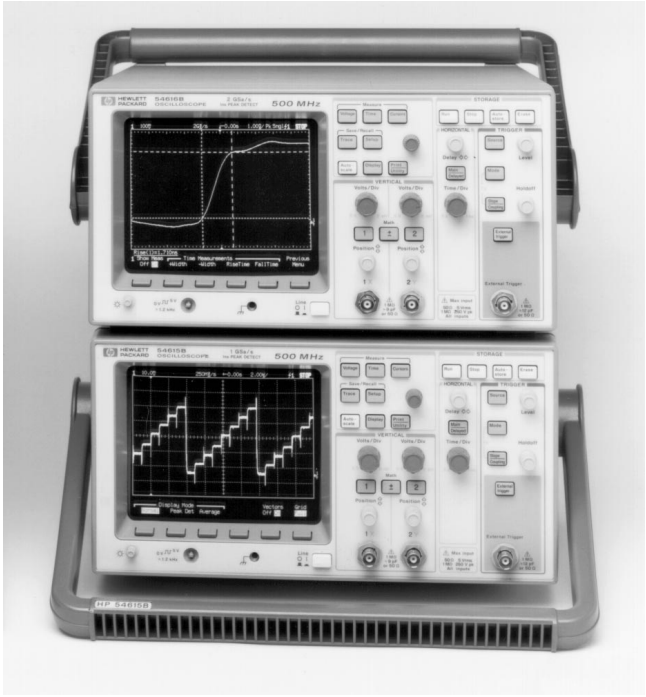

Fig. 1. *The HP 54616B oscilloscope (top) and the HP 54615B oscilloscope (bottom) offer higher sample rates and extended memory depth.*

Product Description

The HP 54515B/16B represent variants on the same software platform. Pursuing this commonality in the underlying software allows efficient delivery of the features and strengths of previous HP 54600 products. To ensure the analog feel of the user interface, fast display update and crisp display quality were cornerstone metrics. Bezel-mounted softkeys facilitate access to advanced control features, and front-panel controls are derived based on the function and operation of classical analog oscilloscopes. Each of the two independent channels delivers a system analog bandwidth of 500 MHz.

Behind the CRT display system and familiar front-panel design is a microprocessor-based acquisition platform that centralizes the overall scheduling of acquisitions and subsequent data filtering and abstraction. Instrument control is through

user front-panel actions or remote control via the HP-IB (IEEE 488, IEC 625) or RS-232. Printers are supported to provide hard-copy imaging of acquisitions and setups.

Optional expansion modules deliver seamless access to additional postprocessing capabilities and full-featured I/O connectivity. Standard 1-ns digital peak detection, advanced measurement functions, and the ability to view events occurring before a trigger permit accurate and detailed characterization of target system designs.

HP 54615B/16B Architecture

Extending the architecture developed for earlier product family members,[1] these new products leverage proprietary technology blocks to deliver added performance. The improved architecture is represented in Fig. 2. Waveform update rate and instrument performance are increased through the delegation of primitive tasks to slave processing elements. Three processors are used. Each has specific tasks and responsibilities that result in a parallel processing boost in responsiveness and a reduction in the "blind" time between acquisitions.

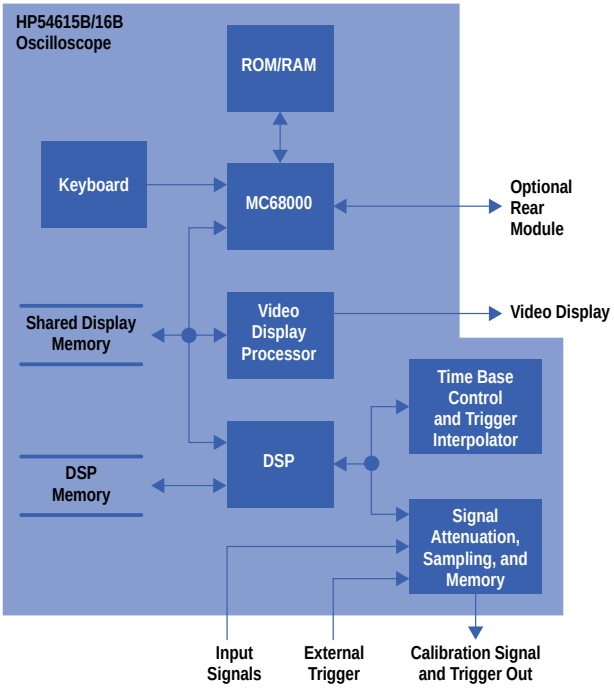

Fig. 2. *Architectural block diagram of the HP 54615B and 54616B oscilloscopes.*

Host Processor

The MC68000 host microprocessor is responsible for the general control and operation of the product. It is the sole provider of service to the front panel, which is of high priority because instrument responsiveness is directly associated with this processor's performance.

In addition to this task, the host maintains communication with and dispatches tasks to the other two processing blocks, where automatic measurements are performed on acquired data and interaction with the optional modules takes place.

During an acquisition, the host processor also tracks the current run state of the instrument and coordinates the subsequent software processing.

Video Display Processor

Once data has been acquired and placed into shared memory for display, the video display processor postprocesses the data record. Data is translated from a time-correlated, sequential organization to one that is appropriate for the display controller. In addition, vector processing on raw data can be performed. This dedicated display processing resource results in a net reduction in the capture-to-display time.

Digital Signal Processor

The TI320C50 digital signal processor (DSP) acts like an acquisition subsystem controller and data processor. It is a slave to the host MC68000 from which it receives instrument state information. The DSP manages the time base and performs sample rate generation. Once a valid trigger is recognized and data is acquired and unloaded from the dedicated front-end acquisition system, the DSP performs time correlation in preparation for postprocessing.

Working at cycle times far shorter than that available on the host MC68000, the DSP, depending on the acquisition mode, performs record averaging and primary vector compression. This processed data record is transferred into a shared memory segment and control is passed back to the host processor. Of significance is the fact that the video display processor accesses this same shared memory segment to transfer the newly acquired record into video RAM without any support from the host. Thus, acquisition-to-display time is markedly superior to methods that require host involvement.

Completion of the acquisition cycle is communicated to the host and, if necessary, the trigger and front-end hardware are reprogrammed and armed for the next acquisition.

Acquisition Front End

The HP 54615B/16B gain many of their capabilities by leveraging hardware technology from other members of the HP 54600 product family. The combined analog attenuation and digital sampling system delivers a signal-input rise time of 700 ps and a sampling rate of 1 or 2 GSa/s. This produces an effective repetitive bandwidth of 500 MHz on both products and a single-shot bandwidth of 250 MHz on the HP 54615B and 500 MHz on the HP 54616B. Through the use of integrated hardware, 1-ns peak detection is achieved over all time base ranges. Following the front-end hardware is a proprietary memory system that is configured to provide 5000-point acquisition records for each channel.

These features permit a high sustained sample rate over a wide number of time base ranges. Engaging the hardware peak detection capability is an effective defense against the possibility of missing fast transient input signals.

Other Capabilities

An integrated internal calibration port enhances the ease of use and reduces the cost of ownership of these products. The CRT, the front-panel keyboard, the internal system memory, and other hardware subsystems are easily tested without the need for additional test equipment. Both vertical and horizontal representations of the acquired data are calibrated for variations in hardware components and the thermal environment.

Additional measurements, enhanced functional capability, mask testing, FFTs, additional nonvolatile memory for setup and trace saving, and expanded I/O connectivity can be provided through the use of attachable option modules.

Software Block Diagram and Theory of Operation

The software environment can be thought of as being assembled from a number of *islands of control*. With the host MC68000 acting as a central dispatcher, tasks are delivered to any of several subcontrollers. Each subcontroller retains independent state information regarding the underlying hardware. In the HP 54615B/16B products, there are three such islands of control.

The first is the MC68000 itself. In addition to running the operating system, the host processor is responsible for dispatching messages related to main and delayed time base sweeps for performing data abstractions on acquired data. In particular, automated measurement calculations on acquired data, mask testing, FFT computation, and function evaluations are performed by the host.

When the state of the host instrument dictates that messages be dispatched to neighboring islands, two methods are employed. The first is a time-sliced access method in which access to a particular island is guaranteed during a given portion of the overall instrument cycle time. During this time, information can be exchanged and island state variables affected. An example of this type of dispatch is the video display processor. When vectors are enabled or disabled, the video display processor is informed of this change of state. In turn, the video display processor effects the necessary changes in the hardware under its control in an autonomous manner.

The second method of message dispatching is based upon a traditional message/interrupt scheme. The host places a message in shared memory, which by protocol is guaranteed not to be corrupted by other islands, and then sends a hardware interrupt to the neighboring island controller. Detection of the message is asynchronous; the host will not initiate subsequent message/interrupt cycles until a handshake from the first is recognized. The DSP is an island that operates on this premise (Fig. 3). For example, when the 1-ns peak detection capability of the instrument is enabled, several message/interrupt packets are built to make the necessary changes to the DSP's internal state variables and tables. Acquisitions are then restarted in the new mode.

Because the host island is running a multiprocess operating system, it can be thought of as several smaller island processes. In addition to the one responsible for communicating with the DSP island, others manage the front-panel keyboard and remote control interfaces. For example, when user interacton is detected by the host, reading of the keyboard state is performed by means of memory mapped hardware located within the address space of the host system RAM.

Each island has specific responsibility for its respective underlying hardware subsystem. Software driver/hardware pairs exist within each island and are unique. For example, the DSP island contains a specific driver to control and operate the integrated time base generator hardware.

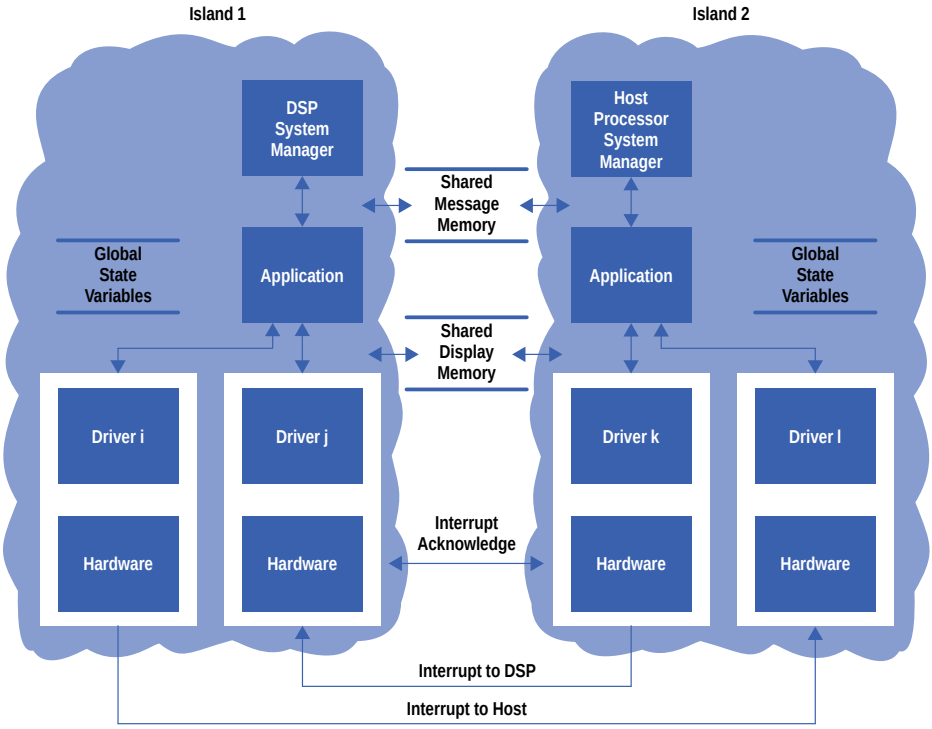

Fig. 3. *Islands of control. Each island consists of a processor with unique applications, hardware, and drivers.*

Code Reuse

An important part of the effectiveness of this development was the the application of software code reuse. An expanded and enhanced printer library was exploited without change to accelerate the development. Taking advantage of software that is ripe for reuse has improved the reliability of this family of instrument products. Consistent with the goal of providing familiar functions throughout the product family, this effort continues.

Summary

Through the application of task-specific hardware and software subsystems, the analog feel of the user interface has been retained while extending the envelope of performance. The notion of islands of control with autonomous operation effectively permits improvements in responsiveness, while an emphasis on software code reuse improves maintainability and the leveraging of existing technology.

Acknowledgments

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Reference

1. *Hewlett-Packard Journal*, Vol. 43, no. 1, February 1992, pp. 6-59.

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