A Cost-Effective Architecture for a 500-MHz Counter for Glitch Trigger

The HP 54645A and 54645D oscilloscopes can trigger on pulses qualified by their width, a feature known as *glitch trigger.* The time qualification is done with a 500-MHz, 37-bit counter that provides 2-ns timing resolution over an 8-ns-to-100-s range. Operation at 500 MHz (a 2-ns period) is too fast for CMOS logic, but the 37-bit counter is too large for economical integration in bipolar logic. The clock for the counter must be asynchronous with the analog-to-digital sampling clock so that the time at which a trigger is generated is in no way related to the times of the samples. Otherwise, in random repetitive acquisition mode (also known as equivalent time sampling), the samples would not be randomly distributed with respect to the input signal and the oscilloscope waveform would contain missing segments.

The block diagram in Fig. 1 shows how these requirements and constraints were satisfied. The least expensive way to obtain the 500-MHz glitch trigger clock was with a commercial single-chip phase-locked loop locked to the 50-MHz reference clock. The phase-locked loop synthesizes a 250-MHz clock, which is doubled to 500 MHz in the bipolar gate array. Phase locking to the reference clock guarantees that the glitch trigger clock is precisely synchronized with the reference. Since the sample clock is also locked to the reference but phase dithered, the glitch and sample clocks have random phase with respect to each other, preventing missing segments in the waveform.

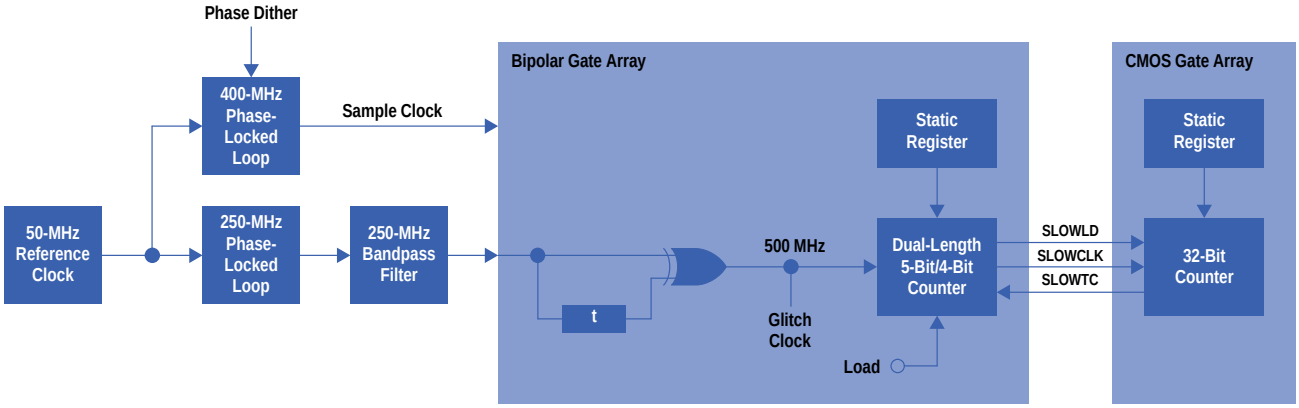

Fig. 1. *Block diagram of the 500-MHz, 37-bit counter.*

The clock doubler generates an active 500-MHz edge on both the rising and falling edges of the 250-MHz clock. The symmetry of the 250-MHz clock affects the uniformity of the periods of the 500-MHz clock. The jitter of the 250-MHz clock causes period jitter in the 500-MHz clock. The delay element τ, formed with gate delays, determines the duty cycle of the 500-MHz clock. The asymmetry and period jitter errors of the 500-MHz clock must both be less than 100 ps to preserve timing margins in the 500-MHz counter. The phase-locked loop IC alone cannot meet these requirements, so a bandpass filter is introduced that removes spurious components in the clock spectrum, improving the symmetry and reducing the jitter from 111 ps to 44 ps.[1]

For reasons of both power and cost, the 37-bit counter is too large to implement entirely in the bipolar gate array. By including only a few of the low-order, high-speed bits in the bipolar IC and the remaining bits in a CMOS gate array we are able to build a very economical, low-power 500-MHz counter. The bipolar portion is called the fast counter and the CMOS portion the slow counter. Together these two operate as a single 37-bit synchronous counter.

The design of the counter is complicated because the CMOS IC must never see pulses narrower than about 10 ns and responds relatively slowly with the terminal count (TC) signal. To overcome these limitations the fast counter operates in either of two modes: as a five-bit counter or as a four-bit counter. For counts from 1 to 31 the fast counter performs all the counting. For counts of 32 and up, the bipolar counter is always loaded with a count between 15 and 31. Since the fast counter is loaded with a minimum count of 15, the slow counter always has at least 15×2 ns or 30 ns to reload itself before it is called upon to begin counting. The fast counter counts down in five-bit mode to zero and then generates a SLOWCLK signal, triggering a count in the slow counter. It then switches to 4-bit mode and counts down, generating a SLOWCLK signal every 15 clocks. Thus, the slow CMOS counter is clocked at only 500 MHz/15 or 33 MHz and has 30 ns in which to generate SLOWTC. These requirements are easily met with modern CMOS gate array technology.

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Reference

1. S.D. Roach, "Achieving Ultra-Low Clock Jitter with Commercial High-Speed Clock Generators," *Proceedings of Design Supercon '96*, High-Performance System Design Conference, Santa Clara, California, 1996.

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