

Design of an Enhanced Vector Network Analyzer

A liquid crystal display (LCD) reduces size and weight and has a larger viewing area. TRL (Thru-Reflect-Line) calibration allows measurement of components that do not have coaxial connectors. New software algorithms achieve faster acquisition and frequency tuning of the synthesized source to give faster updates of the measurement data.

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The development of a new measurement instrument always involves technical challenges. This is also true for the enhancement of an existing family of instruments with the added challenges of getting the enhancements to market in exactly the right form and in a timely manner.

The measurement instrument called a *vector network analyzer* (see Fig. 1) is the integration of a tunable source, a multichannel receiver, and a test set for signal routing and separation, all under the control of an embedded CPU. The block diagram in Fig. 2 shows the interconnection of these components, which for the family of instruments described here are all integrated into one package.



Fig. 1. HP 8720D vector network analyzer.

The purpose of a vector network analyzer is to measure the magnitude and phase of the reflection and transmission characteristics of a microwave component (historically called a microwave network) as functions of frequency. The component is inserted between the test ports, the test signal is rapidly tuned over a span of frequency, and portions of this signal are reflected from and transmitted through the component. These reflected and transmitted signals are ratioed with a portion of the test signal that has been tapped off into the reference channel to display the component's reflection and transmission characteristics as functions of frequency. This information is needed by designers to know if their components will work properly when inserted into a microwave system.

The accuracy of the measurement, which depends on separating the component's characteristics from the characteristics of the instrument, is greatly improved by the ratioing process. The accuracy is further enhanced by a calibration process that measures known standards (calibration components) to characterize and mathematically remove the remaining systematic errors in the instrument.

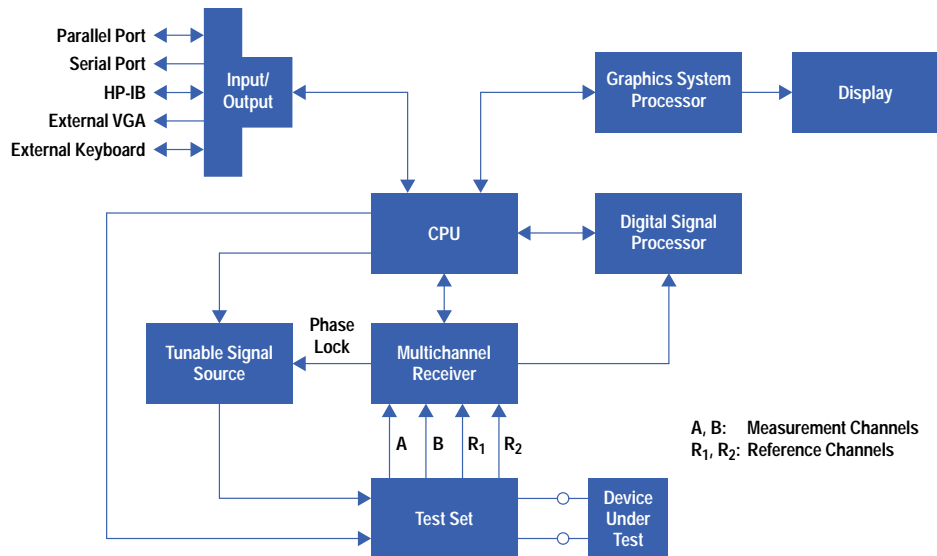


Fig. 2. HP 8720D vector network analyzer block diagram. Two reference receivers, R_1 and R_2 , distinguish the Option 400 model. R_2 is always internal; only R_1 appears (as R) on the front panel.

The components that are measured with a vector network analyzer are used in a wide variety of commercial and military products: cellular phones, broadcast and cable TV, long-distance telephone transmission, satellite communications, microwave ovens, airplane radar, missile guidance, and so on. Each of these applications uses dozens of components that are developed and produced with the aid of a vector network analyzer. Thus, the accuracy and measurement speed of the vector network analyzer will have an impact on the performance and cost of these products.

The family of HP vector network analyzers known as the HP 8720 family is composed of three members that differ in the frequency range over which they can make their measurements. The HP 8719D, 8720D, and 8722D cover the frequency ranges from 50 MHz to 13.5 GHz, 50 MHz to 20 GHz, and 50 MHz to 40 GHz respectively. The family made its first appearance early in 1988 with the introduction of the HP 8720A and has evolved over the years to the introduction of the D models in May 1996.

The evolution of the HP 8720 family from the A models to the C models was to improve the instruments' hardware performance. The recent evolution from the C to the D models was to respond quickly and directly to a change in users' needs. More and more the instrument was being used in a production measurement role as opposed to the previous R&D role. This change brought with it a need for more measurement speed and expanded I/O capability to allow easier and better integration into a larger production test system. Also, the industry trend of higher levels of integration of components made it necessary to measure components that do not have coaxial connectors—for example, a probe station measuring amplifier chips on an IC wafer. We wanted to respond with something that not only met the new measurement needs, but also had a new look: a state-of-the-art display technology and a smaller, lighter package.

The list of improvements we could have made was long, but we could only choose a few because we wanted to respond quickly. This required careful selection and sorting of the customer inputs that come to us directly or through our field sales force. One difficulty in sorting these inputs was the fact that one fundamental need can manifest itself in several different ways—for example, after thorough investigation, an issue of instrument calibration turned into an issue of measurement speed. Another difficulty was sorting the unique but strongly stated needs from the broadbased but quietly stated needs.

Once the sorting and prioritizing were done, we focused on the most important changes that also allowed us the most leverage from existing designs. When this was done, we proceeded to improve the HP 8720 family with these design changes:

- A liquid crystal display (LCD) gives size and weight reductions plus a larger viewing area. These are important features in a production environment.
- In the HP 8720D Option 400 models, hardware and software additions implement a calibration technique called TRL (Thru-Reflect-Line), which uses four receivers: two reference and two measurement. This allows accurate measurement of components that do not have coaxial connectors. Implementing TRL required some careful multiplexing of the receivers' outputs because the instrument is limited to three data channels.
- New software algorithms achieve faster acquisition and frequency tuning of the synthesized source to give faster updates of the measurement data.

Liquid Crystal Display Electrical Design

There were many advantages to be gained by converting the instrument's display from the traditional color CRT to a color LCD, as can be seen in Table I. In particular, note the significant decrease in volume, weight, and power consumption and the increase in viewing area. However, as beneficial as this conversion is, implementing it in a short time presented some significant challenges.

Table I
LCD versus CRT Display Characteristics

	7.5-in CRT	8.4-in LCD	LCD Advantage
Volume	9745 cm ³	240 cm ³	-97.5%
Weight	5 kg	0.33 kg	-93.4%
Power Consumption	35W	3W	-91.4%
Viewing Area	170.4 cm ²	221.5 cm ²	+30.0%
Horizontal Size	15.6 cm	17.1 cm	
Vertical Size	10.9 cm	12.96 cm	
Aspect Ratio	0.7	0.75	
Pixel Frequency	35.9 MHz	25 MHz	
Horizontal Frequency	25.46 kHz	31.41 kHz	
Vertical Frequency	59.9 Hz	59.8 Hz	
Vertical Resolution	400	480	
Horizontal Resolution	1024	640	

Originally, the display interface was designed to drive a monochromatic, digital, vector CRT display with a state machine controlling stroke and font generators. The state machine executed four basic commands (set condition, plot, graph, character) which were stored in a display list. When the monochrome display was later replaced by a color raster display, the same interface was used, making the transition to color more or less a drop-in replacement (with necessary changes to control the color attributes of lines and text).

With the color raster CRT, the display interface was built around a graphics system processor, which emulates the state machine's stroke and font generators. Supporting blocks for the graphics system processor include DRAM to store the graphics system processor code and display list, VRAM to store the pixel data for the raster display frame and fonts, and a color palette, which uses the pixel data to address a color lookup table which then drives a triple DAC to generate the analog RGB outputs to drive the CRT. The block diagram for this is shown in Fig. 3. The pixel data is 4 bits, which allows 16 simultaneous colors to be displayed. Lookup table registers have 12 bits, which allows selecting one of 4096 colors.

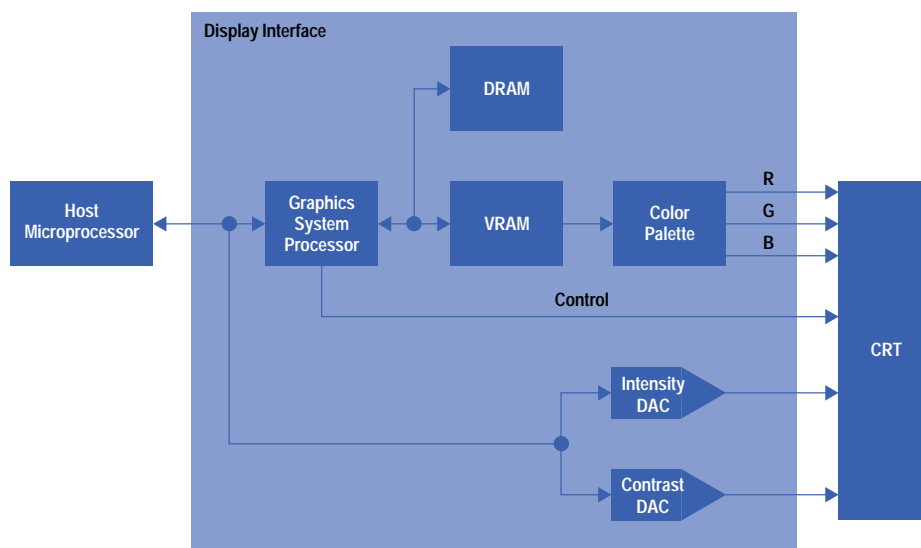


Fig. 3. CRT graphics system.

Changing from the color CRT to a color LCD in a short time did not allow creation of a totally new display interface. The focus was to address each of the differences listed in Table I. This resulted in changes of display resolution, timing, aspect ratio, data format, power requirements, and test patterns. The resolution change required changing the x-axis and y-axis scaling in the graphics system processor plot and graph routines and the size of the bitmapped fonts. The display timing change required modifying the values of the graphics system processor timing register value. The change in aspect ratio required changing the host code that generates circles to maintain their roundness. This change affected the aspect ratio of the printer output, which required a modification in the graphics system processor code controlling the horizontal scale factor. The data format change required changing from the CRT's analog RGB data to digital data. The color palette did not provide access to the digital data, so it was replaced with a static RAM for the color lookup table and a triple video DAC, whose output is used for driving an external VGA monitor, as shown in Fig. 4. The power supply had to be changed to the 3.3Vdc required to drive the display, but more important, this voltage had to be withheld from the display until the video synchronization signals were present or the liquid crystal structure would be damaged. The test patterns were changed to allow for testing some of the unique characteristics of an LCD: a black screen checks for pixels that may be stuck on, primary color bars help evaluate the viewing angle, and 16 color bars help evaluate each of the LCD's color bits for troubleshooting the digital interface.

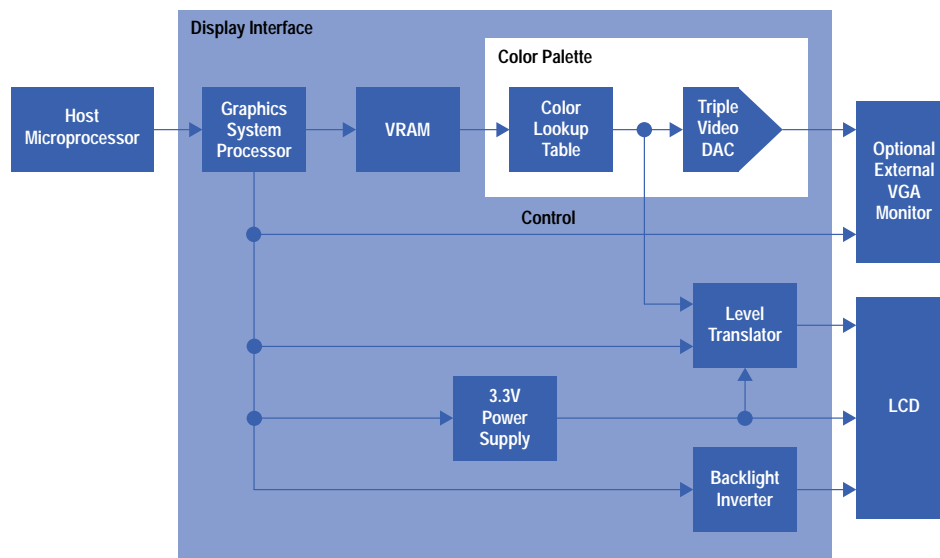


Fig. 4. LCD graphics system.

The LCD, which measures 8.4 inches across the diagonal of the active viewing area, was originally designed for use in a laptop computer. Using it in an instrument required several modifications to the display's viewing characteristics to improve general brightness and grayscale contrast reversal (light areas turn dark and dark areas turn light) over a wide viewing angle.

The laptop application optimized its brightness and contrast for a relatively narrow viewing angle (approximately ± 20 degrees off the perpendicular in either the horizontal or the vertical direction). Instrument application requires a wider angle, typically ± 45 degrees. An instrument display needs to have this wider viewing angle to be free of grayscale contrast reversal. The solution to these problems was to modify the light polarizing and diffusing films that coat the display, and to avoid using colors that are not fully saturated. This restriction on the level of color saturation means that to achieve maximum viewing angle, an LCD that is capable of 4096 colors is limited to a total of eight. This certainly limits the color flexibility, but it is enough for our four-trace display.

One advantage of converting from a CRT to an LCD is that LCDs don't have convergence, focus, geometric distortion, and color purity concerns. This produces a visual image that is sharper and more consistent in color across the entire screen.

Liquid Crystal Display Mechanical Design

The design of the front panel for the HP 8720D vector network analyzer incorporates many features that solve problems associated with the display, including aligning the display with the panel, preventing leakage of electromagnetic fields from the display area, ease of assembly, and space saving.

In past instruments with a CRT display, the display and front panel inherently had poor alignment with each other because of the lack of a common mechanical reference. The LCD design, shown in Fig. 5, solves this problem by integrating into the front panel the display bezel and mounting posts. This allows self-alignment of the display to the bezel. The mounting posts also control the spacing between the LCD and the panel to capture the gaskets and the protective antireflection glass properly.

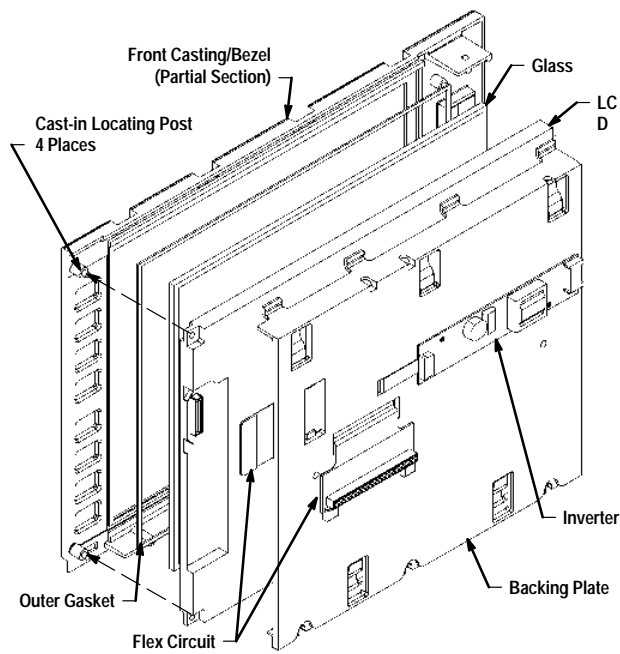


Fig. 5. The LCD bezel and mounting posts are integrated into the instrument front panel.

Electromagnetic interference (EMI) from the electrical circuitry in the LCD is a problem because it cannot be shielded by the instrument's sheet-metal enclosure. To solve this, a thin, transparent layer of metal was added to the surface of the glass, and this layer is electrically connected to the metallic front panel by conductive silver strips along all the edges of the glass. To ensure low-resistance, reliable contact, special spring clips attached to the metalized edges of the glass make pressure contact to the front-panel casting. In addition to the electrical connection, the clips also locate and hold the glass in the panel. The net effect is to produce a continuous metal shield over the display without noticeably affecting the display's viewability. To provide additional shielding for the LCD, a special conductive gasket was added to the LCD's metal frame to connect this frame to the edge metallization on the glass. This gasket also hides the LCD's metal frame, which would have been visible in the wide bezel opening necessary to yield the maximum viewing angle of the display's active area (see Fig. 6).

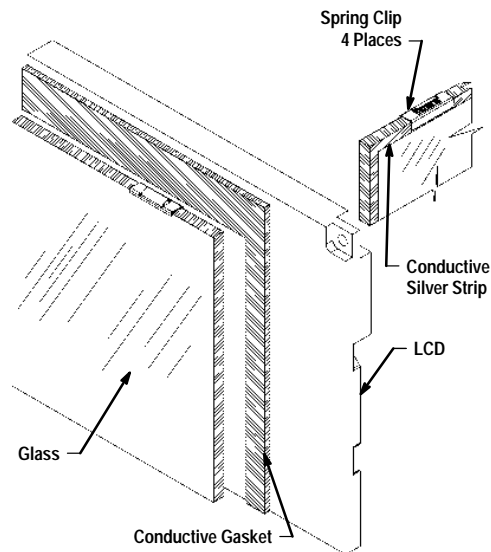


Fig. 6. To reduce electromagnetic interference, the display has a transparent metal layer on its glass surface, a conductive gasket on its frame, and spring clips and silver strips to connect the glass to the frame.

The key to the ease of assembly is the LCD backing plate, which has several functions. It holds the LCD to the bezel with five pressure tabs, it provides mounting for the circuit board that drives the display's backlight, it captures the flex circuit that connects the LCD and backlight driver to the graphics processor, and it allows access to the backlight for easy replacement. The assembly of the LCD to the front panel is a simple layering of parts all from one side, and the layered parts are all held in

place by only three screws. This gives a rugged and very compact arrangement. The full depth of the assembly from the front bezel to the back of the mounting plate is less than 21 mm (compared to 317 mm for a standard CRT). This drastic reduction in the depth of the display allowed a 20% volume reduction over previous models and reduced the depth of the instrument, which is very important because it gives the user more working room in front of the instrument.

Three-Receiver Analyzer

To understand the consequences of adding a fourth receiver, it is helpful to review the characteristics of the standard three-receiver version of the network analyzer. The receiver of the network analyzer is synthesized, and the source is phase-locked to the receiver through the reference receiver path, as shown in Fig. 7. In the standard instrument, the reference receiver path is obtained by splitting some of the signal from the main signal path. This same splitting point is used for the automatic level control (ALC) detection point. The main signal path continues to the test set transfer switch, which directs the signal through one of the test port couplers for forward or reverse signal path measurements. The isolation of the switch in the off path creates a cross-talk term, limiting the dynamic range of the transmission measurements.

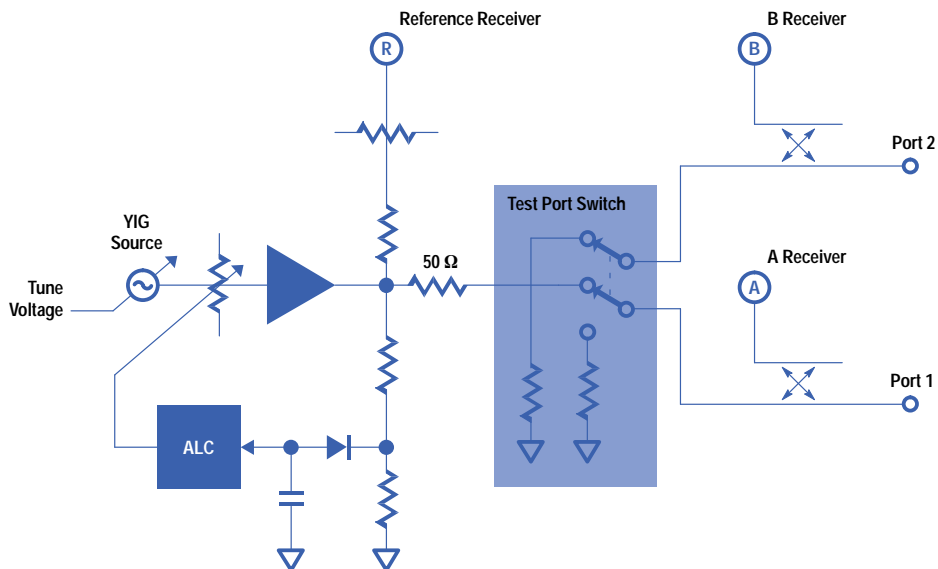


Fig. 7. Test set for a vector network analyzer with three receiver channels.

The effects of the system configuration on measurements can be understood in the context of system specifications as seen from the test ports: power source match, ratio source match, load match, test port output power, and test port power flatness.

A key specification for network analyzers is source match, which is a measure of how close the test port impedance is to an ideal 50-ohm real source impedance. If the driving point impedance of a test port is not equal to the ideal reference impedance, measurement errors such as ripples on transmission measurements will become evident. In fact, there are two different source match terms: actual source match, which might be referred to as the *power source match*, and the source match in a ratio measurement, which is referred to as *ratio source match*. Good power source match is important for test port power accuracy, while good ratio source match contributes to accurate measurement of s-parameters. The ratio source match is created by taking the ratio of a test signal to the reference signal. This provides an improvement over the power source match.¹

For power source match, a sample of the of the source signal is routed to a detector, and the level of the source is controlled to keep the detected signal constant. This has the effect of making the split point a virtual voltage source, thus having a zero impedance. The series 50-ohm impedance in the main path now sets the power source match. The power source match in this case is still not exactly 50 ohms because some signal that does not come from the virtual source node may couple to the detector as a result of high-frequency coupling from the main arm output to the detected output. Also, any physical resistor will have some reactive component, such as series inductance or shunt capacitance. Although minute, these small parasitic elements have substantial effects at high microwave frequencies. For example, 0.1 pF of shunt capacitance has a reactance of 50 ohms at 30 GHz.

Ratio source match is very similar to power source match, in that the sampling of the reference signal makes the node of the sampling point appear to be a virtual source, and the series resistance in the main arm sets the ratio source match. As shown in Fig. 7, the same node is used for both power leveling (ALC) and ratio splitting, and the same series resistor is used for setting both kinds of source match. Because of differing parasitic coupling factors from the main arm to the detector path

and from the main arm to the ratio path, the power source match and the ratio source match will not be identical, especially at high frequencies. For most measurements, the main concern is for good ratio source match.

The *load match* of a network analyzer is the term used for the impedance of the test port that is not the active source. It is easy to see from the block diagram that there is a different path for the load impedance in this state. Therefore, the source match and the load match of a particular port will not be the same.

The insertion loss of the switch reduces the test port signal. The total loss of the switch limits the maximum power available, and the frequency response, or flatness, of the switch determines the test port power flatness. The maximum test port power is determined mainly by the switch loss, but also by the maximum power available from the source amplifier, the loss in the reference and detection splitters, and the loss in the test port coupler. Because the test port switch is positioned between the reference channel and the test channel, any switch repeatability errors, or drift, will be errors in the measurements. Power flatness is determined by how well the detector sensitivity remains constant with frequency. However, because the loss from the power leveling node to the front panel test port increases with frequency, the detector path is designed so that the source power increases with frequency, thus compensating for the loss to the test port.

Incorporating a Fourth Receiver

For the four-receiver version (Option 400), the test port switch needs to come before the reference channel power splitter, thereby creating two reference signals and two test port signals, one for the forward direction and another for the reverse direction (Fig. 8). In this way, the switch repeatability error is “ratioed out” and does not affect measurement accuracy. Current designs use equal-resistance power splitters with a 50-ohm resistor on each leg to obtain the reference signal. The power splitters are integrated into the test port switch. The switch incorporates a shunt p-i-n diode at the splitter node that is forward-biased in the off state such that the node has a low impedance to ground and the off state main-arm impedance is 50 ohms. The reference receiver requires a much smaller signal than the test port, so additional external attenuators are usually added. The loss to the main arm for this configuration is nominally 6 dB. Thus, with no other changes, the maximum test port power and the system dynamic range would need to be degraded by 6 dB. To reduce the power loss in the four-receiver configuration, an unequal splitter was designed to tap off less power for the reference receiver. This decreases the loss through the main arm by about 2 dB, though it does make the power source match a bit worse. The ratio source match in the ratio mode depends upon the design of the splitter circuit (see *Subarticle 12a*).

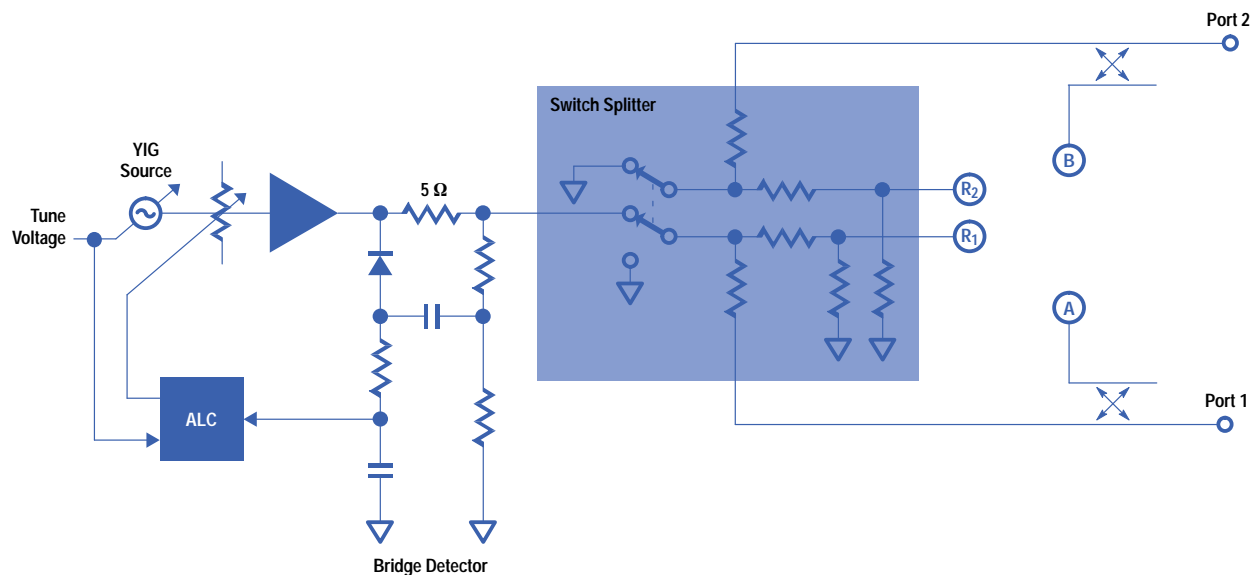


Fig. 8. Test set for a vector network analyzer with four receiver channels.

In the three-receiver version of the network analyzer, the splitter for power level detection and the reference receiver shared the same split node and the same series 50-ohm resistor. In the four-receiver version, the power level detection arm is not part of the splitter, so the power loss from this path can be recovered, allowing more power to reach the test port. An alternative method for generating a detected signal was implemented that uses a custom HP GaAs IC.

This chip has an unequal-resistor bridge with a built-in detector diode, which provides the necessary signal to the ALC circuit and has less than 2 dB of loss. The splitter-detector used in the three-receiver version had about 6 dB of loss, so an additional 4 dB of power is recovered by this modification. The detector circuitry is actually integrated into the source amplifier microcircuit, so a new version of this module was introduced with the bridge detector circuit and without the reference RF output. This change, along with the unequal power split in the switch-splitter circuit, makes up for the loss and means that no degradation is needed in the maximum output power or dynamic range.

The integrated bridge detector has a very flat frequency response, so the power out of the amplifier is quite flat. This would normally seem like a good thing, but there is a lot of power loss slope in the switch-splitter and other components on the way to the test port. The detector sensitivity of the IC cannot be sloped, so the power flatness could become quite bad, something like 8 dB of variation from maximum to minimum power at the test port. Because of this, the design of the ALC circuit needed to be modified to accommodate this slope.

The short duration of the project required that the ALC changes not result in any instrument firmware changes to improve the power flatness. This requirement was met by sampling a portion of the tune voltage of the main oscillator, which is linear with frequency, and using it to modify the reference for the ALC level. Some diode shaping and adjustable gain and offset allow a range of adjustments that provide less than 1.5 dB of power variation over the 20-GHz span of the network analyzer.

For the 40-GHz version of the network analyzer, the equal splitter was retained because the greater loss at 40 GHz requires a larger signal to the reference receiver. The 40-GHz source amplifier was modified with the bridge detector circuit to increase the available power by 4 dB, and the final power amplifier chip, again a custom HP GaAs IC, was changed to a newer high-power version that gives 2 dBm more output power. Thus, the output power specification and dynamic range of the 40-GHz analyzer are not degraded for the four-receiver version.

Thru-Reflect-Line Error Correction

One of the classic difficulties in making s-parameter measurements on a device is that a user would like the measurement environment to be as nearly identical as possible to the environment in which the device will ultimately be used. The difficulty is often compounded by a lack of calibration standards for a particular environment, or by the limited ability of the user to create calibration standards that are predictable and reliable for that environment.

The Thru-Reflect-Line (TRL) technique^{2,3} has gathered momentum over the past decade because it only requires a known characteristic impedance for a short length of transmission line (the "Line" part of TRL). Furthermore, since an infinitely long transmission line can be represented by terminations or loads of a particular characteristic impedance, the technique can be extended to an entire family of TRL techniques, including Thru-Reflect-Match, Thru-Reflect-Attenuator, Line-Reflect-Line, and so on. Like the HP 8510 network analyzer, the HP 8720D Option 400 instruments incorporate four samplers and a switch-splitter arrangement so that self-calibration using a TRL algorithm can be performed for high-accuracy s-parameter measurements.⁴

A key to the self-calibration technique is the source and load match error removal, also called removal of switching errors. This is accomplished in both the HP 8510 and the HP 8720D Option 400 using the algorithm described by Rytting⁴ (see Fig. 9).

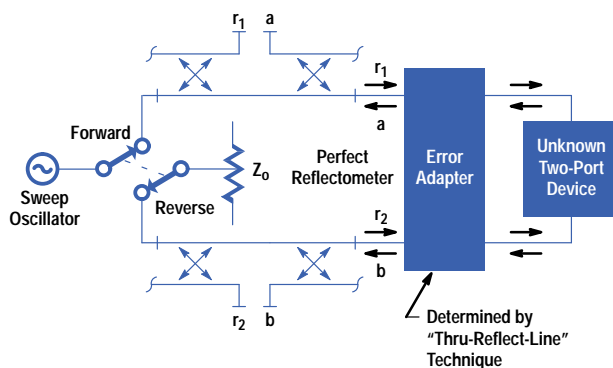


Fig. 9. Forward and reverse paths and signals measured in the TRL calibration technique.

Rytting's paper gives equations relating the measured values of the device's s-parameters to the actual values for the generalized condition in which the source and load impedances are not equal to an ideal 50-ohm impedance. Rewriting these equations using notation unique to the HP 8720D family gives:

$$s_{11m} = [(a/r_1) - (a'/r_2')(r_2/r_1)]/d \quad (1)$$

$$s_{21m} = [(b/r_1) - (b'/r_2')(r_2/r_1)]/d \quad (2)$$

$$s_{12m} = [(a'/r_2') - (a/r_1)(r_1'/r_2')]/d \quad (3)$$

$$s_{22m} = [(b'/r_2') - (b/r_1)(r_1'/r_2')]/d \quad (4)$$

$$\text{where } d = 1 - (r_2/r_1)(r_1'/r_2') \quad (5)$$

and the following are complex numbers: s_{knm} is the measured value of s-parameter s_{kn} , a is the A sampler's measurement, b is the B sampler's measurement, r_1 is the R₁ sampler's measurement, and r_2 is the R₂ sampler's measurement.

The prime sign (') refers to the reverse path as opposed to the forward path of the test set. Ideally, when $r_2 = 0$ and $r_1' = 0$, the switch path has perfect Z_0 impedance, $d = 1$, and the s-parameters reduce to the single-term ratios.

In the HP 8720D family, the intermediate frequency (IF) paths for measuring the reference signals r_1 and r_2 are implemented by an IF multiplexing board described later. Because of the architecture of this board, the magnitudes and phase shifts through the various paths are not perfectly balanced. What is important, however, is that all of the ratios are made relative to the same reference IF path.

In the HP 8720D, the ratio a/r_1 is measured using the A IF path and the R IF path, b'/r_2' by the B and R IF paths, and so on. The ratios r_2/r_1 and r_1'/r_2' are measured using only the A and B IF paths.

To establish some notation for this, we will use @ and capital letters to refer to the IF paths used. For example, $a@A$ is the measurement of a using the A IF path. Thus, the five equations above become:

$$s_{11m} = [(a@A/r_1@R) - (a'@A/r_2'@R)(r_2@B/r_1@A)]/d \quad (6)$$

$$s_{21m} = [(b@B/r_1@R) - (b'@B/r_2'@R)(r_2@B/r_1@A)]/d \quad (7)$$

$$s_{12m} = [(a'@A/r_2'@R) - (a@A/r_1@R)(r_1'@A/r_2'@B)]/d \quad (8)$$

$$s_{22m} = [(b'@B/r_2'@R) - (b@B/r_1@R)(r_1'@A/r_2'@B)]/d \quad (9)$$

$$d = 1 - (r_2@B/r_1@A)(r_1'@A/r_2'@B). \quad (10)$$

If you look at these equations carefully, you will note that the measurements of the reference ratios r_2/r_1 and r_1'/r_2' are not made relative to the R IF path, but the other measurements are. Some means for correcting for this difference is needed. The HP 8720D allows measurement of r_2 using both the R and B paths, and measurement of r_1 by both R and A (see Fig. 10). The correction for IF path differences can be reconciled by:

$$(r_2@B/r_1@A)(r_2@R/r_2@B)(r_1@A/r_1@R) = r_2@R/r_1@R \quad (11)$$

$$(r_1'@A/r_2'@B)(r_1'@R/r_1'@A)(r_2'@B/r_2'@R) = r_1'@R/r_2'@R \quad (12)$$

Since r_2 is the same signal to both the R and B paths, the measurement ratios for forward and reverse are equal:

$$r_2@B/r_2@R = r_2'@B/r_2'@R \quad (13)$$

This ratio can be symbolized as $r_2\text{refcomp}$ for r_2 reference compensation.

Likewise, for r_1 :

$$r_1@A/r_1@R = r_1'@A/r_1'@R \quad (14)$$

This can be called $r_1\text{refcomp}$.

Rewriting equations 11 and 12, the reference ratios are now compensated for the IF path differences:

$$(r_2@B/r_1@A)(r_1\text{refcomp})/(r_2\text{refcomp}) = r_2@R/r_1@R \quad (15)$$

$$(r_1'@A/r_2'@B)(r_2\text{refcomp})/(r_1\text{refcomp}) = r_1'@R/r_2'@R \quad (16)$$

The original equations 1 through 5 can now be used, as long as the reference ratios are compensated as shown in equations 15 and 16.

10-MHz IF Multiplexing Board

The HP 8720 family of network analyzers was originally designed with three receivers based on the HP 8753 IF processing hardware. The first converter, however, was leveraged from the HP 8510 network analyzer, which has four receivers. Thus, there was a place in the first converter of the HP 8720 where a fourth receiver could be added easily, but there was no fourth channel in the IF processing hardware to connect to its output. Therefore, a four-channel-to-three-channel multiplexing circuit was added to the HP 8720D, between the four first-converter outputs and the three second converters (see Fig. 10). This circuit switches the 10-MHz IF signals so that all four channels can be measured and TRL calibration and error correction can be performed properly in the Option 400 models. In a standard three-channel instrument, this circuit does nothing (the switches are always left in the same positions).

At first glance, it would seem that only the R_1 and R_2 channels need to be switched, and the A and B channels could go straight through. This would allow measurement of all four channels; R_1 , A, and B in the forward sweep, and R_2 , A, and B in the reverse sweep. Unfortunately, this would not satisfy the requirements of TRL calibration. During the calibration process, it is required to measure the vector ratios R_1/R_2 and R_2/R_1 , so the additional switching of Fig. 10 is needed.

Design considerations for the IF multiplexer board were:

- Zero-dB insertion gain
- Harmonic distortion below -50 dBc at -10 dBm (full scale) for good measurement linearity
- Noise low enough to have little effect on the overall instrument noise floor

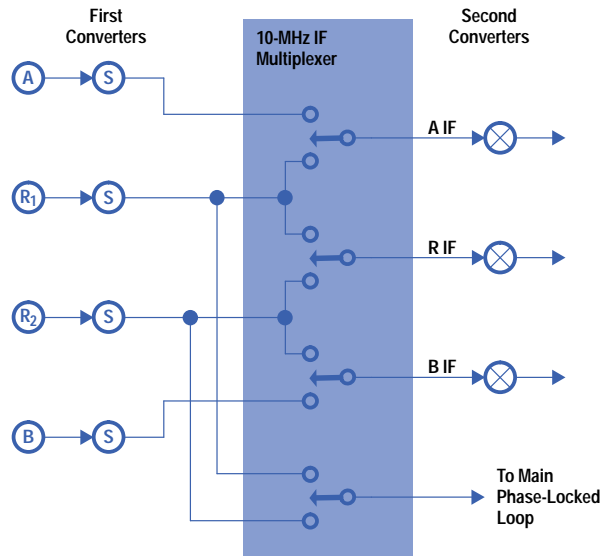


Fig. 10. Four-channel-to-three-channel IF switching.

- IF cross talk between channels less than -100 dB.

The circuit design uses a commercial low-noise IC video operational amplifier with a disable input pin. When disabled, the amplifier's output is a high impedance, so two of these ICs can be used as a SPDT switch by simply connecting their outputs together (Fig. 11). This design was preferred over a video switch because it made it easier to achieve high isolation and it has simple, high-impedance input, low-impedance output interfaces. Each amplifier has off-isolation of 60 to 70 dB, so two are cascaded together in each signal path to give greater than 120 dB.

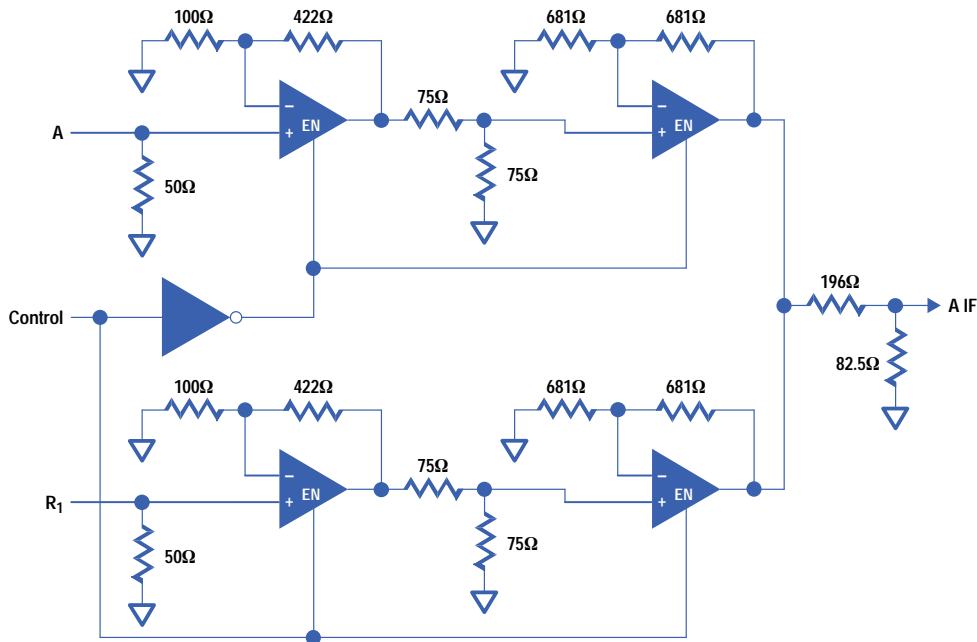


Fig. 11. 10-MHz IF switch.

The output noise power of the IF switch circuit is -123 dBm in a 3-kHz bandwidth, which is 113 dB below full scale. The overall instrument has typically 100 dB of dynamic range in a 3-kHz bandwidth, so the IF switch contribution is negligible. Second and third harmonics are typically -56 dBc at a -10 -dBm output level. Careful consideration of gains and attenuation in the switch circuit was needed to arrive at a good compromise between low noise and low distortion.

The most difficult design goal to meet was the switch off-isolation, which directly affects the instrument's cross-talk specification. Several iterations of the circuit design and board layout were required before the goal was finally met. Careful layout, use of multiple ground planes, and bypassing the power and switch control signals all played a part. But the most vexing problem by far was how the sampler output signals were brought onto the board. These four signals originally

entered the board from the instrument's motherboard through two pin-and-socket connectors, but the best performance that could be achieved with this arrangement was only 90 dB of isolation. It was extremely difficult to attenuate the radiation from the connector pins sufficiently. Eventually, the design team chose to bring the signals onto the board in flexible coax cables, which was deemed a better solution than trying to shield sections of the connectors with elaborate sheet-metal parts. The final design achieves less than -100 -dB cross talk between all channels, with typically -120 dB in the most important cross talk paths.

Source Frequency Control Techniques and Improvements

The main components of the HP 8720D network analyzer source are a microwave YIG oscillator, a sampler, a fractional-N synthesizer, a pulse generator, a main phase-locked loop circuit, and a YIG driver, as shown in Fig. 12. Fig. 13 shows the main phase-locked loop circuit.

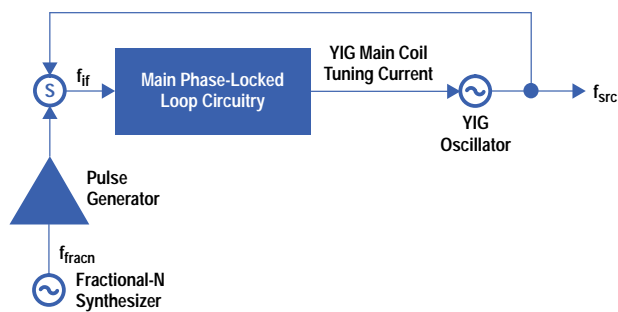


Fig. 12. Basic HP 8720D source block diagram.

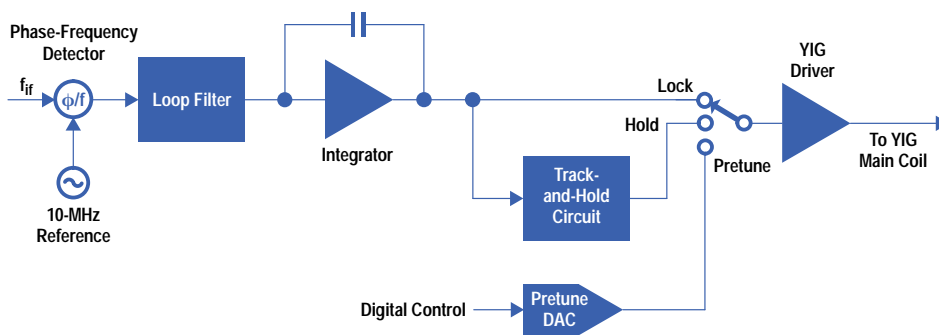


Fig. 13. HP 8720D main phase-locked loop block diagram.

The source uses a master-slave technique to control the YIG oscillator frequency based on harmonic multiples of the fractional-N synthesizer output. To set the output frequency, the YIG oscillator is first pretuned to the start frequency by setting a digital-to-analog converter (DAC) to a value that was previously derived during calibration. The output of the DAC is applied to the YIG oscillator driver circuit, establishing the YIG frequency setting. This simple tuning technique is only sufficient for a rough tuning of the oscillator. The output is neither precise enough nor stable enough for network analysis. The fractional-N synthesizer is tuned to a frequency that is determined by the formula:

$$f_{\text{fracn}} = \frac{f_{\text{src}} + f_{\text{if}}}{N},$$

where f_{fracn} is the fractional-N synthesizer frequency, f_{src} is the YIG oscillator frequency, f_{if} is the intermediate frequency (10 MHz), and N is the harmonic number.

For example, for a source frequency of 10 GHz, the fractional-N frequency would be:

$$f_{\text{fracn}} = \frac{10^{10} + 10^7}{58} = 172.586207 \text{ MHz.}$$

Once the YIG oscillator is pretuned and the fractional-N synthesizer frequency is set, the main phase-locked loop is closed and lock is acquired. The fractional-N frequency is then swept. Since the YIG oscillator is phase-locked to the fractional-N synthesizer, it also sweeps at a rate of N times the fractional-N sweep rate.

One of the limitations of the master-slave tuning technique is the YIG oscillator band crossings. The YIG oscillator can be tuned over a wide frequency range that includes several harmonic bands. The fractional-N synthesizer has a typical range

of 120 to 240 MHz. To sweep the YIG oscillator over its full range requires several band crossings, with relocking of the main phase-locked loop at each band crossing. To avoid pretuning at each band crossing, a sample-and-hold circuit is incorporated as part of the main phase-locked loop. In operation, the fractional-N synthesizer is swept over its range with the YIG oscillator following. Once the fractional-N synthesizer has reached its maximum frequency it must be reset and the YIG oscillator relocked to the next harmonic comb tooth. The YIG oscillator tuning voltage is held constant by the sample-and-hold circuit while the fractional-N synthesizer resets to the start of its range. After resetting, the loop is closed and lock is reestablished at the same frequency, but locked to a new harmonic comb tooth.⁵

The YIG oscillator frequency is determined by the amount of current flowing in its main tuning coil. The transfer function relating main coil current to output frequency is somewhat nonlinear. This makes pretuning the YIG oscillator difficult, since a pretune DAC value must be derived for each pretune frequency. Previous techniques used a multispline, piecewise linear curve fitted to the tuning curve of the oscillator. However, this complicated the pretune calibration process and there was the potential for errors resulting from inaccurate curve fitting.

Another difficulty is YIG oscillator hysteresis. A given amount of current applied to the main tuning coil will result in a different frequency output depending on the previous frequency. For example, if the oscillator had previously been set to 20 GHz, and then 1 mA were applied to the main coil, the resulting output frequency would be several MHz different from the frequency that would result if the previous frequency had been 3 GHz. This hysteresis effect results in inaccuracy when pretuning and potential false locking to the wrong harmonic comb tooth (N).

Improvements in Frequency Tuning and Control

Hysteresis effects of ferromagnetic material are well-understood and were used to advantage in early computers' core memory banks. Hysteresis effects can be minimized by setting the main tuning coil of the YIG oscillator to zero before pretuning. This in effect erases the oscillator's memory of the previous output frequency.

To avoid the nonlinearity of the YIG oscillator tuning curve the technique of pretuning close to the actual start frequency was eliminated. The new technique now pretunes to the YIG oscillator's minimum start frequency regardless of the actual desired start frequency, and the YIG is then swept up to the desired start frequency. This simplifies the pretune calibration process, since only one DAC number is necessary for pretuning. No curve fitting is required, since there is no longer a curve to fit. This pretuning works well with setting the main coil current to zero to minimize hysteresis because the YIG is then already at the minimum of its tuning range.

This tuning technique solves the two difficult problems of tuning curve nonlinearity and YIG tuning hysteresis. However, repeated narrowband sweeps at the upper end of the YIG oscillator's tuning range result in long cycle times, since the YIG must sweep from its minimum start frequency up to its upper frequency limit on each sweep. Setting the main tuning coil current to zero to minimize hysteresis also adds to cycle time, since the time constant of the large-inductance main tuning coil must be taken into consideration. The solution to correct for the long cycle time was to allow for sweeping the YIG oscillator backwards as well as forwards.

To illustrate the technique of sweeping backwards versus pretuning, take the example of a sweep from 19 to 20 GHz. Using the pretuning technique for all sweeps would result in crossing through four bands, with the subsequent delays resulting from four fractional-N frequency resets as well as the long delay required for resetting the main coil current to minimize hysteresis effects. Sweeping backward from 20 to 19 GHz requires no pretuning and no band crossings, and therefore results in a much faster cycle time for network analyzer measurements.

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