A 1.0625-Gbit/s Fibre Channel Chipset with Laser Driver

This chipset implements the Fibre Channel FC-0 physical layer specification at 1.0625 Gbits/s. The transmitter features 20:1 data multiplexing with a comma character generator and a clock synthesis phase-locked loop, and includes a laser driver and a fault monitor for safety. The receiver provides the functions of clock recovery, 1:20 data demultiplexing, comma character detection, and word alignment, and includes redundant loss-of-signal alarms for eye safety. A single-chip version with both transmitter and receiver integrated is designed for disk drive applications using the Fibre Channel arbitrated loop protocol.

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The information revolution has pushed the datacomm world to gigabit rates. Hewlett-Packard's G-Link chipset[1] (HDMP-1000) helped paved the way for low-cost gigabit technology. Since that debut, important standards such as Fibre Channel (FC) have incorporated gigabit rates in their documents. HP now offers a low-cost solution for Fibre Channel applications with the HDMP-1512 and HDMP-1514 transmitter and receiver chips, respectively.

The chipset implements the physical layer interface as defined in Fibre Channel specification FC-0.[2] Both the transmitter and the receiver use a "bang-bang" phase-locked loop technique similar to the G-Link chipset. Since the standard allows the use of either copper or fibre media, the transmitter has an integrated CD (compact disk) laser driver in addition to two 50-ohm cable drivers. Out of concern for eye safety, the standard requires the chipset to include certain monitors and controls to interface to an open fibre control (OFC) chip, so the chipset includes a laser fault monitor and loss-of-signal alarms.

The chipset's speed is selectable: either 1062.5 Mbits/s or 531.25 Mbits/s. To conserve power, the receiver chip implements a demultiplexing scheme that allows the use of lower-speed and lower-power cells to recover the parallel data. A special selectable "ping-pong" mode for the parallel TTL bus helps reduce switching noise on the supply lines. The upper and lower 10 bits are shifted by half a clock cycle relative to each other when ping-pong mode is active.

Both chips are implemented using a proprietary HP device array based on the HP25 bipolar process, a 25-GHz f_T process. The array concept not only allowed quick design cycle times but also enabled the fabrication of a single-chip transceiver that integrates both the transmitter and the receiver. The 10-bit transceiver design heavily leveraged the cells of the chipset. The transceiver is designed for disk drive applications using the Fibre Channel arbitrated loop (FC-AL) protocol.

System Configuration

The chipset is designed for use in a Fibre Channel optical module. Fig. 1a shows a typical system configuration. There are three ICs: the transmitter, the receiver, and the OFC (open fiber control) chip. The transmitter and receiver chips use a system frame clock (53.125 MHz) for transmission and to assist in meeting the data lock time. The transmitter uses an external p-n-p power device to handle the potentially large laser currents—as large as 130 mA. The OFC controller monitors link status lines from the transmitter and receiver chips to handle the safety protocol and the link startup sequence as described in the standard. A photograph of the assembled module is shown in Fig. 1b.

Transmitter Chip

The transmitter block diagram is shown in Fig. 2. It consists of three major blocks—the laser driver, the multiplexer, and the clock generator and phase-locked loop—plus a host of I/O and other supporting circuitry.

Fig. 1. *(a) Block diagram of the HP HGLM-1063 module. (b) HP HGLM-1063 module.*

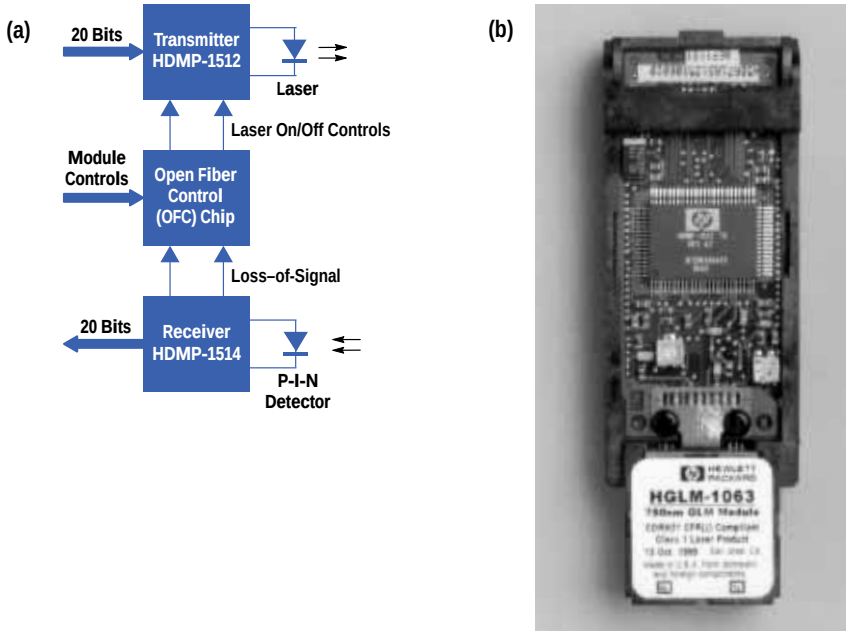
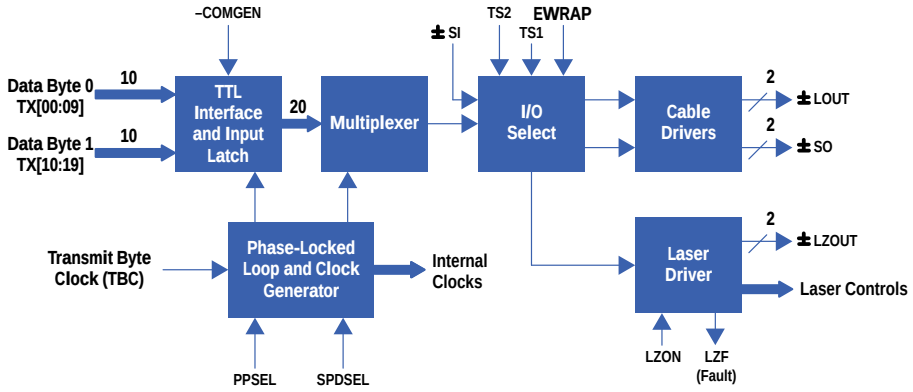


Fig. 2. *HDMP-1512 transmitter chip block diagram.*



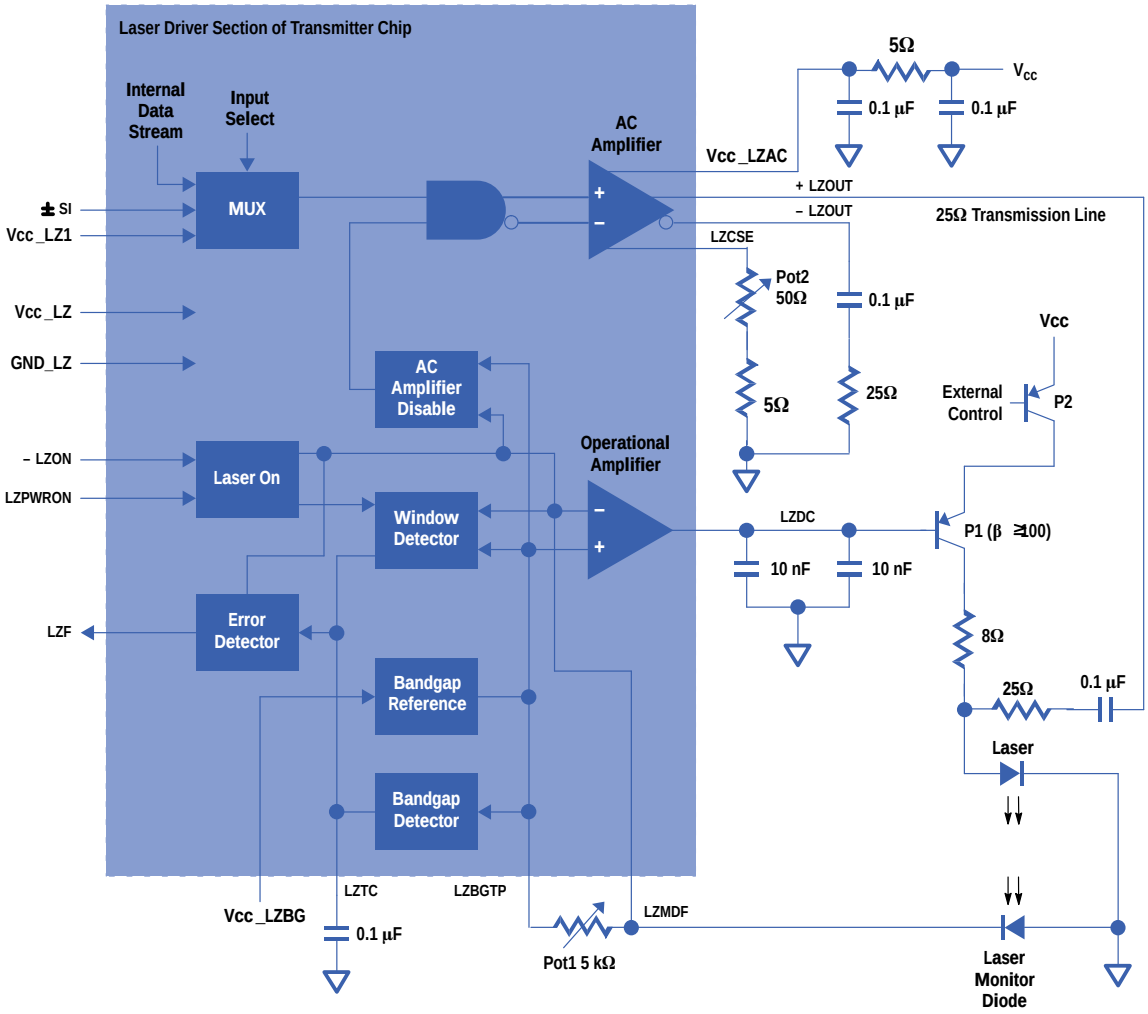
Laser Driver

The three distinct laser driver sections are the dc bias circuit, the ac driver, and the safety circuit, as shown in Fig. 3. The laser driver is designed for anode bias configurations and operating rates up to 1.0625 Gbits/s. The dc bias circuit can handle optical devices that require up to 130 mA of bias current and have V_{th} as large as 2.3V. For 780-nm CD lasers operating at –3-dBm optical power out, the typical dc bias current is 40 mA and the monitor diode current is 400 µA. The ac driver provides a minimum modulation of 25 mA peak-to-peak into the laser.

The dc bias circuit and the ac driver are decoupled for ease of adjustment. The decoupled scheme allows adjustment of either the average power or the modulation depth without affecting the other. Both of these settings are determined by resistive elements. The safety circuit monitors fault conditions to ensure that the laser optical output power will not be at unsafe levels.

DC Bias Circuit. Referring to Fig. 3, the dc bias of the laser is controlled by the operational amplifier feedback loop. The op amp's positive input is internally set to 1.85V. It is obtained through a voltage divider from the 2.42V bandgap reference node (output of the bandgap reference circuit[3]), LZBGTP. The negative input, LZMDF, is connected to a bias network controlled by the laser monitor diode. More current to the laser creates a larger monitor diode current, lowering the voltage on LZMDF. This results in a higher output voltage on LZDC. This decreases the V_{be} of transistor P1, thereby lowering the laser bias current until the monitor diode node LZMDF and the internal reference node are again equal. The monitor diode has a slow optical response (rise and fall times = 10 ns); thus, it acts as a low-pass filter to improve stability.

Fig. 3. *Laser transmitter block diagram.*



The gain through the op amp and the p-n-p transistor affects the accuracy of the loop in holding to the original setting. The op amp has a typical gain of 20 dB. Depending on the external components used, the total voltage loop gain is nominally 40 dB. This is adequate to hold the bias. Current gain is supplied by the external p-n-p transistor.

AC Driver Circuit. The ac driver uses a differential collector-driven output configuration. The nominal output impedance is 50 ohms. The drive current is controlled by the external potentiometer, Pot 2. A temperature and supply compensated constant-current bandgap reference is used to bias the current source. The external resistor should have a low temperature coefficient to minimize its effect on the ac drive as the temperature changes. The supply to the final output stage is made available to the user for filtering out supply noise.

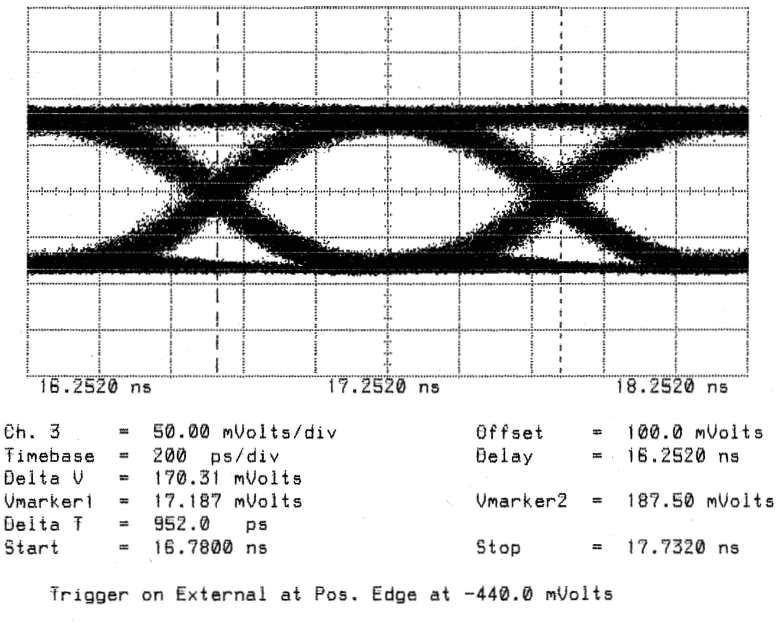
The equivalent ac impedance for the laser diode is on the order of 10 ohms. To assist the ac driver in driving current to the laser and not to the supply path, an 8-ohm resistor and an RF filter are used to increase the impedance looking into the dc bias network.

Fig. 4 shows the optical eye pattern from a 780-nm CD laser. The typical 20-to-80% rise or fall time into a 25-ohm load is 250 ps. The driver can also be adjusted to operate with 1300-nm single-mode lasers.

Laser Monitor and Safety Control. The built-in safety circuit uses the monitor diode current to check for high optical output power. The circuit monitors the laser output for deviations larger than ±10% from the nominal power setting. If the optical power is out of this window, the monitor starts the laser turn-off process. If the fault state continues for a time set by the error timing capacitor LZTC, the laser will be turned off. The circuit can then only be reset by cycling the laser-on pin, LZON.

The laser safety circuit can be activated in different ways. In all cases, the laser is turned off by pulling a large current at the LZMDF pin, causing the window detector to sense a fault. This causes the LZDC output to go high and turn off transistor P1. At the same time, the ac driver is held in a static state. This is necessary because the ac circuit has enough output drive to pulse the laser without the dc bias current.

Fig. 4. *780-nm CD laser eye pattern (–3 dBm).*



The window detector monitors the voltage on LZMDF. The high and low levels are set at 1.85V ±10%. This translates directly to monitoring whether the optical output power has deviated more than ±10% from the nominal setting. If LZMDF goes out of this range, the charge on the LZTC capacitor will be discharged by a few hundred microamperes of current. If the fault continues and the voltage lowers to the fault value (1.3V), then the error detector cell will output a TTL high level on the LZF pin and turn off the dc bias. The error time is set by the capacitance between LZTC and ground. This will be a few milliseconds for a 0.1-μF capacitor.

There is also a bandgap monitor cell which checks for gross faults with the 2.42V bandgap. Because this bandgap is used in setting the window range, a change will not necessarily cause the window detector to sense a fault. The bandgap monitor uses the V_{CC} voltage as a reference to sense when the bandgap is higher than 3.0V or lower than 2.0V. The 3.0V translates into a maximum 2× increase in optical output power before the laser is turned off.

Once a fault has been detected, this condition is latched until the laser driver is reset using the LZON pin. A TTL high on LZON will charge the LZTC capacitor while holding the laser output off. When LZON is set low again, all laser circuitry is enabled.

Transmitter Multiplexer

The block diagram of the transmitter multiplexer is shown in Fig. 5. In the normal 1062.5-Mbit/s mode, shift registers are loaded with the 20-bit-wide parallel data and then shifted to form the high-speed output. To conserve power, an interlacing method is used to allow the shift registers to operate at half speed. These registers are separated into two banks of ten and are loaded with the proper bit order. The outputs of the two banks are then combined with one high-speed D flip-flop. In the 531.25-Mbit/s mode, only 10 bits are loaded into a single bank and the second bank is ignored.

The data byte 1 inputs are inserted with a set of latches, allowing this data to be shifted by one-half bit relative to data byte 0. This configuration allows for the ping-pong mode of operation, in which the two input bytes are time-shifted by one-half bit to minimize possible switching noise.

An extra feature of the transmitter is “comma” character generation. When this mode is asserted, the K28.5 character (0011111010) is loaded into the shift registers. This is particularly helpful in the evaluation phase of the chipset for byte-aligning the receiver without the higher-order FC-1 and FC-2 chips.

Transmitter Clock Generator

The logic block diagram of the transmitter clock generator is shown in Fig. 6. It takes the input from the VCO at 1062.5 MHz and derives the necessary clocks for the multiplexer. The clock rate reduction involves serial divisions of 2, 2, and 5 for the 1062.5-Mbit/s (20-bit) mode and 2, 5, and 2 for the 531.25-Mbit/s (10-bit) mode. The divide-by-5 function is last for the 1062.5-Mbit/s mode, allowing it to operate at the slower speed to reduce power. All of the clocks are retimed by the high-speed clock to ensure proper clock alignment.

Fig. 5. Transmitter multiplexer block.

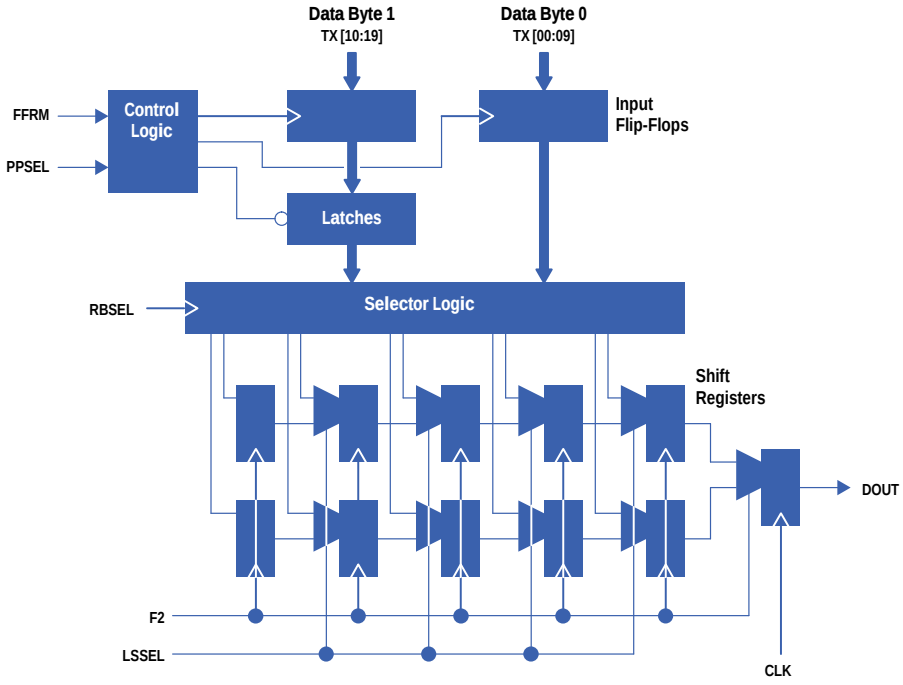
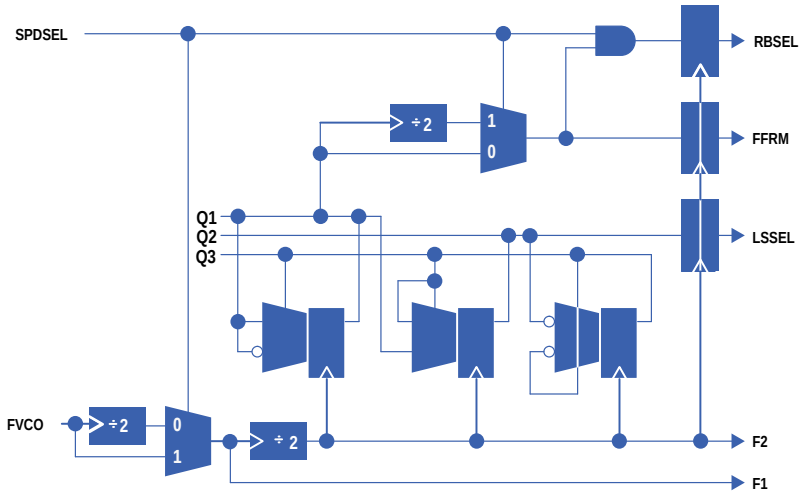


Fig. 6. Transmitter clock generator.



Transmitter Phase-Locked Loop

The phase-locked loop is a bang-bang type and is able to lock onto the reference clock at 53.125 MHz. It consists of a modified sequential detector, a charge pump integrator, a VCO, and the clock generator. The detector, integrator, and VCO were leveraged from the G-Link chipset.[1] The nominal bang-bang time of the VCO is 1 ps per cycle.

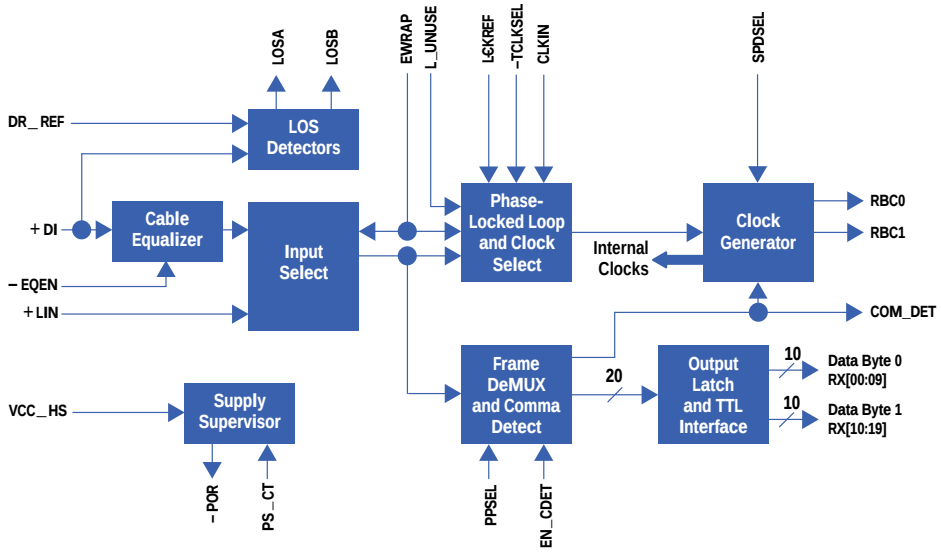
Receiver Chip

The block diagram of the receiver chip is shown in Fig. 7. It consists of the demultiplexer, the phase-locked loop and clock generator, redundant loss-of-signal (LOS) detectors, and other I/O and supporting circuits such as the power-on supervisor.

Receiver Demultiplexer

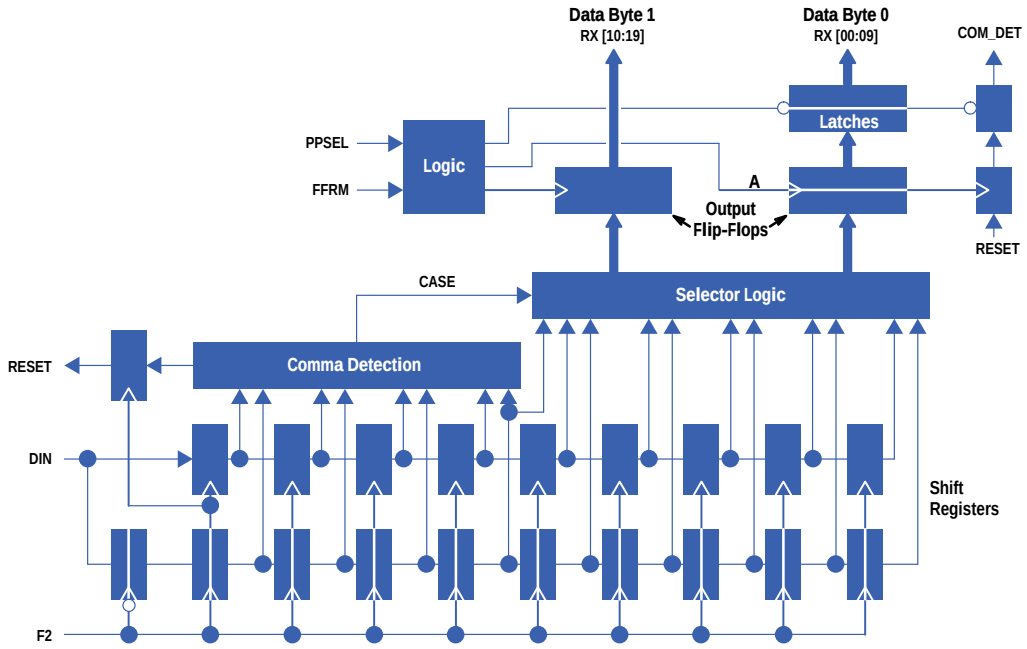
The logic diagram of the demultiplexer is shown in Fig. 8. In addition to providing the serial-to-parallel conversion of the input bit stream, it also detects the comma character (0011111xxx) for proper frame alignment, as required by the Fibre Channel standard. Once the comma character is detected, a reset signal is sent to the clock generator for synchronization.

Fig. 7. *HDMP-1514 receiver chip block diagram.*



To minimize power consumption, an interlacing method of demultiplexing is used in the receiver chip. The high-speed data stream is first deciphered into two streams at half the rate, and these are loaded into two banks of shift registers. The parallel data in the shift registers is then clocked into the output flip-flops at the frame rate. An extra bank of latches is added for data byte 0, which enables the ping-pong mode of operation.

Fig. 8. *Receiver demultiplexer.*



Since there are two possible ways in which the deciphering can occur, that is, bit one could be in either bank one or bank two, proper decoding is needed to reassemble the final byte pattern. This is accomplished by the selector block preceding the output flip-flops, and is controlled by how the comma character is detected within the two banks. When either case is detected, the reset indicator to the clock generator is set high. Since this signal is a critical path in the overall operation of the chip, it is retimed to give the clock generator more margin to reset. As a result, the data is delayed by an additional cycle before being loaded out. This delay is compensated by extending the shift register count by one.

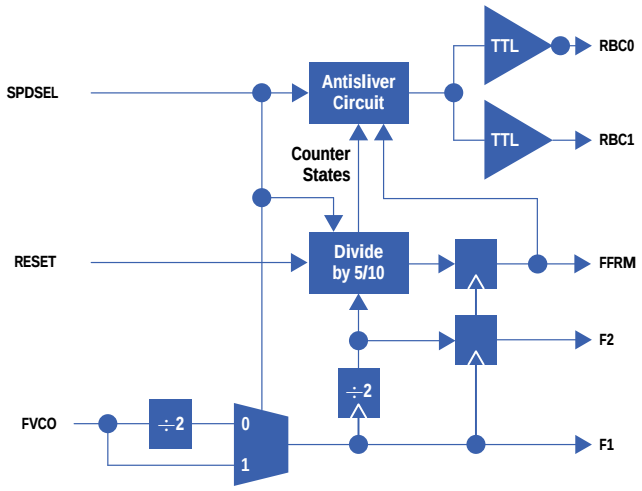
The data is further delayed before unloading by the antisliver feature (discussed next) in the clock generator where the clocks are extended. The number of registers is increased in the same manner to compensate.

Receiver Clock Generator and Antisliver Circuit

The logic diagram of the clock generator is shown in Fig. 9. In a manner similar to its transmitter counterpart, it takes the VCO output and generates all of the necessary clocks required by the chip. It includes an antisliver circuit, which ensures that the frame clock presented to the user has no "slivers," as explained below.

The core of the generator is a divide-by-5-or-10 counter. To minimize power, the frame clock goes through a 2,10 scaling for the 1062.5-Mbit/s mode, and a 2,2,5 scaling for the 531.25-Mbit/s mode. However, RBCLK requires a clock at the frame rate that must have a 50% duty cycle. Since this is not possible with the natural states within the divide-by-five counter (2/5 or 3/5), the pulse of the 2/5 count is extended by one cycle of the high-speed clock, yielding the required 50% duty cycle.

Fig. 9. *Receiver clock generator.*



When the reset signal is applied, the counter is forced to a predetermined state. Because the previous state of the counter is random, the frame clock may contain short pulses or slivers, which could cause problems for the user. The antisliver circuit continuously monitors the counter for this condition and masks these bursts as they occur. The logic accommodates both the 531.25-Mbit/s mode and the 1062.5-Mbit/s mode.

Receiver Phase-Locked Loop

The phase-locked loop of the receiver uses the same basic configuration as the transmitter phase-locked loop, with the addition of a phase detector for NRZ data. The design of this detector is identical to the detector used in another proprietary HP IC,[4] with the exception that the falling edges are ignored. This is to eliminate any effect of the excess jitter of the falling edge, which arises from the self-pulsing CD lasers. The lock-to-reference (–LCKREF) input enables the user to activate the frequency detector for initial frequency acquisition.

Receiver Loss-of-Signal (LOS) Detector

With major concerns for eye safety, the Fibre Channel standard calls for redundant LOS detectors within the optical module to ensure a robust system. Two LOS detectors are incorporated in the receiver IC, and are provided as outputs to the OFC chip. Since the alarm outputs are heavily filtered within the OFC chip, hysteresis is not necessary in the LOS design.

The LOS detectors are based on a concept of envelope detection without the use of a capacitor. One detector is configured to detect the loss of amplitude resulting from a lack of received signal. The second detects the condition in which the differential inputs are static, indicating a fault in the optical receiver. Both LOS detectors are further digitally filtered, with one driven by the reference clock and the other by an internal clock. This further ensures the reliability of the fault detection system for maximum safety. The triggered threshold is preset to 25 mV and can be adjusted with an external resistor, as shown in Fig. 10.

The receiver front-end sensitivity is well below the nominal LOS threshold of 25 mV. Fig. 11 shows the bit error rate (BER) as a function of the input differential signal. The BER is basically zero for signals 6 mV and above. Because it is impractical to perform actual tests for BER as low as 10^{-20} (~3000 years), one can use the plot to extrapolate the BER for the incoming signal amplitude. Tests have been run for weeks without a single error.

Transceiver Chip

One major target application for Fibre Channel is disk arrays. This application demands a much lower-power and lower-cost solution than the chipset offers. The new HP HDMP-1526 transceiver is a 10-bit, 1062.5-Mbaud transceiver designed for this

Fig. 10. *LOS threshold as a function of DR_REF.*

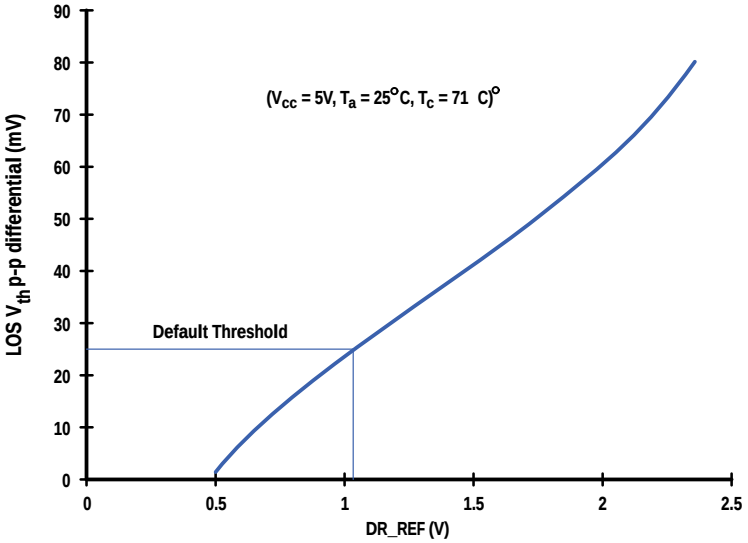
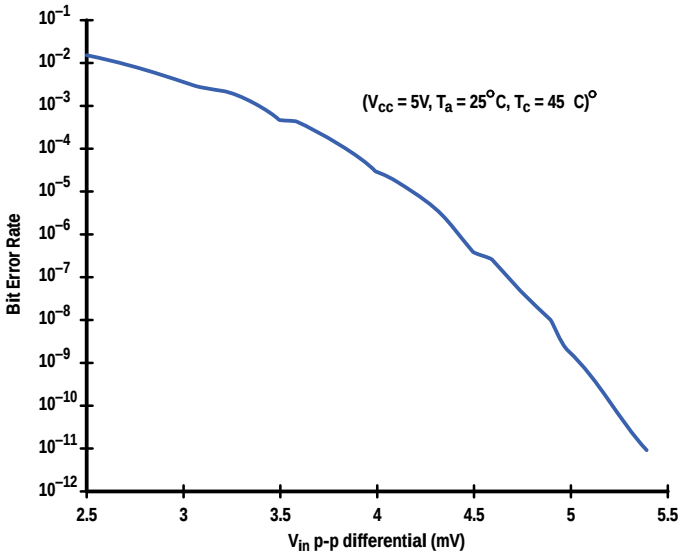


Fig. 11. *BER as a function of data input amplitude.*



Fibre Channel arbitrated loop (FC-AL) market. It is a descendant of the HDMP-1512/HDMP-1514 20-bit, 1062.5/531.25-Mbaud transmitter/receiver chipset. The Fibre Channel chipset has many functions not needed in the FC-AL transceiver chip, such as optical interface blocks. Fig. 12 shows the block diagram of the transceiver. The reduction in functions and the change to a 10-bit bus allowed the integration of both transmitter and receiver functions onto a single die, using a proprietary HP device array. The transceiver uses a 10-bit parallel interface running at 106.25 Mbaud instead of a 20-bit parallel interface running at 53.125 Mbaud.

Deletions on the transmitter side include the ac laser driver and its supporting dc bias circuitry and the comma generator function. Deletions on the receiver side include the power-on/reset circuitry, the loss-of-signal circuitry, and the cable equalizer function. Deleted functions common to both the transmitter and receiver include the speed selector and the ping-pong selector. The loopback ports were also deleted because an internal connection is possible with a single-chip design. This leaves just one high-speed output port and one-high speed input port. Other timing changes were implemented to fit specific customer needs.

Fig. 12. *Transceiver block diagram.*

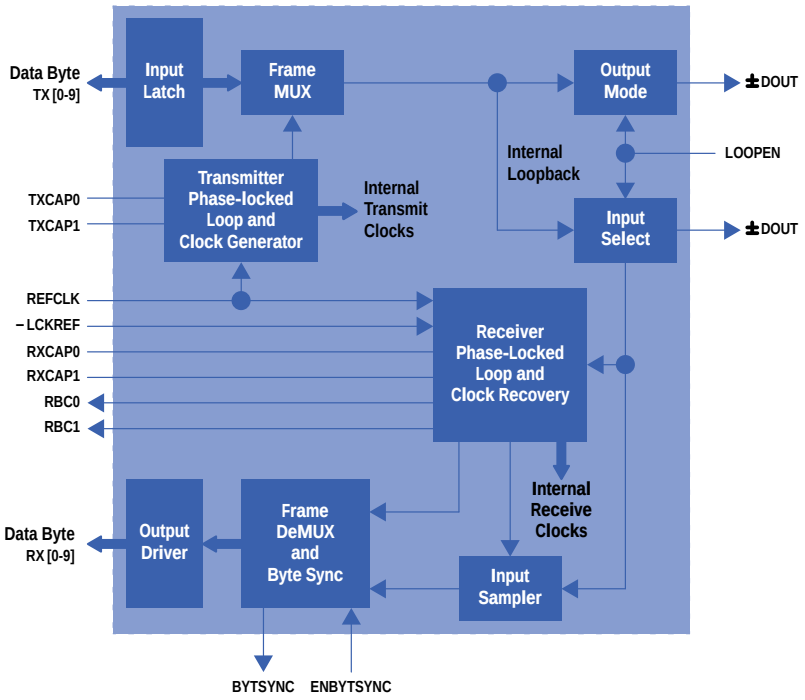
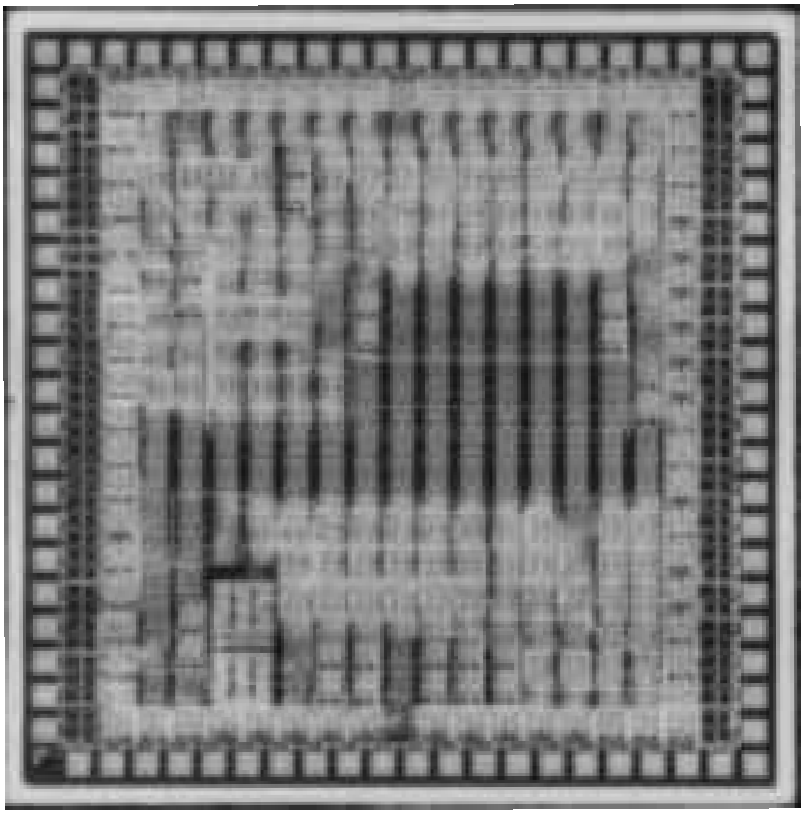


Fig. 13. *Transceiver die (proprietary HP array).*



In the single-chip design, select inputs and clocks are shared between the transmitter and receiver. This lowers the power requirements, reduces the number of pins, and makes possible a smaller chip size if a custom layout is done at a later date. The transceiver, with its 1.8-watt total power dissipation (compared to 3 watts for the chipset), is packaged in a single 64-pin 14-by-14-mm quad flat pack.Isolating the two independent phase-locked loops within a 3.54-mm-by-3.54-mm area presented the biggest challenge during the layout of the chip. The transmitter and receiver phase-locked loops are placed at opposite corners to minimize cross talk. Various portions of the chip are isolated by using separate power supplies and bandgap references. Although much of the chip and block-level layout was redone starting from the 20-bit chipset, the proprietary HP array enabled us to complete the transceiver design very quickly. Fig. 13 shows a photograph of the FC-AL 10-bit transceiver die implemented on the array.

Summary

A two-chip gigabit chipset conforming to the FC-0 specification has been fabricated. The speed of the chipset is user-selectable at either 1062.5 Mbaud or 531.25 Mbaud. The transmitter integrates a high-speed laser driver capable of driving either 780-nm CD lasers or 1300-nm lasers. The receiver has redundant loss-of-signal detectors for eye safety. The chipset runs on a single +5Vdc supply and has TTL data and control interfaces. Implementation using a proprietary HP device array allowed a quick design cycle to produce a 10-bit single-chip transceiver for the FC-AL market.

Acknowledgments

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