Symmetric Multiprocessing Workstations and Servers System-Designed for High Performance and Low Cost

A new family of workstations and servers provides enhanced system performance in several price classes. The HP 9000 Series 700 J-class workstations provide up to 2-way symmetric multiprocessing, while the HP 9000 Series 800 K-class servers (technical servers, file servers) and HP 3000 Series 9x9KS business-oriented systems provide up to 4-way symmetric multiprocessing.

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Blending high performance and low cost, a new family of workstations and servers has been designed to help maintain HP's leadership in system performance, price/performance, system support, and system reliability. This article and the accompanying articles in this issue describe the design and implementation of the HP 9000 J-class workstations, which are high-end workstations running the HP-UX* operating system, the HP 9000 K-class servers, which are a family of midrange technical and business servers running the HP-UX operating system, and the HP 3000 Series 9x9KS servers, which are a family of midrange business servers running the MPE/iX operating system. In this issue, these systems will be referred to collectively as J/K-class systems.

The goals of the the design team were to achieve high performance and low cost, while at the same time creating a broad family of systems that would share many of the same components and meet a wide range of customer needs. The challenge was to create a list of requirements that would meet the needs of the three different target markets: the UNIX®-system-based workstation market, the UNIX-system-based server market, and Hewlett-Packard's proprietary MPE/iX-system-based server market. The basic requirements for these systems were to deliver leadership symmetric multiprocessing performance, memory performance, and capacity, along with exceptional I/O performance. Balanced system performance was the overall goal.

Hardware Features

All of the J/K-class platforms are built around the same basic building blocks (see Fig. 1). The backbone of these systems is the high-speed processor-memory bus called the Runway bus. This is a 640-to-768-Mbyte/s (peak sustained bandwidth), 64-bit-wide bus that connects the processors, system main memory, and the I/O adapter (bus converter). The Runway bus is described in more detail in *Article 2*. The I/O adapter provides connections to two HP-HSC (Hewlett-Packard high-speed system connect) buses, providing a raw I/O bandwidth between 128 Mbytes/s and 160 Mbytes per second (95 to 116 Mbytes/s peak sustained bandwidth). The HP-HSC bus is an extension of the GSC (General System Connect) bus used in earlier workstations.[1]

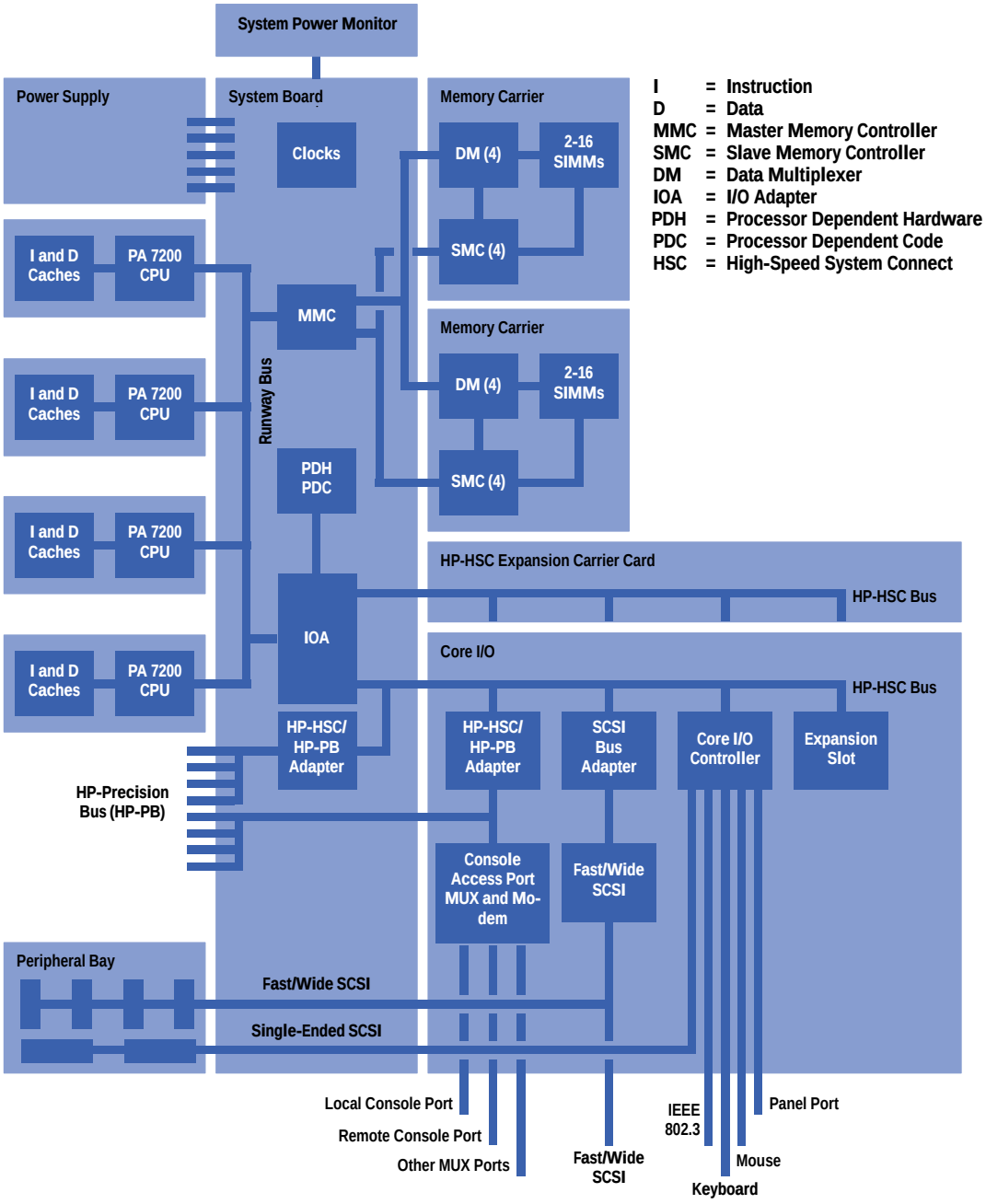
In addition to the Runway and HP-HSC buses, the J/K-class systems also support a connectivity I/O bus. In the HP 9000 J-class workstation systems, the connectivity I/O bus is EISA (Extended Industry Standard Architecture); it has a peak bandwidth of 32 Mbytes/s. In the HP 9000 K-class and HP 3000 Series 9x9KS server systems, the connectivity I/O bus is the HP Precision Bus (HP-PB). The servers have one or two four-slot HP-PB adapters. Each HP-PB has a peak bandwidth of 32 Mbytes/s.

Processor

The core of the J/K-class systems is a high-performance processor module that interfaces directly to the Runway bus. It is based on the HP PA 7200 CPU chip,[2] a PA-RISC superscalar processor, which is an evolution of the high-performance, single-chip, superscalar PA 7100 processor. The PA 7200 incorporates a high-speed Runway bus interface, a new data cache organization with an on-chip assist cache, data prefetching, and two integer ALUs. This microprocessor is fabricated using HP's 0.55-micrometer CMOS process and delivers reliable performance up to 120 MHz. More information on the PA 7200 can be found in *Article 3*. Fig. 2 is a photograph of the processor module.

The tables on pages 3 and 4 indicate the processor speeds for each of the platforms in the J/K-class family. Table I is for the HP-UX workstation systems, Table II is for the HP-UX symmetric multiprocessing servers, and Table III is for the MPE/iX symmetric multiprocessing servers.

Fig. 1. *Block diagram of the HP 9000 Model K400 server.*



System Board

Central to the J/K-class systems is the system circuit board (Fig. 3). This printed circuit board contains all the circuitry required for implementing the Runway bus and connectors for the processors, the master memory controller, and the I/O adapter. The bootstrap code and other system-specific hardware are also on the system board. For the entire family of J/K-class systems, there are only three system board designs: one for the 1-way or 2-way symmetric multiprocessing workstation configuration (J class), one for the uniprocessor server configuration (K 100), and one for the 1-way to 4-way symmetric multiprocessing server systems (K2x0, K4x0).

In the workstation systems, the system board includes the Runway bus and system dependent hardware mentioned above, the complete memory system including the connectors for the memory modules (SIMMs), most of the circuitry required for the system's built-in I/O functionality (core I/O), and power supply management and control circuits. Five I/O slots are provided for system I/O expansion. These five slots are shared; a combination of EISA and HP-HSC cards can be installed, with a maximum of four EISA cards or three HP-HSC cards. For example, a system could have four EISA cards and one HP-HSC card, or three EISA and two HP-HSC cards, or two EISA and three HP-HSC cards.

Fig. 2. *Processor module.*

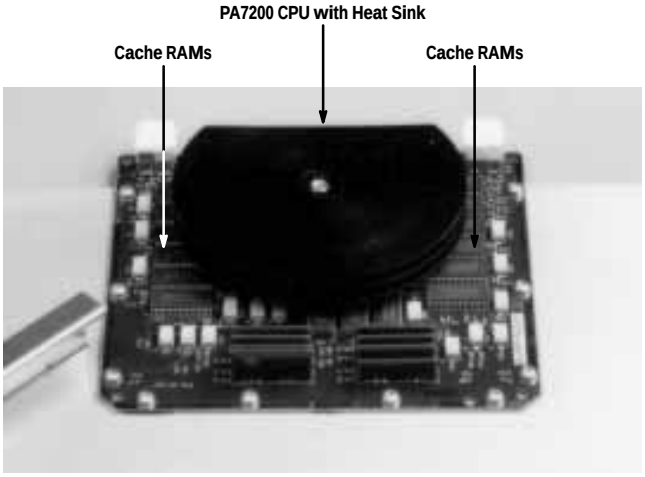


Fig. 3. *System board.*

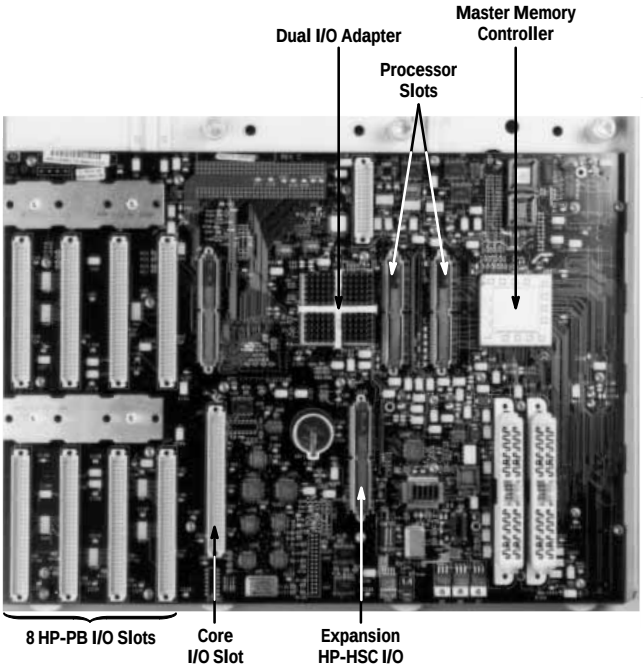


Table I
HP 9000 J-Class Processor Speeds

Model	Processor Slots	Processor Speed
J200	2	100 MHz
J210	2	120 MHz

Table II
HP 9000 K-Class Processor Speeds

Model	Processor Slots	Processor Speed
K100	1	100 MHz
K200	4	100 MHz
K210	4	120 MHz
K400	4	100 MHz
K410	4	120 MHz

Table III
HP 3000 Series 9x9KS Processor Speeds

Series	Processor Slots	Processor Speed
939KS	1	80 MHz†
959KS	4	100 MHz
969KS	4	120 MHz

† Effective Processor Speed

The symmetric multiprocessing server system board includes the Runway bus and system dependent hardware as described above, along with slots for a separate core I/O card, an optional expansion HP-HSC I/O carrier card, one or two 1G-byte memory carriers, and four or eight HP-PB slots. Four Runway slots are provided for the processor modules. Depending on the processor used in the system, the Runway bus operates at 100 MHz or 120 MHz.

The uniprocessor system board (HP 9000 Model K100) has a single processor, all memory controllers and SIMM slots, a core I/O card slot, and four HP-PB slots.

System Firmware

All of the J/K-class systems share a common firmware base that tests and initializes the system on power-up. This code is a combination of PA-RISC assembly code and C. It was a design goal to support all of the server products using the same firmware and to have a common firmware base for the technical workstation products. The code was designed in a very modular fashion so that the code base could be easily ported to the various system platforms.

The system firmware is designed to be very robust. For example, during memory configuration and test, it uses a combination of bank and page deallocation to deconfigure memory containing hard errors, allowing the user to continue using the system until the failing memory can be replaced. Similarly, processors that fail self-test are deconfigured and the system boot process is continued.

In addition to providing a robust system to the customer, the system firmware allows designers and the manufacturing processes easy access to system test and configuration of hardware and firmware features. Some of these features allow enabling or disabling of processor cache prefetching, full memory test or memory initialization only, and so on. This helped in the system debug effort by speeding the boot process and making it possible to disable certain functions while searching for the root cause of a bug in the system.

Another feature built into the system firmware during the system debug process was a debug interface that would allow the lab engineers to set soft breakpoints and step through instruction execution one instruction at a time. This tool proved to be quite valuable, providing increased visibility into system behavior and the system state.

The J/K-class firmware is installed in flash EPROM. The firmware can be updated through the system offline diagnostic environment. If for any reason the system firmware needs to be modified, it can easily be upgraded by loading a new firmware image from tape or another medium into system memory and then loading it into the firmware flash EPROM.

The result of these design choices is system firmware that provides flexible functionality, reliable system test and initialization, and some tolerance for certain types of failed components in the system boot process.

High-Performance Memory

Memory performance was highly important throughout the J/K-class system design and implementation. The J/K-class memory subsystem is designed with consideration for high bandwidth, low latency, and expandability from 32M bytes to 2G bytes. It is capable of interleaving memory accesses across 32 banks of memory. The memory system is built around the master memory controller (MMC), which interfaces to the high-speed Runway bus. The MMC communicates with up to eight slave memory controllers (SMC) on one or two memory carriers (see Fig. 4 and *Article 5*). Also on the memory carriers are data multiplexers and pairs of SIMMs (single-inline memory modules). This design results in a high-bandwidth, interleaved, 2G-byte memory subsystem. As 64M-bit DRAMs become cost-effective, the 2G-byte limit will increase to 3.75G bytes of main memory. Table IV shows the maximum amounts of memory available in various J/K-class systems.

Fig. 4. *Memory carrier board.*

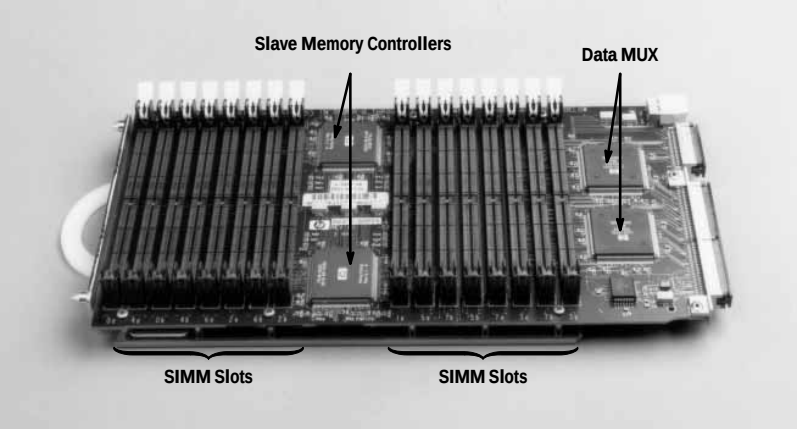


Table IV
Maximum Memory

System Type	Model or Series	Maximum Memory
HP 9000	Model J2x0	1024M Bytes
HP 9000	Model K100	512M Bytes
	Model K2x0	1024M Bytes
	Model K4x0	2048M Bytes
HP 3000	Series 939KS	1856M Bytes
	Series 959KS	2048M Bytes
	Series 969KS	2048M Bytes

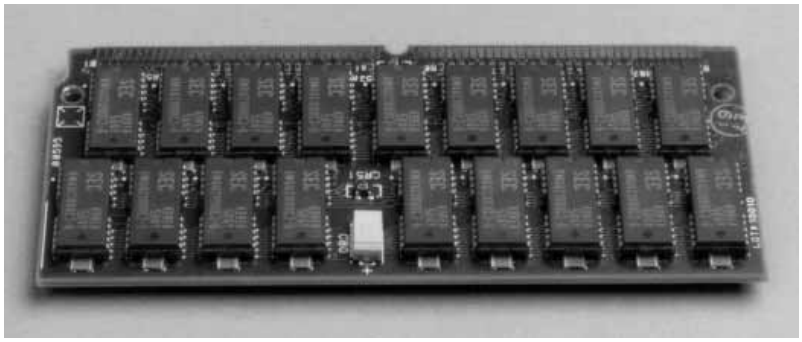
Supporting a high-density and high-performance memory system with industry-standard memory SIMMs would have resulted in a costly memory system that would not have performed at the desired levels. Instead of the industry-standard approach, a denser memory module was designed. These memory modules (Fig. 5) are actually a dual-inline design, although they are still referred to as SIMMs. In the J/K-class systems, these dual SIMMs are inserted in pairs, providing two separately addressable, 128-bit, ECC (error correcting code) protected banks of memory (144 bits including ECC check bits). Each dual SIMM provides 72 bits of the two 144-bit banks. Using 4M-bit or 16M-bit DRAMs, the SIMMs are available in 16M-byte and 64M-byte sizes. While these memory modules are not standard, there is no HP proprietary technology in them, helping to keep memory pricing very competitive with the industry.

I/O Adapter

The J/K-class I/O adapter (bus converter) interfaces between the Runway bus and the HP-HSC I/O bus. The I/O requirements for a J/K-class system call for multiple I/O buses, so the I/O adapter package contains two fully independent bus converters (see Fig. 6a). To maximize system flexibility, the I/O adapter is designed to support a range of bus frequencies on either bus, thus requiring a full synchronizer. Fig. 6b is a block diagram of the I/O adapter.

The HP-HSC bus only has a 32-bit address space, while the Runway bus supports a 40-bit address space. This requires an address translation mechanism to provide the additional eight address bits. The processor's aggressive data prefetching requires a new mechanism for DMA (direct memory access) to coexist with this processor feature. Hardware cache coherent I/O solves these two problems (see *Article 6*). Prefetching is also included in the HP-HSC bus to reduce memory read latency and increase I/O bandwidth. All of these features required additional hardware support in the I/O adapter.

Fig. 5. *Dual-inline memory module.*



According to the PA-RISC architecture definition, a bus converter also needs to provide the registers to configure address space, enable and disable features, log errors, manipulate the TLB, and provide diagnostic access. Therefore, these registers are included in the I/O adapter.

The J/K-class systems required several other hardware features that by default were put into the I/O adapter. Among these is the hardware to interface to external components implementing the processor dependent hardware (PDH) necessary to provide boot firmware, stable storage for system configuration information and error logging, and scratch RAM. The I/O adapter also provides a real-time clock for keeping track of time when power is off.

Basic VLSI support of scan-based testing, both internal and boundary (JTAG or IEEE 1149.1), is built into the I/O adapter, along with double-strobe capability for speed path testing and built-in self-test (BIST) for the RAM structures.

Finally, it was desired that the design be done in a modular fashion, enabling future designs to easily borrow portions of the design for future enhancements or to lower costs. This required that the chip be designed with well-defined and simple interfaces. The synchronizers made very natural places to define the boundaries of these modules. All of these requirements led to a modular, synchronizer queue-coupled, hardware cache coherent, dual bus converter design.

Core I/O Functionality

The basic I/O requirements for both the workstation and the server systems include 20-Mbyte/s fast-wide SCSI (Small Computer System Interface) for system disk connectivity, 5-Mbyte/s single-ended SCSI for archival storage, and an IEEE 802.3 LAN interface for networking. The HP-UX systems also include a Bitronics parallel interface port, keyboard and mouse connections, and serial I/O ports as part of the core I/O functionality. A photograph of the K-class core I/O board is shown in Fig. 7. The workstation model adds high-quality audio input and output to the built-in core I/O.

The server system includes additional serial ports and an integrated modem for remote service access. The server systems also have a remote service console access port to allow remote servicing of hardware and software by Hewlett-Packard's customer support organizations.

I/O Expansion

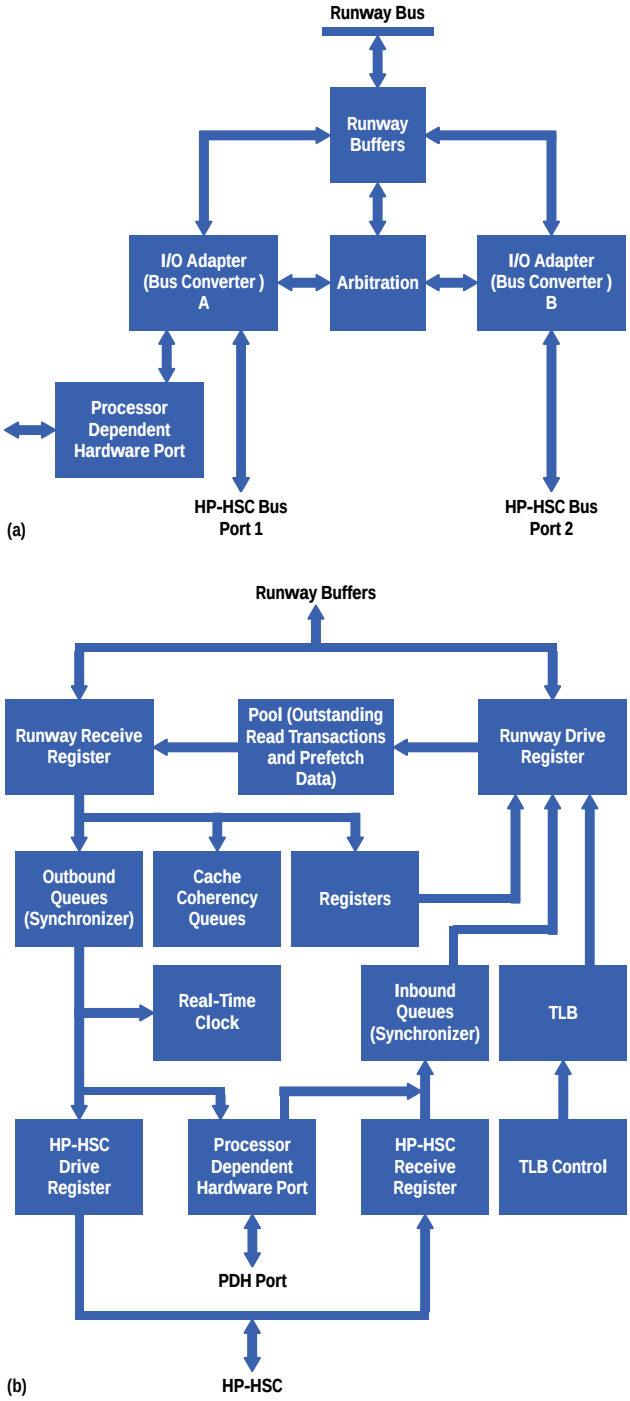
On the HP 9000 K-class server systems, several configurations support various system I/O needs (see Table V). As a minimum, the system comes with one 32-MHz HP-HSC bus slot for expansion I/O. This slot is in a compact 3-by-5-inch form factor. As I/O needs increase, the system can be upgraded to provide four 40-MHz HP-HSC slots in addition to the one 32-MHz HP-HSC slot (Model K4x0 only). In addition to the HP-HSC slots, the K-class server has four or eight Hewlett-Packard Precision Bus (HP-PB) slots. These slots are configured such that the user can install up to four double-high HP-PB cards and still have four single-high HP-PB card slots available.

Table V
HP 9000 K-Class I/O Expansion Capabilities

Model	HP-HSC Bus Slots	HP-PB Slots	Peak Sustained I/O Bandwidth†
K100	1	4	95 Mbytes/s
K200	1	4	211 Mbytes/s
K210	1	4	211 Mbytes/s
K400	5	8	211 Mbytes/s
K410	5	8	211 Mbytes/s

† Combined bandwidth of the two HP-HSC buses.

Fig. 6. *(a) There are two fully independent I/O adapters in the I/O adapter package. (b) I/O adapter block diagram.*



In the HP 9000 J-class workstation configurations, the system supports an 8-MHz EISA bus (maximum of four slots) and a 40-MHz HP-HSC expansion I/O bus (maximum of three slots). These slots provide the workstation user with a great deal of flexibility in configuring I/O devices and meeting high-speed I/O requirements (see Table VI).

Fig. 7. *K-class core I/O board.*

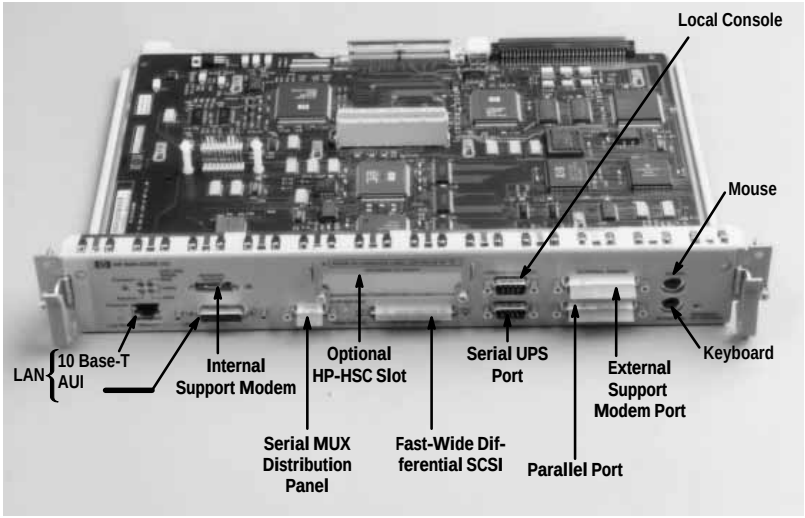


Table VI
HP 9000 Model J2x0 I/O Expansion Capabilities

I/O Slot	Configuration
Slot 0	HP-HSC
Slot 1	HP-HSC or EISA
Slot 2	HP-HSC or EISA
Slot 3	EISA
Slot 4	EISA

A number of I/O cards are currently available for use in the high-speed I/O and HP-PB bus slots. A number of EISA cards are supported in the workstation system. The following is a partial list of the I/O cards available for J/K-class systems:

- 5-Mbyte/s single-ended SCSI
- 20-Mbyte/s fast-wide SCSI
- HP Fiber Link
- IEEE 802.3 LAN
- IEEE 802.5 token ring
- FDDI
- FibreChannel
- ATM (asynchronous transfer mode)
- Programmable serial interface
- Bitronics parallel port
- 16-port serial RS-232
- 32-port serial RS-232
- 2D graphics card
- 3D graphics card.

Integrated Peripherals

The server systems all have a standard DDS tape drive and a CD-ROM drive integrated into the system. In addition, there is space available for up to four 20-Mbyte/s SCSI disk drives in the system box. The workstation comes with a standard 3.5-inch flexible disk drive, a CD-ROM drive, a tape drive, and two slots for 20-Mbyte/s SCSI disk drives built into the system box.

Industrial Design

The J/K-class industrial design is intended to convey a strong perception of the power within, wrapped in bold, distinctive designs that are elegant and pleasing to the eye. The K-class product is designed to work as a floor-standing product as well as rack-mounted in an industry-standard HP 19-inch EIA rack (Fig. 8). A growing number of rack-mounted HP peripheral products such as disk arrays, uninterruptible power supplies, and LAN hubs complement the overall system. The J-class system (Fig. 9) is designed for floor-standing use in the commercial workstation environment, but can be rack-mounted on a custom basis.

Fig. 8. *K-class server configurations.*

These machines were designed with ease of assembly and serviceability as high priorities. They use plastic parts that snap together over a riveted steel chassis without a single screw or fastener, making assembly and disassembly very quick and easy for service and for the eventual recycling at the end of the products' life.

Customer ease of use was another design priority. This is evident in the brightly backlit liquid crystal display, which conveys system status information in a clear text font, a vast improvement over previous systems, which had flashing LEDs. A simple three-position keyswitch for on, off, and service mode is clearly marked and positioned within easy reach on the front of the K-class system. The front door gives the user easy access to peripherals and visual feedback in the form of disk activity lights. Inside the front door are a pocket for the user manual, a safe storage location for the system key, and a system label with the most pertinent user information.

Fig. 9. *J-class workstation system processing unit.*

Extensive effort went into label design, working with field support engineers, to make these products the leaders in their class in ease of installation, serviceability, and field upgradability. The labels use color coding and detailed diagrams clearly defining such things as board locations, memory SIMM loading sequences, and disk locations. These have been very successful in making the many configurations easily understood by customers and HP manufacturing and field service personnel.

Server Package Design

Like every other aspect of the design of the J/K-class systems, designing the chassis and plastics proved to be challenging. With a strong emphasis on development schedule and a desire for a very robust and flexible design, the engineering team had to create some innovative solutions to keep on schedule and keep the cost of the product low.

Several requirements defined the maximum height and width of the server box. It had to fit into a 19-inch rack, so it could be no wider than 17.3 inches and no deeper than 25 inches. It could be no taller than 25.24 inches, so that as a standalone unit it would fit under a standard table.

An additional challenge was that of the Runway bus. The expected high speeds of the bus required that the bus length be kept to a minimum to reduce signal propagation delays. At the same time, up to six different components needed to attach to this bus: four processors, the master memory controller (MMC), and the I/O adapter. The processor module spacing was kept to 1.2 inches, allowing the overall length of the Runway bus to be short enough to support reliable 120-MHz operation.

This small size also presented an additional challenge, that of cooling the many components in the system. An intensive effort was launched to simulate and create mockups of the proposed mechanical designs for airflow and expected internal system temperature rises. A number of cooling alternatives were proposed and evaluated. The resulting solution provides an air-cooled system with excellent airflow and a remarkably quiet system for the power dissipated within the box. There are only two fans in the entire system.

Other desired features helped to define how the system was partitioned into the various circuit boards. Each board needed to be easy to access. Almost every component in the system can be accessed and removed from the system for maintenance or repair in a matter of minutes. The size and type of add-on I/O cards also required some creative design to allow flexibility in the design as well as flexibility for the customer.

Power System

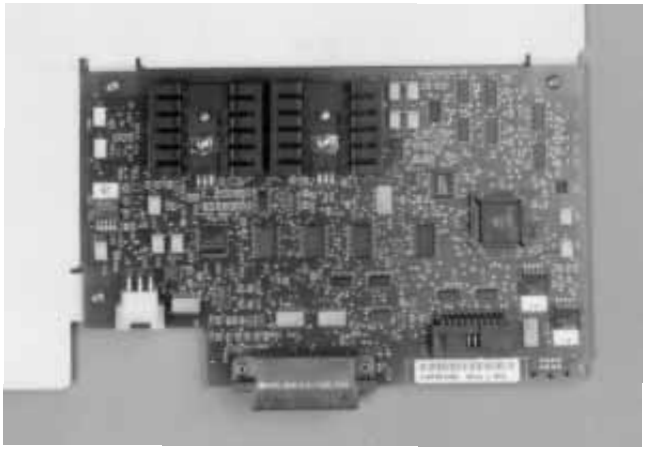
The power system for the J/K-class systems can be split into three subsystems: the system power supply, the system power monitor, and the uninterruptible power supply (UPS). The power features implemented in the workstation and server systems are slightly different but follow the same general philosophy: provide reliable power to the system at a low cost.

The server system power supply provides the voltage rails for the components in the system. This 925-watt supply incorporates power factor correction and accepts a wide range of input voltages and input frequencies between 50 and 60 Hz. It provides a carryover time of 20 milliseconds after a power failure.

The system power supply does not include any intelligence to control the system turn-on or reset activities. This intelligence is provided by the system power monitor (Fig. 10). This circuit monitors the various aspects of the computer system and the power supply output to determine if the power should be turned on or off. This includes monitoring the system internal temperature, checking the voltage output to ensure that there is no undervoltage or overvoltage condition, and providing diagnostic messages on the system's liquid crystal display when problems occur.

The uninterruptible power supply (UPS) is an optional component of the J/K-class systems. It provides additional assurance of system availability and data integrity, even if the ac power lines fail for any reason. Upon a powerfail event, the UPS provides ac power to the system for up to 15 minutes, allowing the system to continue operation, or in the case of an extended power outage, to shut down gracefully and save critical data to disk. When ac power returns, the system will continue operation, or if it was shut down, it can be restarted without loss of data.

Fig. 10. *System power monitor.*



More details on the power supply, monitor, and UPS can be found in the sidebar: *K–Class Power System*.

System Performance

The J/K-class systems were developed to provide customers with excellent performance in the intended markets: midrange servers and high-end workstations. Our goal was not necessarily to provide the highest single-component performance, but to provide customer-valued application performance at an extremely attractive price.

The most common component benchmark is the SPEC (Systems Performance Evaluation Cooperative) suite, which measures CPU integer and floating-point performance. For these benchmarks, the processor in the J/K-class products provides about 168 SPECint92 integer and 258 SPECfp92 floating-point performance at 120 MHz. With the well-balanced symmetric multiprocessing J/K-class systems, the SPECrate_int performance of a four-processor 120-MHz system is 12,150 and the SPECrate_fp92 performance is 19,600.

It is in the real-world applications and at the system level where the J/K-class computer systems really start to shine. The balanced design of the Runway processor-memory bus, the memory subsystem, and the performance I/O system provides the user with exceptional performance. Two widely used benchmarks that try to measure the performance of realistic customer workloads are SPEC SFS1.0(LADDIS) and TPC-C. The 120-MHz LADDIS performance of the J/K-class is as high as 4750 I/O operations per second, which exceeds many high-end servers that typically have twice as many processors (8 to 10 processors compared to four for a Model K400). A four-way J/K-class server at 120 MHz has demonstrated in excess of 3,000 transactions per minute on the TPC-C transaction benchmark. At the time of introduction of the J/K-class systems, the only other single system with higher performance was HP's own T500 corporate business server.

On the technical side, workstation applications clearly benefit from the increased memory bandwidth. At the same time, the introduction of multiprocessing in a high-end client configuration provides the opportunity for either parallel processing of a single task or more parallel execution for multiple tasks. With the addition of the new high-end HP Visualize48 graphics, for which the J-class systems provide some specific hardware performance enhancers, the workstation products will handle large, complex design and visualization problems easily.

Design for Lasting Value

The J/K-class systems were designed to provide HP's customers with lasting value. Processors can be easily added to the system, to a maximum of two processors in the workstation systems and up to four processors in the server systems.

Upgrading from 100-MHz to 120-MHz processors is just as simple. The J/K-class systems are also designed to accept future processors easily, such as the PA 8000 processor,[3] through a simple processor module upgrade.

Not only are processors easy to upgrade, but memory and I/O are also designed so that it is easy to add memory and I/O functionality. Memory can be added in 32M-byte or 128M-byte increments up to 1024M bytes in a J-class system or up to 2048M bytes in a K-class or Series 9x9KS system. As increased-density DRAMs become cost-effective, memory limits will increase to 3.75G bytes of main memory, filling most users' memory configuration and capacity requirements far into the future.

System Verification

The design of any computer system requires an extensive test and verification effort. For the chips and boards designed for the J/K-class platforms, many engineer-months were dedicated to ensuring the systems manufactured and shipped to HP's customers are of the highest quality and reliability. This testing can be grouped into several different categories: presilicon chip and system simulation, formal verification methods, system functional verification, chip and system electrical characterization, and system validation.

Simulation. Before committing any part of the J/K-class design to silicon, extensive simulation had already proven the basic functionality of each component individually and as part of the system. Each component design team provided a model of their particular part of the design to an overall system simulation team. The system simulation team then pulled together tools first to simulate subsystems and eventually to simulate the entire J/K-class system. In addition to the logical simulation to verify correct functionality, electrical simulation was done for the critical portions of the system such as clock distribution, system buses, and chip internal critical paths (see *Article 4*).

Formal Methods. For some parts of any design, it is very difficult to verify complete adherence to design specifications. One area of concern in the J/K-class design was the bus protocols for the Runway bus. In an effort to reduce risk and improve system reliability, formal methods[4] were used to analyze the bus transaction protocols used in the Runway bus definition. The analysis pointed to several defects, which were corrected before implementation of the system.

Functional Verification. As the first components became available to the design teams for initial debugging, efforts were focused on verifying that each component functioned properly in the system. The first goal was to boot the system to the initial system loader. At this point either the operating system (HP-UX) could be loaded or system and component diagnostics could be loaded. While booting the operating system is a great accomplishment, the task of verifying correct functionality was far from completed when this was done.

Numerous tests were developed specifically for the J/K-class systems. These tests employed a number of techniques for finding defective components and defects in design. These techniques included pseudorandom and pseudoexhaustive code and data sequences that stressed the processors (integer units, floating-point units, caches, program control, etc.), the memory and memory controllers, and the I/O bus adapters and I/O controller cards.

Electrical Characterization. Once a minimal level of system functionality was attained, several electrical characterization efforts were launched to prove that the components and the system would function in the electrical environment. This testing focused on measuring electrical noise on chips as well as boards, and looking at bus cross talk and power supply variation and noise. Systems were stressed beyond normal temperature ranges, voltage ranges, and frequency ranges to find the weakest link in the system electrical environment. Through all this characterization effort, designs were modified and improved, resulting in a system that is capable of running reliably throughout the specified system operating environment.

System Validation. Because of the desire to stress the system beyond what HP's customers will do, the functional and electrical characterization efforts mainly focused on test software and environments that do not match our customers' operating conditions. While it is likely that all hardware defects (design related as well as manufacturing related) will be found with the methods shown above, it is not known if the new hardware might uncover software defects. At the same time, it is possible that actual system software and applications could uncover hardware defects. For this reason, each system is tested under various load conditions and system configurations while running actual HP-UX and MPE/iX application programs and system exercisers. These efforts result in a system that has been designed to operate reliably in normal operating conditions as well as under extremes of environment.

Conclusion

The J/K-class family of workstations and servers takes a big step in the direction of converging HP's workstation and server lines. At the same time, the J/K-class provides leadership performance at exceptional value to computer systems users.

Acknowledgments

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we could design. Confirming the quality of their industrial design, the J/K-class systems won an award at the 1995 iF (Industrie Forum Design Hanover), the world's largest product industrial design forum.

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