

100VG-AnyLAN 15-Port Hub Design

Much of the intelligence and uniqueness of a 100VG-AnyLAN network is concentrated in the hub. Special repeater, transceiver, and end node chips implement the functionality of the HP J2410A AdvanceStack 100VG Hub 15.

by Lisa S. Brown

Hewlett-Packard has introduced several network products for 100VG-AnyLAN applications. Products available since mid-1994 include a 15-port hub, a 10Base-T/100VG bridge and SNMP management module, a 10Base-T/100VG ISA adapter card, and a 10Base-T/100VG EISA adapter card. These products were developed before completion of the IEEE 802.12 standard and are currently under modification to include changes that occurred in the standard between the time of product definition and the final version of the standard. Most notably, this includes changes to support token ring framing. Additional 100VG-AnyLAN products available in 1995 are a 10Base-T/100VG PCI adapter card, a multiport hub, a fiber hub, and a 10Base-T/100VG switch.

Much of the intelligence and uniqueness of a 100VG-AnyLAN network is concentrated in the hub. Therefore, this

article mainly focuses on the design of HP's 15-port hub, the HP J2410A AdvanceStack 100VG Hub 15 (see Fig. 3 on page 9). Some 100VG-AnyLAN-specific aspects of the other products are also explored in this article.

Hub Architecture

The key components of a 100VG-AnyLAN hub are the repeater chips and transceivers. In the HP 15-port hub solution, a microprocessor subsystem provides configuration and management functions. Fig. 1 is a block diagram of the 15-port hub.

The repeater chip implements the demand priority protocol, the signaling to receive and transmit packets, and the interfaces to the system. The system interfaces include a port

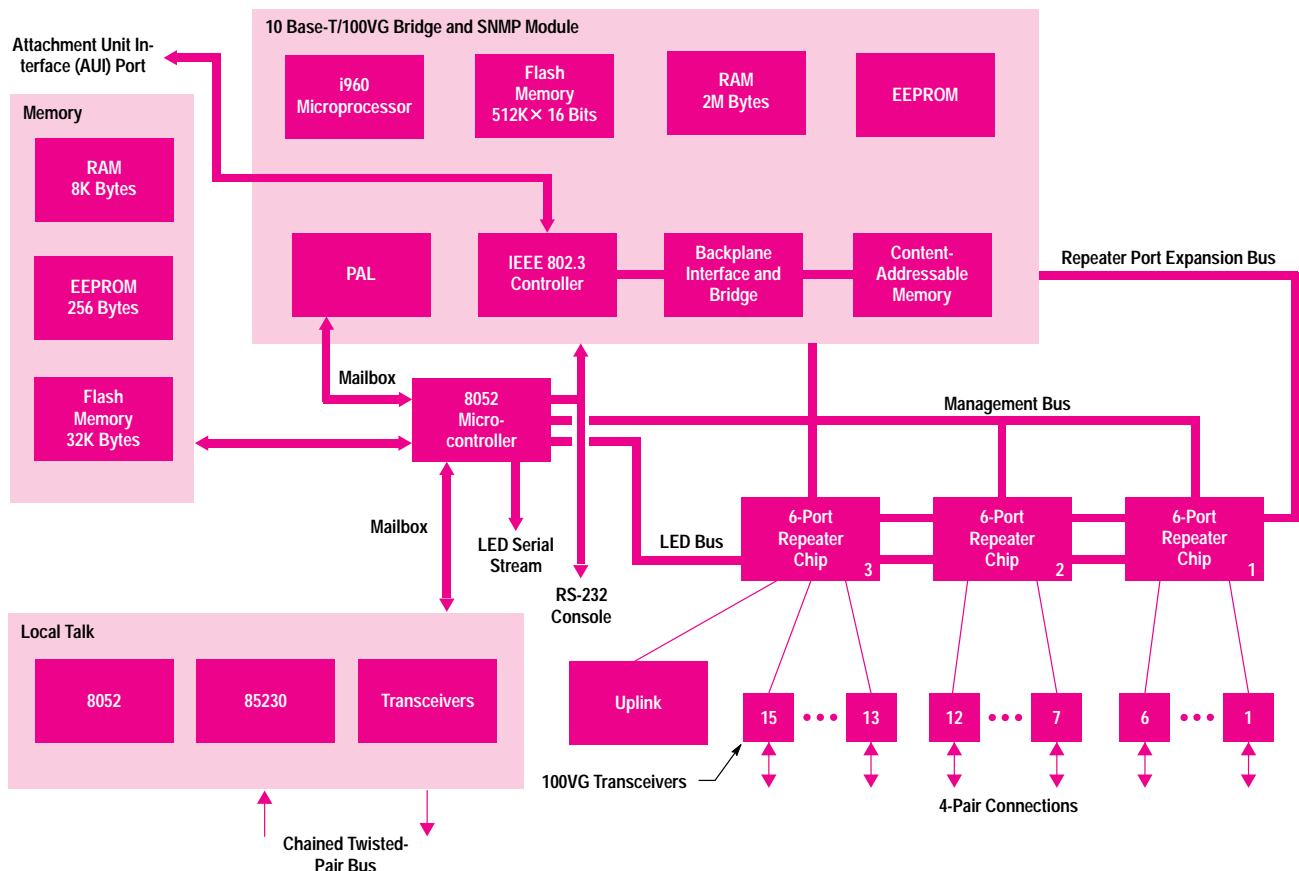


Fig. 1. Block diagram of the HP J2410A AdvanceStack 100VG Hub 15, a 15-port 100VG-AnyLAN hub.

expansion bus to connect several repeater chips into one logical repeater and an interface for network management functions, such as control and status information. The repeater chip is a six-port device that connects directly to six transceivers. Additionally, it has a single uplink port which also connects to a transceiver for use in a cascaded hub topology. For the 15-port hub, three repeater chips provide the 15 ports plus one downlink. The repeater chips act as one logical repeater through the use of the parallel expansion bus.

The transceiver chip implements the physical layer as described in the article on page 18. It is used in conjunction with a filter specially designed for use in 100VG-AnyLAN applications. The 15-port hub uses 16 transceiver chips, one for each of the 15 ports plus another for the uplink connection. The transceivers connect directly to the repeater chips.

Repeater Chip

The repeater chip logic was developed by HP and AT&T engineers in conjunction with the IEEE 802.12 standard development. It is now commercially available through AT&T as the ATT2R01. It implements the following functions:

- Demand priority protocol
- 100VG-AnyLAN RMAC (repeater MAC)
- Port expansion bus to connect multiple repeater chips together
- Interface to six transceivers for downlink ports
- Interface to transceiver for uplink port
- Packet buffer RAM
- Six-port CAM (content-addressable memory)
- Management bus
- Control and status registers
- Management counters.

Fig. 2 is a block diagram of the repeater chip's internal modules.

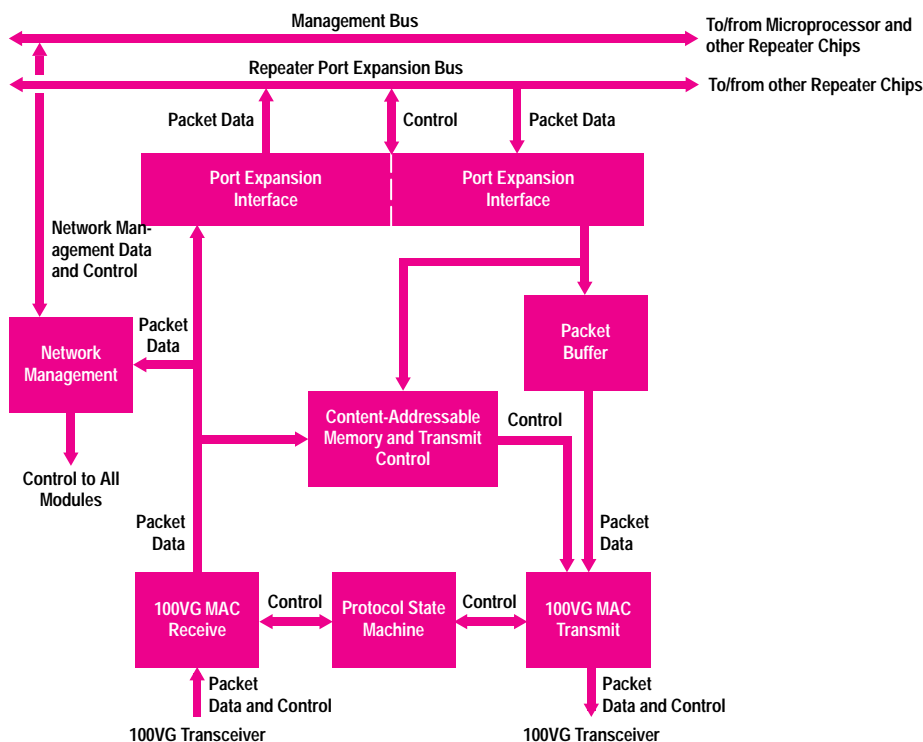


Fig. 2. Repeater chip block diagram.

A packet traverses through the hub in the following manner. The protocol state machine polls the ports as described in the article on page 13 and determines which port will receive a packet from its end node next. It initiates the proper tone sequence through the transceiver and readies the hub to receive a packet. When a packet is received, it first passes through the receive portion of the 100VG repeater MAC. The data is decoded as described in the article on page 27 and is passed through as bytes. Statistics for network management functions are gathered on the packet data and the packet is passed through to the port expansion bus. Each repeater chip on the port expansion bus loads the packet into its own internal packet buffer. The packet buffer is implemented as a RAM that is large enough to hold a maximum-length packet. The first six bytes of the packet are sent to the CAM. At this point, the destination address of the packet is decoded and compared with all entries in the CAM. The transmit control circuit decides which ports, if any, will transmit the packet to an end node. This is based on whether there was a match with a CAM entry, if the packet was a broadcast or multicast packet, or if any of the ports are configured as promiscuous. Finally, the packet passes through the transmit portion of the 100VG repeater MAC where it is encoded for transmission as described in the article on page 27.

The repeater chip also implements the training functions as described in the article on page 13. The protocol state machine controls the training sequence in a manner similar to its control of data transfers. As the training packets are received, the chip learns the status of the connected port and writes the source address into the internal CAM. It monitors the received packet, and if an error is detected the packet is not counted as a good training packet. Training continues until 24 sequential good packets are transmitted in each direction (see "Invalid Packet Marker" on page 41). If the

Invalid Packet Marker

When a packet has been received with an error, the invalid packet marker is appended when the packet is retransmitted to an end node or another hub in a cascaded network. Invalid packet marker information is useful during training and during normal packet transmission.

During training, if a packet is received at the end node with an invalid packet marker attached, this implies that an error occurred on the link where the packet was transmitted from the end node to the hub. If a packet is received at the end node with no invalid packet marker but an error is detected on the link, this implies that an error occurred on the link where that packet was transmitted from the hub to the end node. In either case, the packet is not counted as a good training packet.

During normal packet transmission, the detection of the invalid packet marker indicates that an error occurred in a link upstream from where the invalid packet marker was detected. For example, in a cascaded repeater network, the combination of receive error and invalid packet marker detection can be used to determine which link in the cascade produced the error. Excessive errors on any one link could indicate a marginal physical connection. A network administrator might then decide to examine the link to improve network performance.

link is faulty, the node will not pass training and the protocol state machine will pause the training attempt, wait one to two seconds, and then allow training to be attempted again.

The management bus allows the processor subsystem to access the repeater chips. In the network management block of Fig. 2 there are many control registers, which network management applications can set as needed. These include functions such as disabling ports, allowing for promiscuous ports, setting the hub in a bundled cable configuration, security functions, and a host of others. The processor also has read access to the CAM, which can aid network managers in building a map of the network. Additionally, there are sixteen 24-bit counters per port and a number of status registers in the network management block that can be read via the management bus. The counters accumulate statistics on each port such as the number of bytes received, good and bad packets received, errors, high-priority and normal-priority packets received, and others. The LED control interface is a simple bus that provides port status information to the 8052 microcontroller for driving the hub LEDs.

Transceiver Chip

The transceiver chip logic was developed by HP and AT&T engineers in conjunction with the IEEE 802.12 standard development. It is now commercially available through AT&T as the ATT2X01. It implements the following functions:

- 100VG-AnyLAN physical layer (PHY)
- Quartet signaling
- Adaptive equalization
- Timing recovery
- Data justifier
- Receive control signals (RCS) machine
- Transmit control signals (TCS) machine.

Further information on the functionality of the transceiver chip can be found in the article on page 18.

Network Interface Card Architecture

The key components in the network interface cards, such as the 10Base-T/100VG ISA and EISA adapter cards, are the 10Base-T/100VG end node chip, the external buffer RAM, the 100VG transceiver, and the 10Base-T transceiver. The 10Base-T transceiver is available commercially through a number of vendors and is used to provide a 10-Mbit/s interface to Ethernet networks. The 100VG transceiver is the same device that is used in the hub, the ATT2X01, and is described above. The 10Base-T/100VG end node chip is a new device to accommodate both 10-Mbit/s and 100-Mbit/s networks.

The 10Base-T/100VG ISA and EISA adapter cards are implemented with the same end node chip, which includes both the ISA and EISA system buses and the 100VG and 10Base-T interfaces to transceivers. An EISA workstation adapter card is available for HP 9000 Series 700 servers. The end node chip was developed by HP and AT&T engineers and is now commercially available from AT&T as the ATT2MD01.

The end node chip implements ISA and EISA bus interfaces specifically tuned to handle 100 Mb/s in the most efficient manner possible. The EISA interface provides bus mastering to allow 100VG servers to achieve LAN link rates with minimal CPU overhead. These bus interfaces comply with the industry-standard specifications for ISA and EISA machines.

Each end node device implements a 100VG module, which consists of a 100VG MAC and a protocol state machine. Through direct connection to a 100VG transceiver, this module generates and recognizes the appropriate tone sequences for training and data packet transmission. It converts internal chip bus data to 5B/6B encoded data and it decodes incoming 5B/6B data for the internal chip bus.

The end node chip also implements an interface to a 10Base-T network. It complies with all IEEE 802.3 specifications and connects directly to commercially available 10Base-T transceivers. This interface allows customers who may still be installing 10-Mbit/s networks to upgrade easily to 100VG-AnyLAN in the future without replacing adapter cards.

Other System Components

HP has also implemented a combination 10Base-T/100VG bridge and SNMP module. The module provides a connection from a 100VG network to a 10-Mbit/s Ethernet legacy network. It also has enough memory to load and run SNMP management functions for Ethernet and token ring networks.

This module slides into the hub and interfaces to the management bus and the port expansion bus on the repeater chip. The module has an i960 microprocessor and memory subsystem. The i960 is fast enough to process the counter information from the repeater chips in real time. The large 2M-byte RAM provides enough memory for both SNMP and bridging functions to run on the card.

This module also has an IEEE 802.3 controller chip to interface between 10-Mbit/s and 100-Mbit/s systems. Between this controller chip and the bus attached to the repeater

chip is an ASIC which controls the data and management information flow through the module. The module has direct access to the repeater data bus so that packet data can flow between the IEEE 802.3 controller and the 100VG network.

Acknowledgments

The introduction of the products discussed in this article was the result of tremendous effort and dedication on the part of

the 100VG-AnyLAN team in Roseville and Bristol. Through the well-orchestrated efforts of the research, design, manufacturing, and marketing teams these products were successfully introduced into the marketplace, thus establishing 100VG-AnyLAN as a viable low-cost, high-speed network for the applications of today and tomorrow.