Integrated Pin Electronics for Automatic Test Equipment

A single integrated circuit provides complete pin electronics for the HP 9493 mixed signal LSI test system. It contains a high-speed digital driver, an active load, a window comparator, and a parametric tester for setting a voltage and measuring current.

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As system designers increase the degree of integration of their systems, the functionality of large-scale integrated (LSI) circuits becomes more complex and varied. As a result, to verify the operation of an LSI chip on a wafer and to certify a finished device as a good one, two major requirements must be met. First, the LSI test system must be equipped with higher pin count capability to test these highly integrated devices. However, in meeting this first requirement, the size of the system may increase greatly and inhibit the use of peripheral equipment in confined spaces. Second, the test system must have much higher throughput to minimize the test cost, which must be included in the selling cost of the device. To meet this requirement, the test system itself needs improved functionality. One way to provide this is to equip the system with many more resources. However, this may also expand the size of the system.

The HP 9493 mixed signal LSI test system (Fig. 1) is designed to meet both of these requirements while retaining the ability to operate in confined spaces. The number of digital pins is increased to 256 pins, double the number of pins of previous products, while peripheral equipment can easily be used close to the test head, which is the same size as in previous designs.

Architecture

The models of the HP 9490 Series employ the concept of having in one tester all of the resources necessary to provide the functions of digital, analog, time, and dc measurements. This allows many kinds of test signals, especially digital signals such as address, data, clock, and control signals, to be generated or received at all pins at the same time.

Fig. 2 is a block diagram of the architecture of the HP 9493 LSI test system. The digital test subsystem consists of the sequencers, capture memory, timing vector generators, per-pin digital electronics, and per-pin dc electronics. The synchro pipe consists of special hardware to synchronize operation of the digital test subsystem and the analog test subsystems such as the arbitrary waveform generators and the waveform digitizers. The timing vector generator and the per-pin digital electronics are the per-pin digital test resources. Up to 256 digital channels can be installed.

The timing vector generators, which generate the programmed test patterns, are located in the test system cabinet. There is one timing vector generator for each pin. The same number of digital and dc pin electronics blocks, located in the test head, work independently in accordance with the

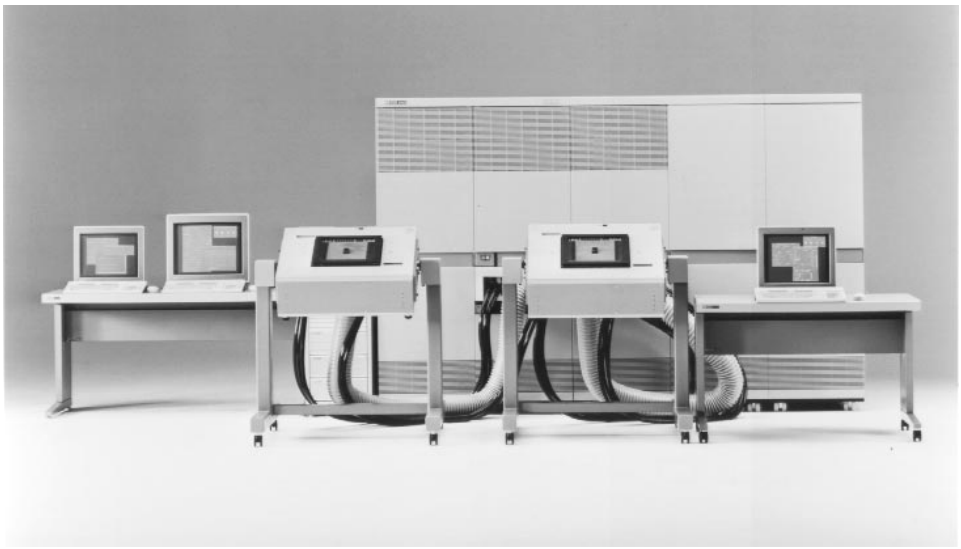

Fig. 1. The HP 9493 mixed signal LSI test system has up to 256 pins and dual slim-design test heads to allow use of peripheral equipment in confined spaces. The system shown has two test heads, three monitors, and 2½ equipment bays.

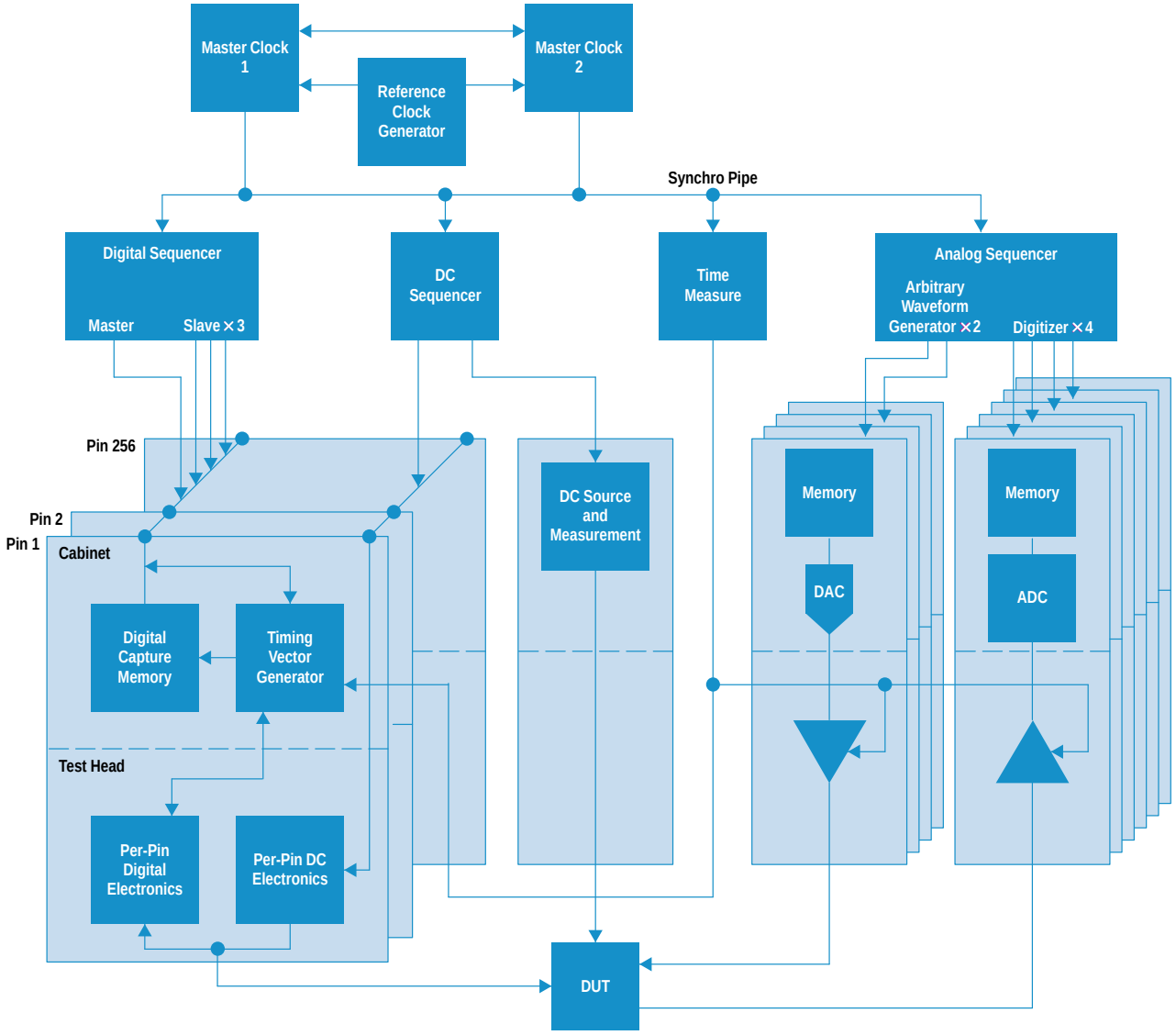

Fig. 2. Architecture of the HP 9493 mixed signal LSI test system. Each pin is equipped with both digital and dc resources.

defined patterns generated by the timing vector generators. The test head is the interface for test signals between the DUT (device under test) and the LSI test system. The pin electronics generate or receive digital signals and dc measurements at the front end of the DUT. This per-pin architecture gives the system improved throughput and the ability to interface various kinds of signals in the testing of LSI devices.

In addition to the pin electronics, many other hardware functions are built into the test head. The HP 9493 has a maximum capacity of 256 digital pins, and to reduce the size of the test system, the test head needs to be small. The test head was carefully designed to incorporate both small size and total functionality. This saves floor space and makes the system easier to handle.

Pin Electronics Functions

For LSI testing, the following functions are necessary:

- Driving formatted digital patterns to the DUT at arbitrary voltage levels
- Capturing digital patterns from the DUT and getting the results of timing measurements at arbitrary threshold levels
- Dynamically defining the load conditions at the output ports of the DUT
- VFIM (voltage force and current measure) and IFVM (current force and voltage measure), which are used for continuity tests, supply voltages, input currents, and leakage current measurements.

The pin electronics are responsible for performing these functions. The following circuits are necessary for providing various test capabilities in the HP 9493 mixed signal LSI test system.

- Pin driver. The pin driver generates the digital test signals to the DUT. The maximum data rate is 128 MHz.
- Pin comparator. The pin comparator receives the digital signals from the DUT and compares the signal levels with the reference voltage. The maximum data rate is 128 MHz.
- Active load. The active load receives and terminates the digital signals from the DUT. It also delivers the programmable current load to the DUT.
- VFIM. The VFIM function applies a constant voltage to the DUT and measures the current flowing into or out of the DUT.

- IFVM. The IFVM function applies a constant current to the DUT and measures the output voltage of the DUT. This function uses a successive approximation method and the programmable current of the active load.

We wanted to lower costs, increase functional pin capability, and double the pin count in the same test head volume. One way to achieve this is to combine functions within an IC chip and minimize the external components servicing the chip. Pin electronics have needed quite different technologies to perform their functions—one technology was used for the high-speed circuits (maximum frequency up to 128 MHz), while another was used for the precision dc circuits (resolution as high as 2.5 mV and 3 nA). We decided that the way to combine these functions was to design a custom monolithic analog ASIC (application-specific integrated circuit) that would include everything except the successive approximation circuits.

Pin Board on a Chip

This goal of combining the per-pin digital and dc electronics is realized in the PBOC, an acronym for pin board on a chip. The PBOC contains in a single chip a high-speed digital driver, an active load, a window comparator, a parametric tester for setting a voltage and measuring current, and control circuitry.

A functional block diagram of the PBOC is shown in Fig. 3.

The IC fabrication process was chosen for its device attributes of high speed and high voltage. Because of very low leakage requirements and variable chip temperatures, great effort went into minimizing all leakage paths, including device-to-device, device-to-substrate, and inversion paths. This was accomplished by using appropriate channel stops and metal guarding of the integrated components.

The objectives of the chip were:

- Low cost
- Eight channels on one board for a 256-pin system
- Minimum external components on the board
- Demanding linearity and accuracy specifications
- Compatibility with previous system designs.

Key features of the PBOC are:

- Pin driver, pin comparator, active load, and VFIM in one chip
- Operating frequency up to 128 MHz (64 MHz for large-amplitude pulses)
- Pin driver current to 35 mA
- Short-circuit protection
- Active load capability to sink or source 35 mA
- Two-nanosecond capture pulse width for the pin comparator
- Three VFIM ranges: 6 μA, 200 μA, and 6 mA
- On-chip measurement resistors
- On-chip range changing capability
- On-chip temperature compensation.

The main objective of the PBOC chip was to achieve a low-cost solution by including both analog and digital functions on one chip. The chip functions are linear within 0.05% to 0.1%, which simplifies calibration because it means that the functions only have to be calibrated at two points. This also lowers the cost of the system.

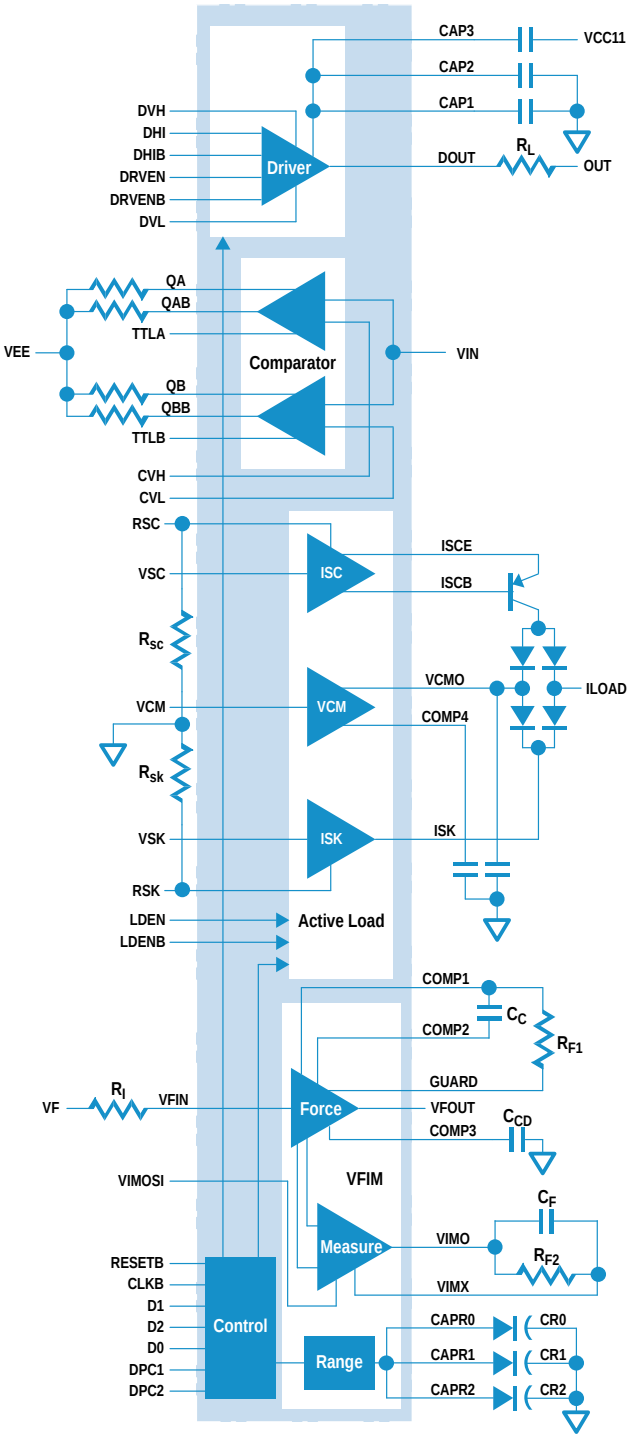

Fig. 3. Block diagram of the pin board on a chip (PBOC) integrated circuit.

Pin Driver. The pin driver drives the output terminal to either VOH or VOL according to the DHI and DHIB ECL inputs. A special override using TTL inputs sets the driver to either an on or an off condition by overriding the enable function. VOH and VOL are set by analog voltage inputs to DVH and DVL. Fig. 4 shows the functional block diagram of the pin driver.

The pin driver output can be put into a high-impedance mode by ECL inputs DRVEN and DRVENB in normal operation

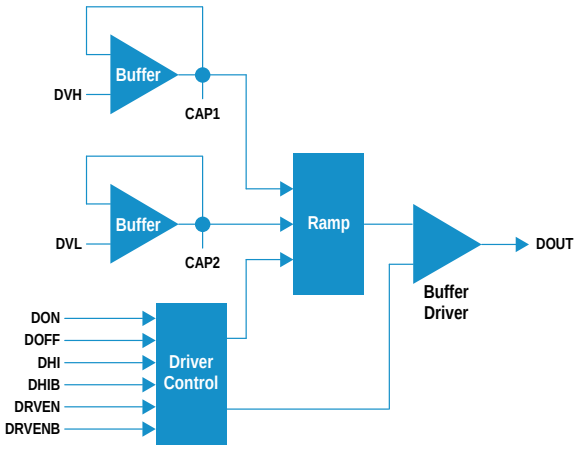

Fig. 4. Pin driver functional schematic diagram.

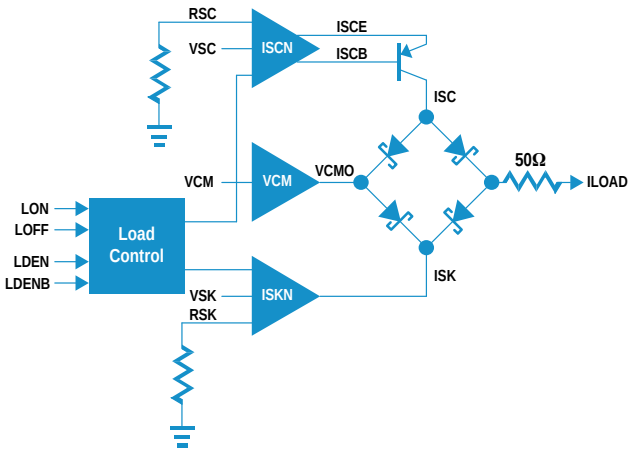

Fig. 6. Active load functional schematic diagram.

or by the internal DON and DOFF control functions, which are data inputs to the chip.

The pin driver provides a programmable output voltage of –2.1V to 7V with 12-bit resolution, 0.05% linearity, a 50-ohm output impedance, and a tristate output (high logic level, low logic level, high impedance). It can sink or source more than 70 mA for ac operation.

Pin Comparator. The pin comparator is a two-channel window comparator that compares the input signal against two reference voltages CVH and CVL. The ECL outputs (QA and QAB, QB and QBB) indicate whether the input voltage is higher or lower than each reference voltage. The outputs are balanced ECL10K-compatible signals driving 100-ohm twisted pair wires. TTLA and TTLB are TTL-compatible signals used for system setup calibration; their inclusion eliminates an external signal conversion circuit for the tester controller.

Fig. 5 is the functional block diagram of the pin comparator. The comparators have typical hysteresis voltages of 2.8 mV and typical offset voltages of 1 to 2 mV. The input range is from –2.1 volts to +7 volts. The comparator is capable of operating at over 128 MHz and has the ability to capture a pulse less than 2 nanoseconds in width. It has a combinational ECL logic output and an input impedance of 4 megohms.

Active Load. The active load loads the DUT with a specified current programmable from analog voltage inputs VSC and VSK. Fig. 6 is the functional block diagram of the active load.

If the voltage of the output terminal is higher than the commutation voltage (VCM), then the current programmed by VSK will be sunk from the DUT output terminal. If the voltage of the output terminal is lower than VCM, then the current programmed by VSC will be sourced to the output terminal. When the voltage at the output terminal is near VCM, then the output current characteristics show a resistive impedance of 50 ohms. The voltage-current relationship is shown in Fig. 7. Notice that when the voltage (VCM ±DUT voltage) is greater than the sink current times 50 ohms or less than the source current times 50 ohms, the output becomes high-impedance and the DUT sees only the current being applied.

The relationship between the source current (ISC) or sink current (ISK) and the current control voltage (VSC and VSK) is given by the following:

$$ISC = VSC/RSC \times G.ISC$$

$$ISK = VSK/RSK \times G.ISK,$$

where RSC = RSK = 4 kilohms and G.ISC = G.ISK = 20 (typical).

The active load's high-impedance function is controlled by the enable signals LDEN and LDENB, which are balanced ECL10K input signals. In normal operation, a signal using TTL inputs can override the enable signals and activate or deactivate the load circuit. This condition is used for setup

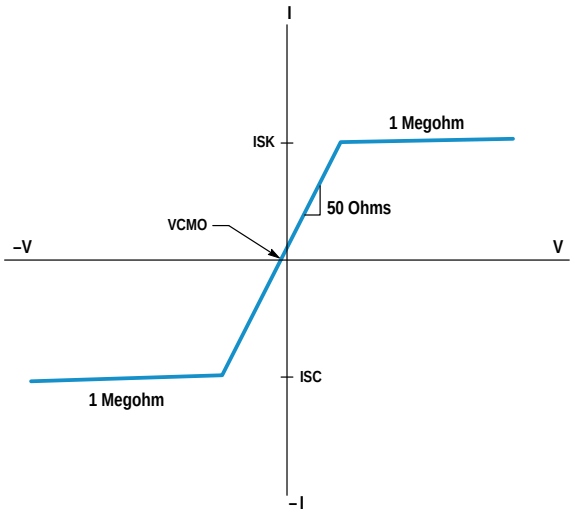

Fig. 5. Pin comparator functional schematic diagram.

Fig. 7. Active load voltage-current relationship.

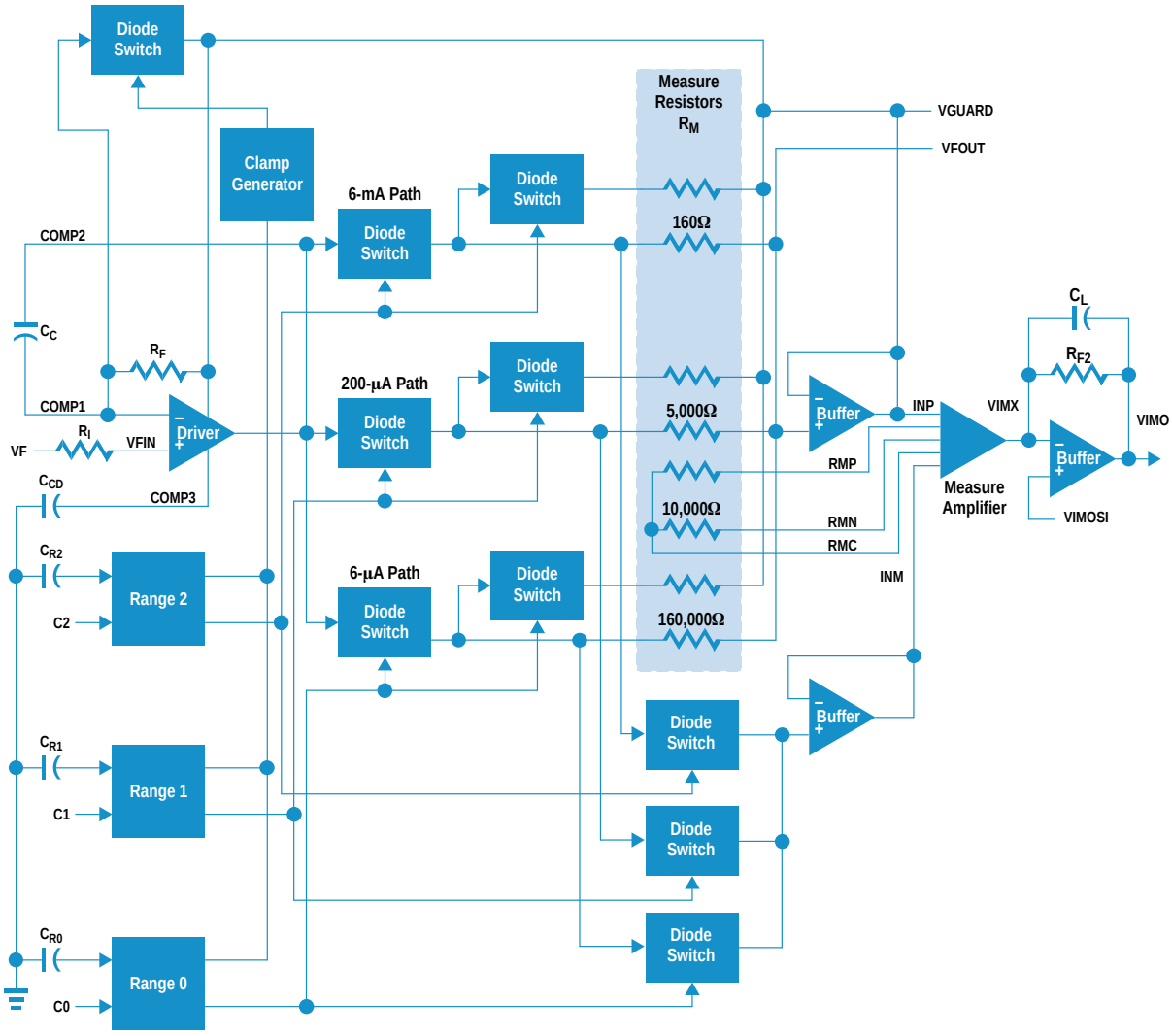

Fig. 8. Voltage force and current measure (VFIM) circuit functional schematic diagram.

and calibration. It is an abnormal operation in which excess power is dissipated on the chip. External to the chip, DRVEN and LDENB are connected together and DRVENB and LDEN are connected together such that only one circuit (driver or active load) is operational at any time.

In the off condition, the active load has a high-impedance output state and its power consumption is minimized.

The functions of the active load are realized with a few external components, including a p-n-p transistor, a Schottky diode bridge, two capacitors, and three resistors. The resistors are for setting source and sink currents and for adjusting the output impedance (50 ohms) in the resistive termination region.

The active load can sink or source from 10 µA to 35 mA with voltage compliance of −2.1V to 7V. It has 12-bit resolution, linearity of 0.1%, and an output impedance of 50 ohms. In the current sinking or sourcing mode, the output impedance is more than one megohm.

Voltage Force and Current Measure (VFIM) Circuit. The VFIM circuit is the portion of the PBOC that performs the precision voltage force, current sense, and current limiting functions of a voltage force driver measuring system. Design emphasis was on high resolution and accuracy spanning a range of force voltages from −2.1 to +7 volts and current sense ranges of 6 µA, 200 µA, and 6 mA.

Fig. 8 is the functional block diagram of the VFIM circuit. The VFIM input voltage VFIN, which is derived from the pin board circuitry, is an analog voltage source ranging from −2.1 to +7 volts. VFIN is buffered and applied to a current measure resistor R_M. A buffered loop compensates for the drop across R_M and produces VFOUT. The output current is measured by measuring the voltage drop across the terminals of R_M. Load current may flow in either direction through R_M. The resistor voltage drop is converted to a single-ended output, amplified to 4 volts full scale, and offset by +2.5 volts. The offset is needed to accommodate the operating voltage range of the pin board, which functions as both digital-to-analog and analog-to-digital converter. The result is VIMO, which ranges from −1.5 to +6.5 volts. A current limiter limits the output current to about 135% of each range.

The current measurement ranges are controlled by an internal register programmed by the test system controller. Three values of measure resistors are switched in and out of the circuit to achieve the three current ranges. The rate of transition between current measure ranges is controlled by external capacitors and the range blocks in Fig. 8. During range

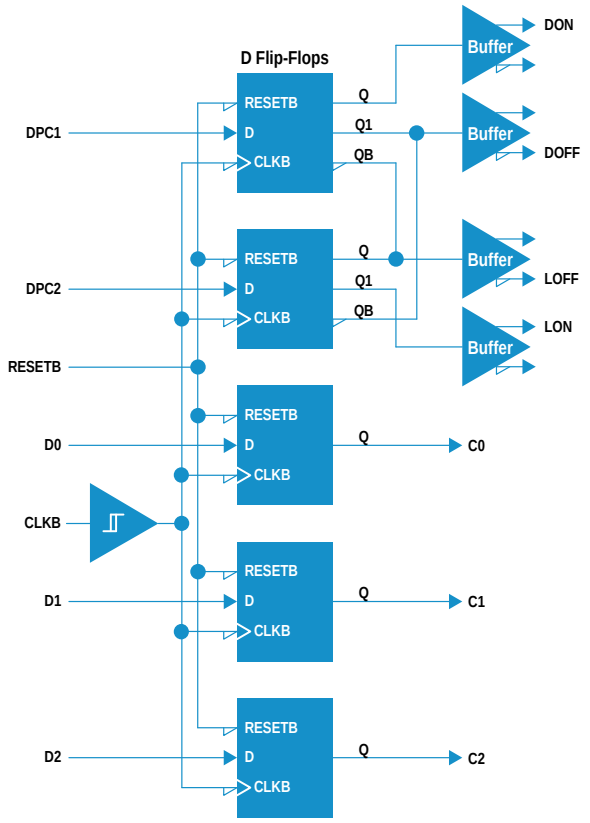

Fig. 9. Control circuit functional schematic diagram.

change transitions, the feedback resistor R_F is shunted by a low resistance, thereby decreasing the response time of the voltage force loop. This feature effectively reduces the height of the spike generated during range changes.

Nine external components are required for the VFIM function. Capacitor C_C is required for compensation and stability of the voltage force loop. Capacitor C_{CD} is required for stability of the drive amplifier. Capacitor C_L forms a low-pass filter in the current measure path. Resistor R_{F2} sets the gain of the current measure path. Resistor R_F is required for the voltage force feedback path and R_I is a matching resistor for the VFIN input. Capacitors C_{R0}, C_{R1} and C_{R2} are required to control the speed of the range changes.

The VFIM circuit can measure currents from 3 nA to 6 mA in three ranges of 6 μA, 200 μA, and 6 mA full scale. The circuit has voltage and current linearities of 0.05%, current common-mode rejection of 0.1%, and 12-bit voltage and current resolution.

Control. The control circuitry (see Fig. 9) controls the VFIM range changes and turns the driver and active load circuits on and off. The inputs CLKB, RESETB, DPC1, DPC2, D0, D1, and D2 are TTL signals. The data is captured in D flip-flops, which then logically control the functions of the chip.

The data input, reset, and clock signals are generated from other HP custom integrated circuits so as to minimize external components and reduce the pin count of the ICs used. This greatly reduces the pin board area needed for supporting eight channels.

Design Limitations and Challenges

The PBOC is used as a retrofit for an existing automatic test system. This constrained the design of the chip. It limited the choice of HP silicon fabrication processes and required the use of preselected automatic test system voltage supplies and conformance to preselected control conditions. It also required the use of diffusion resistors (nonlinear and temperature sensitive) and high-voltage biasing of components. Voltage breakdown limitations, leakage currents, and chip temperature excursions had to be dealt with.

Design challenges for the pin driver included a fast slew rate, accurate amplitude, a low-leakage tristate output, non-loading capacitance in the off state, an all n-p-n transistor push-pull design to minimize power consumption, and driver enable and disable capability.

The active load required conversion of input voltages to output currents, the ability to enable and disable the sink and source currents, the ability to monitor beta and compensate for base currents, and a linearized current range.

The comparator required fast capture times, small propagation delays, small input hysteresis voltage, and high input impedance.

The parametric tester required range changing without overshoot and within time limits, 3-nA sensitivity and accuracy maintained over chip temperature and voltage excursions, linearity of 0.05% for both voltage output and current measurement, and conversion of the current being measured to a voltage output.

Solutions and Implementation

The driver consists of buffer circuits for setting output levels and a ramp circuit to drive the output unity-gain buffer-driver. The buffer-driver consists of an all n-p-n transistor configuration. The push-pull effect is achieved by a variable pulldown current dependent on the state of the driver. A controlling circuit coordinates the ramp and push-pull capability of the buffer-driver.

The active load consists of transconductance amplifiers to change voltage inputs to known currents. These currents are then amplified with a gain of 20 to produce the ISC and ISK output currents. The circuit must attain its programmed output value from an off condition in 20 nanoseconds. To make this possible, the current amplifier capacitors are precharged so that the amplifiers reach the proper biasing voltages quickly.

The ISC output current needs to be corrected for the base current of the external p-n-p transistor. This is done by sensing the base current and reapplying it within the current amplifier. This corrects for gain variation, nonlinearity, and output impedance variation over the entire current range.

The ISK output current requires a similar correction for the internal n-p-n transistor. In addition, the current produced by the input transconductance amplifier is mirrored and then amplified 20 times. Additional correction is provided by a linearizing circuit. Again, the base current of the output transistor is sensed and reapplied within the current amplifier. This, as before, corrects for gain variation, nonlinearity, and output impedance variation over the entire current range.

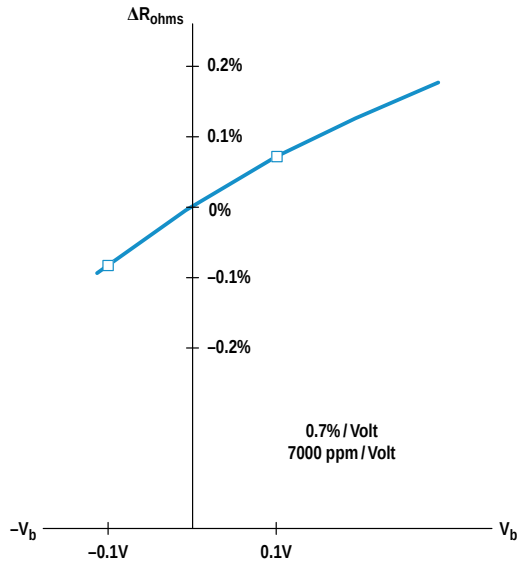

Fig. 10. Nonlinear diffused resistor curve, showing dependence of resistance on bias voltage.

The comparator requires input current cancellation to produce the high input impedance. This is accomplished by sensing a replication of the base current of the input transistor and subtracting it from the input node.

VFIM Current Measuring Resistors. One of the most creative solutions used in the PBOC was the design of the measure resistors R_M for measuring currents in the VFIM circuit. Diffused resistors are inherently nonlinear when used at different voltage bias conditions. Our objective was to produce resistors that have linearities better than 0.05% over their full operating current range, do not change value over the common-mode voltage range, and are not affected by leakage paths. The VFIM circuit measures currents from 3 nA to 6 mA and tolerates common-mode voltages from –3 volts to +8 volts about ground. For these ranges we needed to have 160-ohm, 5000-ohm, 160,000-ohm, and 10,000-ohm resistors that had matching characteristics over the operating current and voltage conditions and temperature variations.

Diffused resistor values vary with biasing potential (Fig. 10). By biasing a resistor so that one end is forward biased by a small amount and the other end is reverse biased the same amount with respect to the epitaxial island, the nonlinear effects are cancelled. The resulting resistor element has the same value whether it is operating at full current or zero current.

The solution is to bias a resistor element so that the potential at its center equals the resistor island potential as shown in Fig. 11. This makes the voltage excursion of the resistor ends about the center equal, so the resistor retains its value and linearity. The larger the number of elements used the more linear the resistor becomes. We settled upon five elements to produce each resistor. The resistors R_1, R_2, and R_3 are p-type diffused resistors in an n-type epitaxial island. The measurement resistor R_1 is symmetrically forward and reverse biased by no more than 0.1 volt. This minimizes the forward biased injection and the forward biased current is cancelled to a certain extent by the reverse leakage. Resistors R_2 and R_3 bias the island at midpoint. These resistors also bias the resistor island to the substrate potential to eliminate this leakage

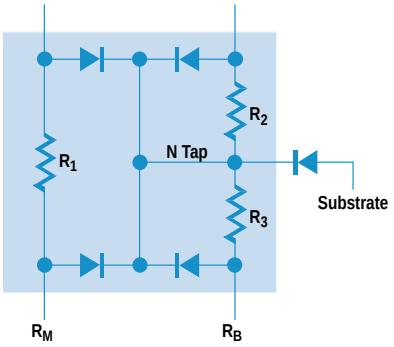

Fig. 11. One element of the measure resistor, showing parasitic diodes.

path. Fig. 11 shows the resistors and the resistor-to-island and substrate-to-island parasitic diodes.

The way the resistors are biased also helps eliminate leakage currents so that even at high temperature, the 3-nA capability is kept intact. Fig. 12 shows the five elements that make up a measuring resistor. They form a biasing string and a complete measurement resistor. Low-impedance drivers drive the bias string of R_2 and R_3 resistors which bias the R_1 resistors at midpoint and remove leakages to the substrate.

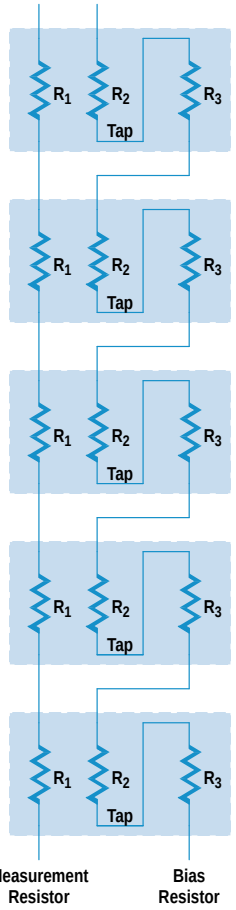

Fig. 12. The complete measure resistor consists of five elements in series. The R_2 and R_3 resistors form a bias string.

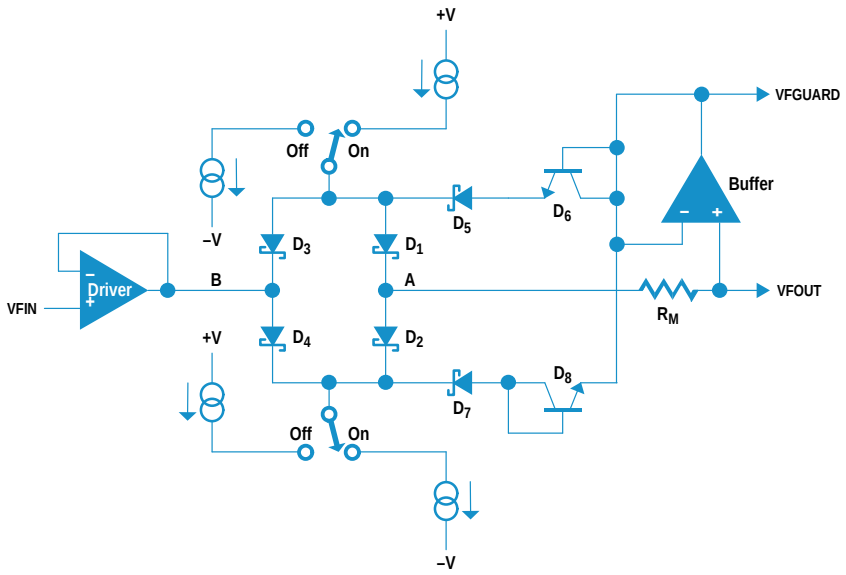

Fig. 13. Diode switch biasing.

The current measure amplifier of Fig. 8 has its resistors embedded in the measure resistor region so that mismatch and thermal effects are alleviated. These resistors also have five elements which are biased at their midpoints. This allows the measure amplifier output current at node VIMX to be an exact replica of the current being measured times some amplification factor determined by the resistor ratios. The output current sets up a voltage drop across an external precision resistor. The resultant voltage is measured by other analog-to-digital converters in the system.

The layout of the measure resistors ensures good thermal equalization between the elements. Good matching of resistors differing in value by 1000:1 was accomplished by series and parallel connection of resistor elements of the same width, as is customary in IC design. For example, 40 1280-ohm resistors are connected in parallel to make a 32-ohm resistor, while two 16-kilohm resistors are connected in series to make a 32-kilohm resistor. The 1280-ohm and 16-kilohm resistors are of the same type and width, differing only in length.

Leakage. Leakage is intolerable in a VFIM circuit of this type. Integrated Schottky diode bridge switches used for connecting the measurement resistors to other circuitry need to have very low leakage in the off state. When measuring current, two of the measurement resistors are connected to Schottky diode switches that are idle and reverse biased. The reverse-bias diode currents are large enough to affect the current measurements, especially at higher temperatures. In addition, the diode leakage current is a function of the reverse bias voltage. The matching of diode leakage is very good when bias conditions are equal.

Our approach was to back-bias the diodes by equal amounts so that leakage into a nodal point equals the leakage out of the node. The biasing scheme is shown in Fig. 13. When diodes D_1 and D_2 are reverse biased, they have equal bias potentials. This allows the current going into node A from diode 2 to equal the current out of node A to diode 1. The voltage needed for operation of the driver at node B is about 1 volt. Diodes D_5, D_6 and D_7, D_8 set up the equal biasing potential. Since no loading occurs from node A, VFOUT is not affected by these leakages.

Ranging Speed. To minimize or eliminate output voltage spikes during range changes and to minimize the range change time, the driver response speed needs to be increased during range changes. This is accomplished by shorting out the feedback resistor R_F during the range change period. A diode switch is used to short out the feedback resistor for the drive amplifier during the period of range change. Fig. 14 shows how the diode switch controls the voltage force driver. This allows the driver to react much faster by charging and discharging its compensation capacitor through the switch instead of through the resistor. The compensation capacitor C_C is quite large to provide high stabilization for all load conditions at VFOUT.

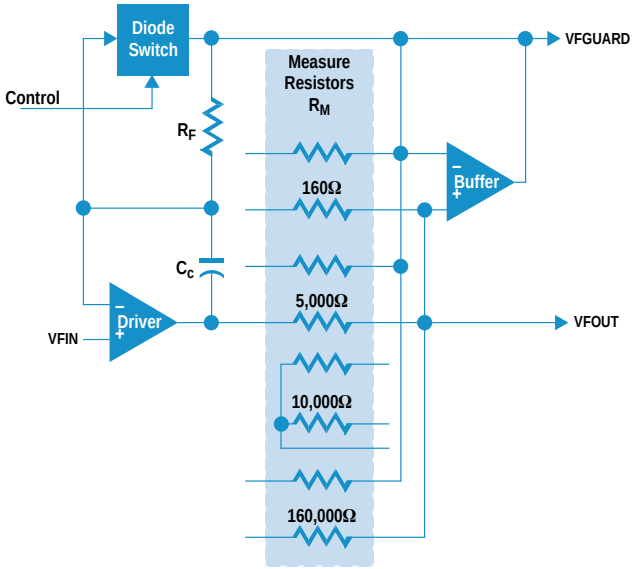

Fig. 14. Simplified schematic diagram showing the method of shorting the feedback resistor to improve driver response speed.

Conclusions

An integrated circuit was successfully designed and implemented to allow all of the pin electronics of the HP 9493 LSI test system to be included in one IC package with minimal external components. This makes it possible for a single board to hold eight channels, resulting in a compact test head size for a 256-pin system.

Acknowledgments

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