Manufacturing Test Optimization for VXI-Based Scanning Analog-to-Digital Converters

The high density of the hardware for the HP E1413 scanning analog-to-digital converter, the low cost per channel, and the wide variety of optional signal conditioning plug-ons require a production test strategy that is fast, flexible, and efficient.

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The wide range of features and functionality available in the HP E1413 scanning analog-to-digital converter, the flexibility provided by the signal conditioning plug-ons (SCPs), and the desire to occupy only a single VXIbus slot dictated a design that is complex and requires a high-density hardware implementation using double-sided surface mount technology with numerous fine-pitch components. Since the cost per measurement channel is aimed at being one of the lowest in the industry, the challenge to manufacturing was to develop prototype and production test and evaluation strategies that would be cost-effective.

Four project test goals were established at the start of the project to provide a low-cost test solution. The first goal mandated the use of existing test systems to reduce hardware development costs. The second goal was to reduce the cost of testing by removing defects as early in the production process as possible. The third goal was to reduce unit test times by a factor of three relative to similar products currently in production. The fourth goal was directed specifically at the SCPs. Because the SCPs have high production volumes (eight SCPs for each HP E1413 motherboard) compared to the HP E1413 motherboard and because of their low cost and relatively straightforward hardware design, the goal was established that the plug-ons would only be tested at one point in the production process.

Test Strategy

From these four goals the test strategy for the HP E1413 was developed. The need to remove process defects as early as possible in the production cycle requires testing the product at the completion of circuit board loading in the surface mount fabrication area (see Fig. 1). Testing at this point ensures that any process defects are removed as early in the manufacturing process as possible so that the product can function and be capable of being calibrated at final test. This test strategy enabled us to recognize another goal for the project and that is to refrain from duplicating tests in the surface mount and final test areas.

"Just-enough-test" is another test strategy that was implemented for the HP E1413. The aim of just-enough-test is to try to minimize test costs while at the same time ensuring that product quality is maintained at a high level. The simplest way to ensure high product quality is to test all of a product's specified parameters. Although this is certainly a safe and easy approach, it is also the least cost-effective in terms of development time and production test time. On the other hand, the lower the amount of test coverage the greater the risk of shipping a defect. Most test engineers probably tend to err on the side of too much testing, rather than too little, to ensure that as many defects as possible are found. With the HP E1413 we wanted to optimize the amount of testing. The HP E1413 test suites use several techniques to address this issue.

Reducing test costs requires not only that test run times be kept low, but that setup times be held to a minimum as well. To accomplish this, especially in the surface mount area, it was necessary to minimize the hookup time by requiring

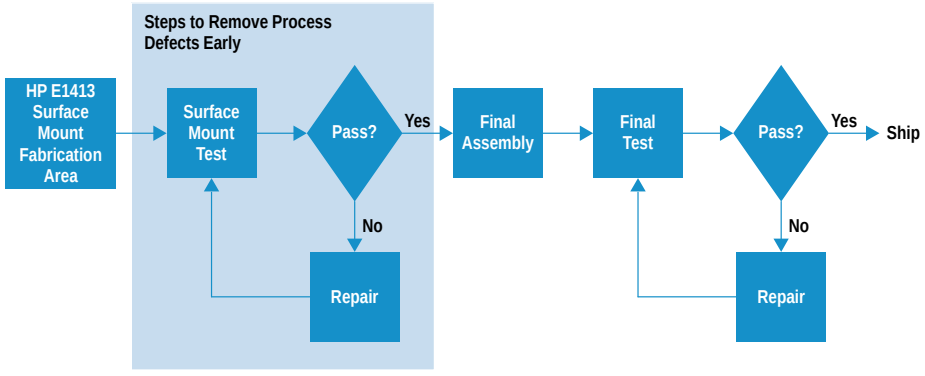

Fig. 1. The HP E1413 assemblies pass through a two-stage test and repair process. The surface mount test stage is aimed at detecting process defects and the final test stage is intended for calibration and performance verification.

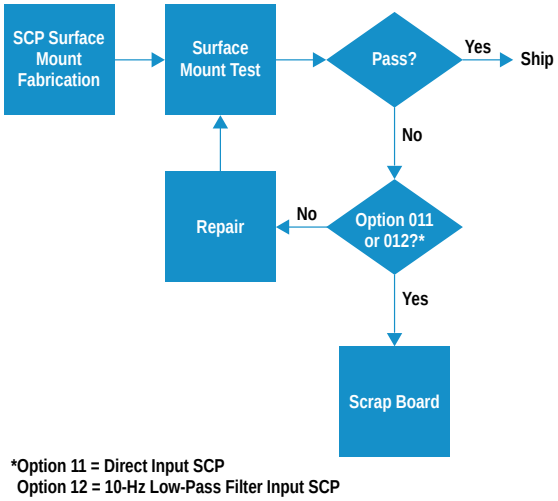

Fig. 2. The test and repair process for SCPs. Signal conditioning plug-ons are tested only after fabrication because they do not require final assembly or calibration.

front-panel connections only. To this end we needed access to major functional blocks within the product from either the backplane or the front-panel user interface. We decided that an internal analog self-test multiplexer that provides access to the internal functional blocks and is accessible from the front panel would be the best solution.

While the goal of doing a single manufacturing test for the signal conditioning plug-ons was easily met, the test process for the plug-ons still required a test set with a minimum amount of components and the shortest possible repair times. An analysis of the cost of repair versus the factory cost of various SCPs showed that for the lowest-cost boards that did not pass the tests, it was more economical to discard such boards rather than repair them (see Fig. 2). This was a major change in our old manufacturing paradigm in which all failures had to be repaired.

Implementation

Having defined the test goals and strategies and adding the goal that tests would not be duplicated from one area to another, we were able to split the test development workload between two test engineers and reduce the product test development time.

Early identification of test requirements was given high priority because of the need to identify any potential hardware additions, such as the analog self-test multiplexer, which might be required for manufacturing test. This early identification allowed these additions to be incorporated into the layout of the printed circuit board during the initial design phase.

We decided early in the design phase that the self-test multiplexer would need independent measurement capability so that it would not have to rely on other internal circuits for confirmation of functionality, and that it would be able to interface with the internal ADC for the built-in self-tests. These two paths for routing the multiplexer's output are necessary because there are two different problems to solve. First, at power on the self-tests are looking for process problems such as missing or backwards parts, and later, during

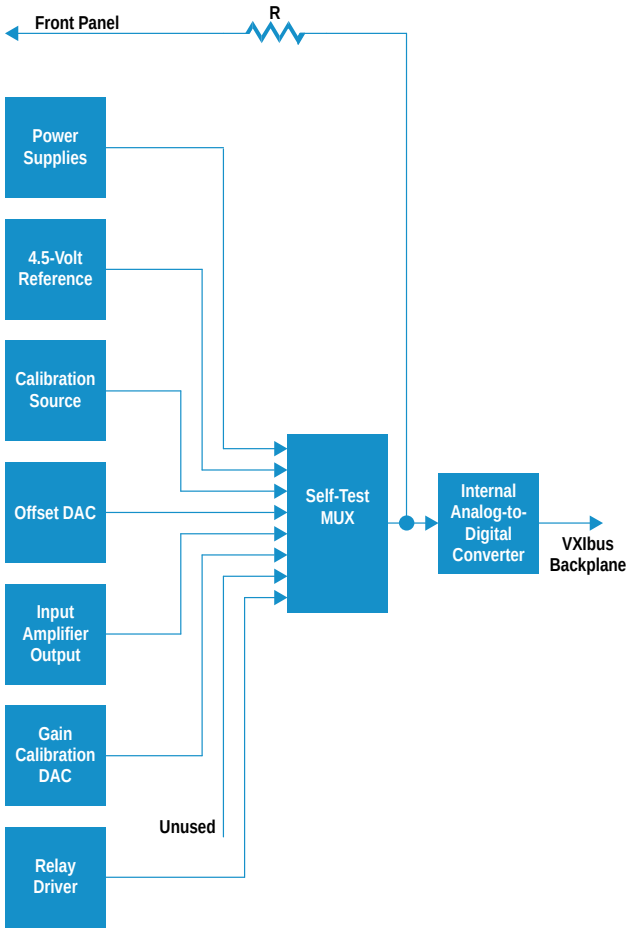

Fig. 3. Inputs to self-test multiplexer.

field verifications the self-tests are looking for component failures.

During surface mount production testing the accuracy of an external voltmeter is relied upon to verify important circuit parameters, while the internal ADC is used for built-in self-test measurements. Thus, from a design point of view it was necessary to determine which circuits would be critical to measure and whether the measurements could easily be done on the HP E1413 printed circuit board. The major implementation concerns were parts cost and printed circuit board area. The density of the HP E1413 does not allow much room for extra self-test parts. An eight-channel multiplexer was selected as a compromise between test coverage and printed circuit board area. Fig. 3 shows the major blocks that provide input to the HP E1413 self-test multiplexer.

The expanding kernel approach* has been used for structuring the tests throughout the development of all of the test suites. The first test is designed to measure several critical internal power supplies with one measurement. This "one measurement" constraint was mandated by the limited number of inputs to the self-test multiplexer.

Some of the power supply buses used in the HP E1413 are connected directly to the mainframe power supplies, while

* The expanding kernel test methodology selects a minimum set, or kernel, of circuitry that is assumed to be functional and then verifies the remaining circuits in sequence, building on the kernel.

others are derived from those supplies. It was decided to test only the four power supplies derived from the mainframe supplies. The test assumes that the five mainframe power supplies are functioning and so they are not tested. The hardware implementation consists of a wired-OR connection of the derived power supplies to one input of the self-test multiplexer.

The next major functional blocks tested with the self-test multiplexer are the outputs of the input amplifier, the reference voltage for the ADC, the calibration source, and the DACs used for calibrating the HP E1413.

The DACs for the calibration source, gain, and offset corrections are tested by setting the conditions of all zeros and all ones plus zero-ones and one-zeros combinations to test for stuck high or stuck low bits, while the input amplifier is tested for all input conditions, including overload (by using an external source).

The self-test MUX also verifies the relay drivers. The output of each relay driver is wire-ORed through a resistor to one of the MUX inputs. The drivers are activated one at a time, and since one side of the relay coil is hardwired to ground with the driver acting as an active pull-up, the relay driver is able to verify that the relay coil is activated.

The seven self-test multiplexer channels (the eighth is unused) in conjunction with the built-in self-test proved to be more than adequate to verify the performance of the HP E1413 before final calibration and test.

The final test of the HP E1413 is made up of two sections: calibration and analog verification. The calibration section performs a full-scale and tare offset calibration* for each of the 64 channels and the internal current source. It also verifies all of the internal calibration constants to ensure that they are close to their nominal values. Any deviations would indicate a possible fault.

Final Test Optimization

To meet the goal of a threefold improvement in analog verification times over other similar products, it was necessary to implement a set of stringent test selection criteria. Traditional test techniques usually extract only one bit of test data for each measurement. A traditional test suite was generated for the analog portion of this product and a list of these tests is shown in Table I along with their test times.

The test data yield can be increased by selecting tests that verify a number of different parameters at one time, or by selecting tests that verify a block of ports simultaneously. As the test data yield is increased, the length of the test suite will decrease. This occurs because more test data is extracted from each test, resulting in fewer tests being required to provide adequate test coverage. Also, since the number of executable tests is decreased, test times should decrease as well.

A good example of a high-data-yield test is the discrete Fourier transform (DFT). An analysis of the results of a DFT test can give information on noise, signal-to-noise ratio, aperture uncertainty, number of effective bits, harmonics and harmonic distortion (magnitude, frequency, and phase), integral and differential nonlinearity, missing codes, and spurious responses. While there are other methods of measuring these parameters, they would all require additional data processing and in some cases additional test system hardware. The DFT is able to measure all of these parameters with just one hardware configuration, a sine wave source and a low-pass filter, and one software analysis routine.

Table I
Traditional UUT Verification Test Suite

Test	Test Time (minutes)
Built-in test	3.0
Offset and noise (1 channel, 5 ADC ranges)	0.9
Offset and noise (64 channels, lowest ADC range)	1.2
Full-scale gain (1 channel, 5 ADC ranges)	1.3
Full-scale gain (64 channels, highest ADC range)	3.2
Integral linearity (5 ADC ranges)	5.0
ADC bandwidth (1V range)	0.6
Number of effective bits (DFT) (1V range)	0.9
Overload detection/recovery (1V range)	0.5
MUX switching speed (64 channels)— T_{on} and T_{off}	12.2
Total Test Time	28.8

The DFT test can also be used to verify the FET multiplexer of the UUT (unit under test), which would normally be verified by measuring such parameters as switching times and leakage currents for each of the 64 channels. While these parameters might be of some interest in themselves, the primary concern is whether the FET MUX is able to scan the input signals at the specified rates and accuracies.

If the main performance objective of the MUX is to maintain a specified measurement accuracy at the maximum scanning rate, then this is the manner in which it should be tested. In production testing the HP E1413, the 64 MUX channels (eight channels per SCP and eight SCPs per HP E1413) are connected in parallel to a sine wave signal source and a continuous scan is initiated that sequences through all of the channels at the maximum scanning rate. This results in a digitized waveform in which successive data points are measured on different channels. Any dynamic switching problems that are present will show up as an elevated noise floor of the DFT.

Even traditionally slow tests such as gain and offset can be redefined to improve their efficiency. Rather than measuring the full-scale gains of each channel one at a time (e.g., 100 readings at channel 0, 100 readings at channel 1, and so on), a scan list can be set up to scan all 64 channels sequentially (e.g., loop 100 times taking one reading at each channel during each iteration). This entails only one configuration for the UUT and the application of the same input to all 64

* A tare calibration measures and corrects for the customer's and the HP E1413's offset errors on each channel. Tare calibration is described in the article on page 25.

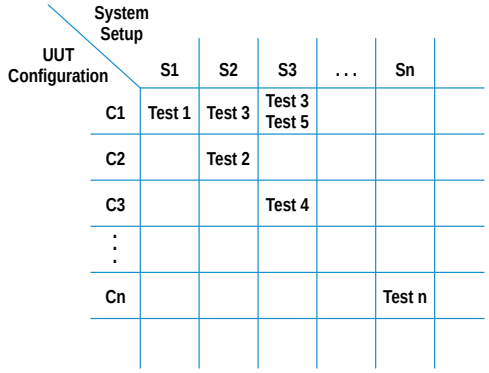

Fig. 4. System setups and UUT configurations are combined with their respective tests to indicate tests that share common data needs. In this figure tests 3 and 5 can both use the same data defined by system setup S3 and UUT configuration C1.

channels of the UUT. The data for all 64 channels is transferred to the computer in one large block rather than in 64 smaller blocks. This reduces much of the software overhead associated with computer I/O operations. The data for the 64 channels is sorted by channel and only the worst channel's results are reported to the user for pass/fail determination. Only in the event of a failure is all of the data returned to the user.

This scanning technique is used for almost all of the HP E1413 analog tests. The value of this approach is not just reduced test times. During the development phase of the product, several design and component problems were encountered that only manifested themselves during the scanning tests.

Data Duplication

Another area of opportunity for increasing test efficiency came from the recognition that many test suites contain duplicate measurement data. Since source setup and settling times are major contributors to test times, any duplication of measured data results in longer test times. For example, the data required for an integral linearity test includes plus or minus full-scale data, zero data, and other intermediate points. One data set can therefore be used for computing linearity as well as gain, offset, and noise.

Duplicate data sets can easily be seen by creating a table of system setups and UUT configurations as shown in Fig. 4. Grid locations that contain more than one test number indicate that duplicate data is being taken and are opportunities for test consolidation. This approach leads the test engineer to consider the test process from the point of view of data acquisition rather than test results.

Test Statistical Quality Control Process

Extensive use was made of audit and depend test types to provide additional data for statistical quality control (SQC) purposes and repair technicians. These tests were designed to verify the UUT's performance in the traditional manner, one channel at a time.

Audit tests are tests that are executed on samples of the production UUTs to ensure that the new test techniques, such as the scanned gain and linearity tests, are adequately verifying the UUT's analog performance. The test results are reviewed on a periodic basis to determine whether or not tests should be added to or removed from the audit list.

The tests classified as depend types are executed if a specified preceding test failed. The purpose of depend tests is to provide the repair technicians with additional data to aid them in locating the cause of a failure.

Fuzzy Logic Data Analysis

The HP E1413 project was also used as a test bed for a fuzzy logic tool that was developed as an alternative to statistical methods to aid in the analysis of prototype and production test data.[1] The fuzzy logic tool is especially useful for summarizing the test results from small quantities of products, even a single unit.

The fuzzy logic tool attempts to quantify the test results for a single UUT by emulating the analysis patterns of a human test engineer. The results of each test are graded by their proximity to nominal values and by their weight, or relative importance. The grading is accomplished by normalizing each test result relative to the test specification, determining its fuzzy equivalent, and then combining all of the results via a fuzzy rule base to yield a fuzzy conclusion and a fuzzy logic figure of merit, or fuzzy index. Each test can be weighted by applying a fuzzy logic hedge, which includes terms such as "very" or "slightly" that allow a specific test result to be emphasized or deemphasized relative to other tests. The ability to weigh the test results is of particular importance because it allows more emphasis to be placed on test results that are expected to be more accurate than others. Calibration point testing represents tests of this type.

The fuzzy index, which is much like a weighted average, indicates the overall performance of the UUT. This result can be used to compare multiple UUTs tested under the same conditions or to compare one UUT's performance over changing environmental conditions.

The fuzzy index has also proven to be a useful metric for tracking prototype development. The overall performance figure should show improvement relative to the product's target specifications as development progresses and circuit design is refined.

Signal Conditioning Plug-ons

The lack of any necessity for final assembly and the ability of the HP E1413 to compensate effectively for gain and offset errors within the SCPs enabled a test-it-once solution to be implemented during surface mount technology fabrication. The same testing techniques were implemented for the SCPs as are used for the HP E1413 motherboard.

Since the SCPs are designed to operate as part of the HP E1413 motherboard, either a known good HP E1413 is required as a test fixture, or a custom test fixture is necessary. The strategy chosen is to use a known good HP E1413 motherboard because it is the simplest and most cost-effective solution compared to a custom test fixture. It also allows a simpler maintenance and upgrade strategy.

To enhance the flexibility of the test process, the test is designed to allow operators to mix and match SCPs on the test motherboard. The software is designed to interrogate each of the eight plug-on locations to determine if an SCP is loaded and if so, its type, and then to load the appropriate test program.

Conclusion

The result of these efforts is a test process that minimizes throughput in production and at the same time ensures that all product specifications are met. All of the project goals were met, including those of no process defects at final test and the 3× reduction in test times as summarized in Table II.

Table II
Optimized Verification Test Suite

Test	Test Time (minutes)
Built-in test	3.0
Overload detection and recovery	0.5
MUX, ADC, bandwidth FFT (64 channels in parallel)	1.5
Integral linearity, gain, offset, noise (64 channels, 5 ADC ranges)	6.5
Total Test Time	11.5

Reference

1. B Kolts, "Fuzzy Logic Improves Small-Lot Data Analysis," *Evaluation Engineering,* Vol. 30, no. 5, May 1994, pp. 30-36.