High-Throughput Amplifier and Analog-to-Digital Converter

High system throughput in converting analog signals to digital format in the HP E1413 is achieved by not relying on downstream digital processing hardware and software to compensate for analog anomalies and instabilities.

by Ronald J. Riedel

The amplifier and analog-to-digital converter (ADC) section of the HP E1413 provide the interface between the multiplexed analog signals from the signal conditioning pods and the digital world. Some of the functionality provided by this section includes:

- Accepting input signals ranging from a few microvolts to ±16 volts
- Correcting for gain and offset errors on a channel-by-channel basis
- Acquiring each multiplexed signal in turn and settling to full accuracy with no memory of the previous channel, even if the previous channel was severely overloaded
- Converting the analog input to a 16-bit digital number with commensurate linearity and accuracy
- Providing a voltage reference, current source, and calibration voltage source for use by the ADC and the rest of the card.

A key contribution to the overall system throughput and customer ease of use of the HP E1413 is that the above functions are provided smoothly and accurately without the need for further error correction by the downstream digital hardware and software. We resisted the temptation to rely on digital processing to compensate for analog anomalies and instabilities, even though this approach would have saved money and time on the analog design.

Fig. 1 shows the block diagram of the amplifier and ADC section of the HP E1413.

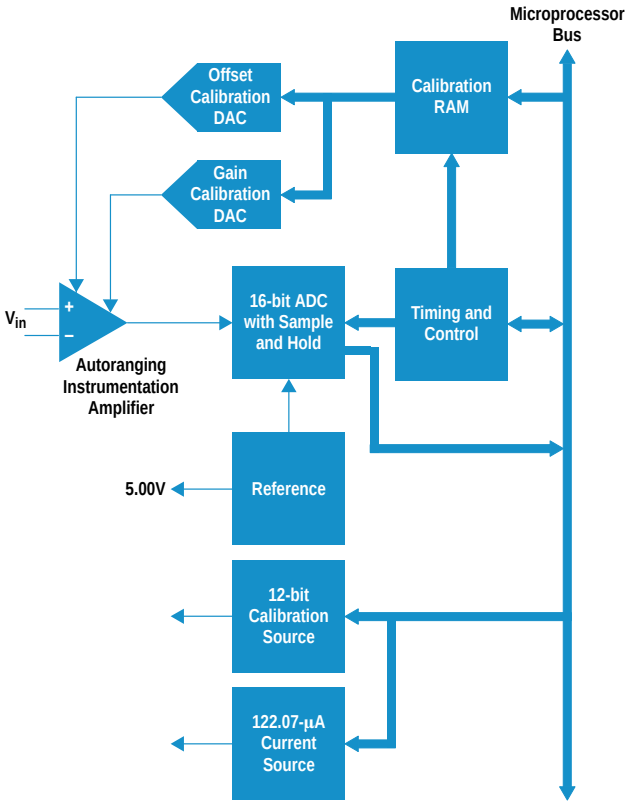

Fig. 1. HP E1413 analog-to-digital converter block diagram.

Amplifier Design and Performance

The performance requirements of a high-resolution, high-speed scanning voltmeter such as the HP E1413 dictate some fairly challenging criteria for the main input amplifier of the ADC section. In fact, more than any other single piece of analog circuitry, the amplifier can define and limit the performance of the entire system. Some of the design requirements for this amplifier included:

- Fast settling time. To achieve full accuracy on a low-level channel following a high-level channel while scanning at 100 kHz, the amplifier must settle to 10 µV after an input of 16 volts, in 10 µs. This represents settling to better than 1 ppm in less than 10 µs.
- Fast overload recovery. So that an overloaded channel does not affect measurements on subsequent channels in the scan list, the amplifier must recover from overload quickly and cleanly. Our goals were recovery to linear operation in less than 1 µs and full settling in less than 10 µs.
- Fully balanced differential inputs. The HP E1413 resolves signals down to 2 µV with a "straight-through" signal conditioning plug-on. However, because of the high conversion rate we cannot use the normal noise reduction techniques of integration, filtering, and averaging. Fully balanced differential inputs are necessary to achieve adequate noise rejection and to eliminate ground loops from the measurement path. The straight-through SCP is described in the article on page 9.
- High common-mode rejection ratio. A high common-mode rejection ratio is necessary for good noise rejection and to allow measurement of sensors such as strain gauges, which typically involve a small differential signal (in the order of

millivolts) impressed onto a large (several volts) dc common-mode signal. Our design goal for common-mode rejection ratio was greater than 120 dB up to 60 Hz on the most sensitive (62.5 mV) voltage range.

- Low noise. Once again, standard noise reduction techniques of averaging, filtering, and integration are not normally available in high-speed scanning applications. Thus, a low-noise amplifier is essential if the full resolution of the HP E1413 is to be usefully realized. Our design goal was a noise level of less than 5 μV rms referred to the input of the amplifier.
- Autoranging with no loss of scanning speed or accuracy. In a scanning system, a customer may connect channel 1 to a thermocouple generating 1 mV and use channel 2 to monitor a 10-volt power supply. The amplifier must be able to range between these two signals at speed, without degrading system accuracy. Also, many customers may be unsure as to the exact voltage expected on a given channel. Autoranging allows them to let the HP E1413 select the optimum measurement range on a sample-by-sample basis. The customer's measurement task is greatly simplified if there is no need to give up speed or accuracy to use autoranging.
- Linearity and accuracy commensurate with a 16-bit system. Our goal was to provide 0.01% overall system accuracy.
- Good dc performance. For all of its high speed, the HP E1413 still has the requirement to be a good dc voltmeter. Thus, low drift (< 10 μV/°C) and low bias currents (< 1 nA) are essential.
- 16-volt differential and common-mode input range. For many applications, particularly in the automotive world, the standard input limits of ±5 volts or ±10 volts seen on many high-speed ADC systems simply are not adequate. We set a goal to provide a full ±16-volt input range so that 12-volt and 14-volt buses can be measured without the use of cumbersome speed and accuracy limiting attenuators.

While none of the performance requirements mentioned above are particularly difficult to achieve in isolation, satisfying all of them simultaneously proved much more challenging. Initially, it seemed to make sense to attempt to implement the amplifier using the classic three-operational-amplifier circuit shown in Fig. 2 with off-the-shelf parts. However, an exhaustive search of manufacturers' catalogs soon revealed that commercially available opamps couldn't do the job. All the parts we considered suffered from one or more of the following limitations: poor settling time or overload recovery, excessive input bias currents, inadequate common-mode rejection ratio, or limited input voltage range.

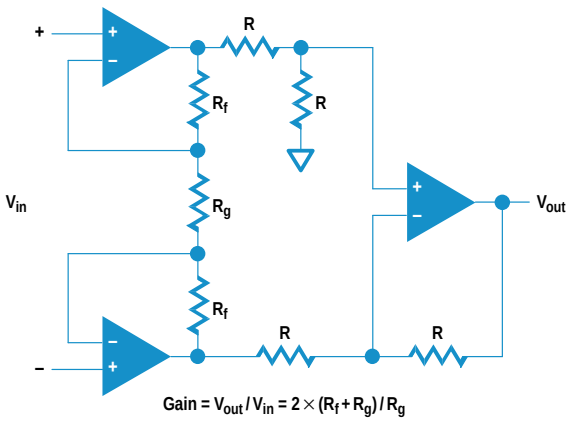

Fig. 2. Classic three-opamp instrumentation amplifier.

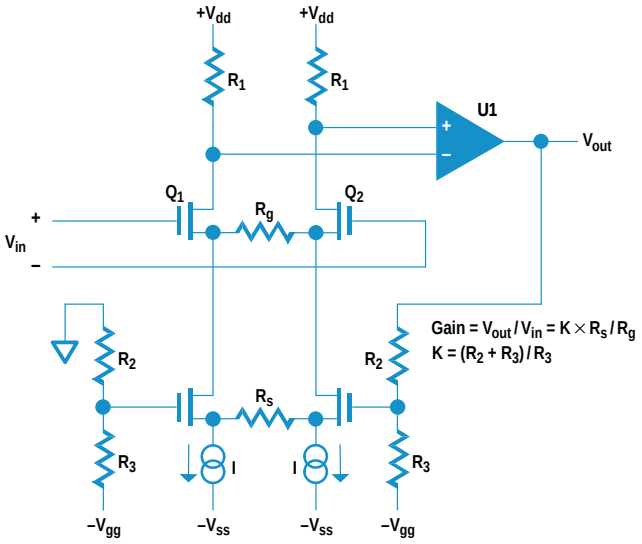

Fig. 3. Basic current-mode instrumentation amplifier.

Another avenue, which involved using a monolithic instrumentation amplifier, was also considered. However, these parts typically require a switch with low resistance and low capacitance such as a relay to switch the gain accurately. This made them useless for meeting our autoranging requirements.

For these reasons, we determined that a discrete amplifier design would be necessary. The amplifier uses a classic current-mode instrumentation configuration, with a special gain switching circuit that is both fast and accurate. It implements overload clamping in such a way as to greatly reduce recovery time by eliminating internal saturation and nonlinear operation. Finally, the amplifier provides for "on-the-fly" gain and offset correction on a per-channel basis so that the ADC sees an accurate signal for conversion. This eliminates downstream time-consuming digital processing to correct the readings for gain and offset errors and allows the full range of the ADC to be used for measurements.

Fig. 3 shows a simplified schematic of the basic current-mode instrumentation amplifier. Because of the feedback action of opamp U1, matched input FETs Q_1 and Q_2 operate at constant, equal currents. Thus, the voltage impressed across R_g is equal to the input voltage with a common-mode shift equal to the V_{gs} of the input FETs. The current through R_g becomes V_{in}/R_g. This current must flow back through R_s to keep the lower current sources satisfied. The output of U1 will servo to make this happen, resulting in an input/output transfer function of:

$$V_{out}/V_{in} = K \times R_s/R_g$$

where

$$K = \frac{R_2 + R_3}{R_3}$$

Thus, the amplifier gain is controlled entirely by the value of K and the ratio of R_s to R_g. K and R_s influence the bandwidth

Binary Ranges Speed Processing

Referring to Fig. 3 in the accompanying article, for the HP E1413 R_s is fixed at 600 ohms. R_g has values of 55.555 ohms, 222.22 ohms, 888.8 ohms, 3.555 kilohms, and 14.222 kilohms, and K = 6.6667. This gives amplifier gains of 72, 18, 4.5, 1.125, and 0.28125. Since full-scale at the ADC is 4.5 volts, this gives full-scale input voltage ranges of 62.5 mV, 250 mV, 1 volt, 4 volts, and 16 volts. At first glance, these full-scale ranges may seem odd; why not choose a more common 1,3,10 or 1,2,5,10 sequence? These values were not chosen for ease of human comprehension, but to interface well to a binary number system. The ranges have full-scale values of 2^n, where n has values of –4, –2, 0, 2, and 4, so the digital reading from the ADC maps directly into the mantissa of an IEEE floating-point number with no further processing required beyond right or left shifts for normalization. This greatly relieves the burden on the downstream processing hardware, freeing it for more productive tasks.

and stability of the amplifier and are normally not varied for a particular design. R_g is used to set the gain because, to a first approximation, bandwidth, settling time, and stability are independent of R_g.

Also notice that ideally the amplifier has no gain for common-mode signals, resulting in a theoretically infinite common-mode rejection ratio. Obviously, there are real-world limitations, which will be discussed later.

Several additions had to be made to this basic amplifier architecture to allow it to meet the performance demands of the HP E1413. The first is a viable means of accurate, high-speed range switching. Simply using several series FET switches to switch in various values of R_g is not workable. The lowest value of R_g used in the HP E1413 is 55 ohms. Any series FET used to switch this resistor in and out of the circuit would have to have an on resistance of much less than one ohm to meet gain accuracy and stability requirements. Such a FET would inherently have a large parasitic capacitance of many hundreds of picofarads, which would destroy amplifier stability, bandwidth, and settling time if used in that area of the circuit.

To meet the performance requirements of the HP E1413, an arrangement of current-steering diodes and small geometry FET switches are used to switch the amplifier gain. Fig. 4 shows a simplified form of this circuit involving two gain ranges. Switches S1a, S1b, S2a, and S2b are small-geometry FETs with channel capacitances around 5 pF and on resistance of 50 to 100 ohms. Since these FETs are in series with the very high impedance of the lower current sources, this range of on resistance has a negligible effect on circuit performance.

As an example of the operation of the circuit shown in Fig. 4 assume that S1a and S1b are on, and S2a and S2b are off. There is then a current path through CR1a and CR1b, enabling R_{g1} to control the gain. R_{g2} is effectively isolated by the back-to-back diodes CR2a and CR2b and the off switches S2a and S2b. CR1a and CR1b operate at constant current, as do Q_1 and Q_2, so that diode nonlinearities have no effect. It is important that the diodes track with temperature since the amplifier input offset voltage is a direct function of the difference between the forward voltage drops of the on diodes.

This gain switching arrangement provides the high switching speed, good settling, and gain stability required for the HP

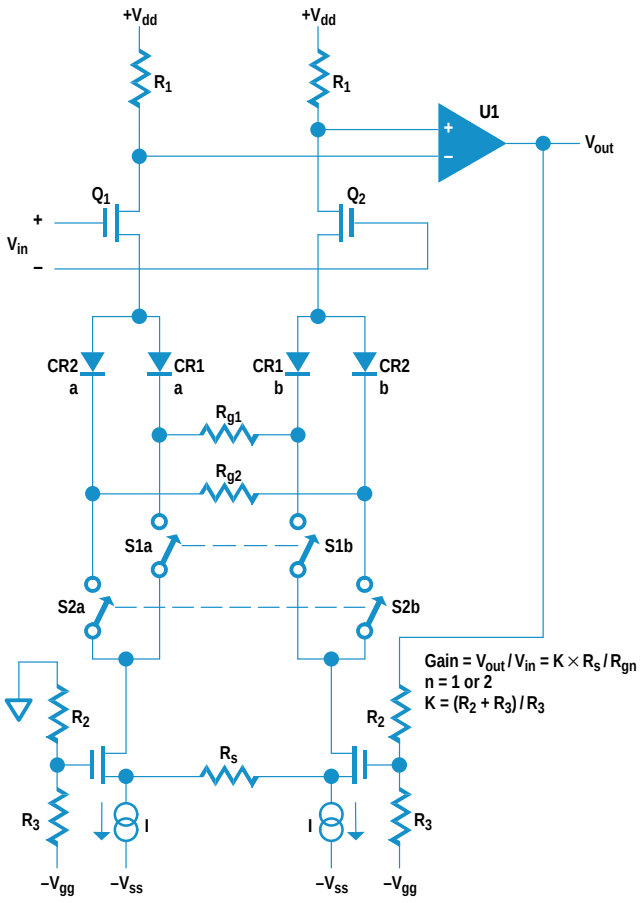

Fig. 4. Basic (2-range) range switching scheme for the current-mode instrumentation amplifier.

E1413. It also allows us to meet our goal of autoranging at the full 100-kHz scanning speed without compromising accuracy.

For an amplifier to recover rapidly and gracefully from an input overload, it is important that the internal biasing be upset as little as possible when such overloads occur. In the HP E1413, this is accomplished by a special set of clamp circuits that do more than simply limit the input or output voltages. During an overload condition, bias current is simply routed around the gain section instead of through it. This has the effect of reducing the gain to whatever value is necessary to keep the output in the linear region. At the same time, the lower current sources and the output opamp see no change in operating conditions compared to a normal input. Thus, these critical parts of the amplifier are not upset during an overload and recovery is rapid and uneventful (see Fig. 5).

Buffering of the input FETs from common-mode voltage changes is important to achieve the desired high-level common-mode rejection ratio. In the circuit shown in Fig. 3 these FETs will see the entire common-mode voltage as a change in their V_{ds}. Unless the FETs are perfectly matched (an impossibility), this will result in a change of input offset voltage, which will in turn translate into a small differential input signal as the result of the changing common-mode signal.

To prevent this, a cascode arrangement is used (see Fig. 6). The combination of current sources Q_3 and Q_4, along with

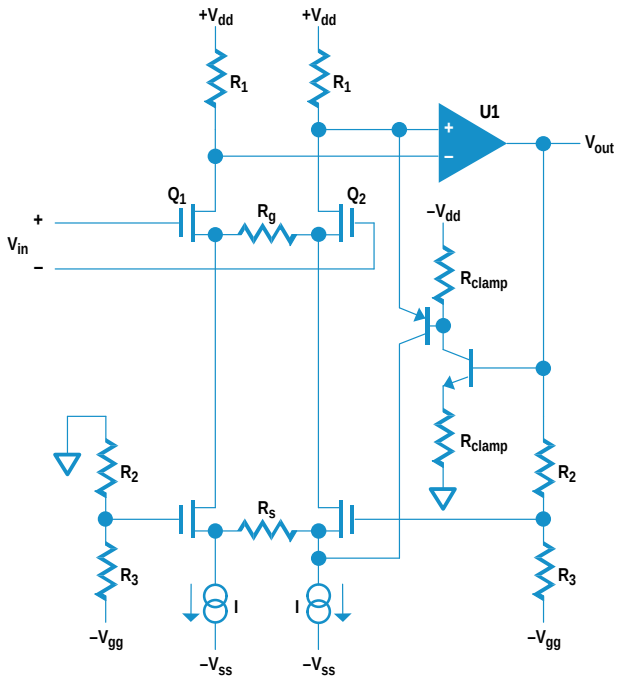

Fig. 5. Amplifier overload clamping technique (only positive clamp is shown).

bipolar pair Q_5 and Q_6, provide a stable, fixed V_{ds} for input FETs Q_1 and Q_2 regardless of the common-mode voltage. Thus, since Q_1 and Q_2 are isolated from common-mode inputs, their offset does not change, and the common-mode rejection ratio remains very high.

The result of all of this careful and sometimes subtle design work is an amplifier that occupies about 2.5 in^2 of printed circuit board area, draws about 300 mW of power, and

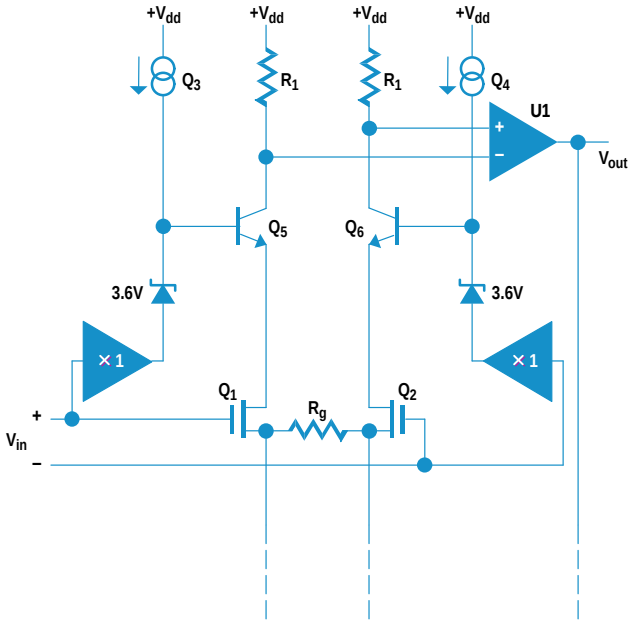

Fig. 6. Upper FET bias scheme for high common-mode rejection ratio.

meets or nearly meets all of the performance criteria outlined above. It is this sort of meticulous design that makes the HP E1413 not just another plug-in ADC card, but a dependable, accurate, information gathering system free from pitfalls and hidden problems for the user.

Calibration, Pipelining, and Timing

On-the-fly gain and offset correction, which is done in hardware in the analog domain, is an important feature of the HP E1413. It may seem old-fashioned to use analog hardware for this purpose in today's world of high-speed number-crunching, but there are some advantages. First, it relieves the downstream digital processing hardware of this task, freeing system resources for more complex tasks such as sensor linearization, engineering unit conversions, and so on.

Secondly, it is useful to recognize that the most fundamental limit on system resolution and dynamic range is the 16-bit analog-to-digital conversion process. Any uncorrected gain and offset errors that occur before the ADC subtract directly from this dynamic range. For example, assume we were doing digital gain correction after the ADC and the uncorrected gain was high by 5%. If a customer tried to measure a 15.9-volt signal in this case the result would be an overrange because 15.9 volts times 1.05 = 16.69 volts, which is above the ADC input range of 16 volts. In fact, for this example, the maximum input voltage that can be measured is only 15.24 volts. This is confusing and frustrating for a customer who presumably ordered and expected to get a 16-volt ADC. Even more confusing, a second unit, presumably identical, might have an uncorrected gain error of 5% low. This unit would then measure up to 16.84 volts before showing an overload.

This kind of customer confusion and uncertainty is unacceptable for high-quality instrumentation. The customer should not have to think about such issues. Analog correction ahead of the ADC process eliminates these issues.

Thirdly, analog offset correction allows us to remove large fixed sensor offsets at the amplifier front end, using the TARE:CAL function. This function allows the customer who is only interested in monitoring changes in sensor output rather than absolute value to increase measurement resolution. This is particularly useful with sensors such as strain gauges. Tare calibration is described in more detail in the article on page 25.

Fig. 1 shows the blocks belonging to the gain and offset calibration subsystem. A local RAM stores a separate 12-bit gain correction constant for each of the five amplifier ranges and each of the 64 channels (64 × 5 = 320 gain calibration constants in all). The RAM also stores two offset correction constants for each range and channel (an 8-bit coarse constant and a 12-bit fine constant). This allows us to correct gain errors of up to ±5% and offset errors of up to ±25% of full scale. This relatively large amount of correction range makes the calibration system very robust and able to accommodate a wide variety of signal conditioning plug-ons and sensors. All of these calibration constants are derived automatically during the various system autocalibration functions based on a few fundamental calibration factors measured during factory or calibration laboratory calibration.

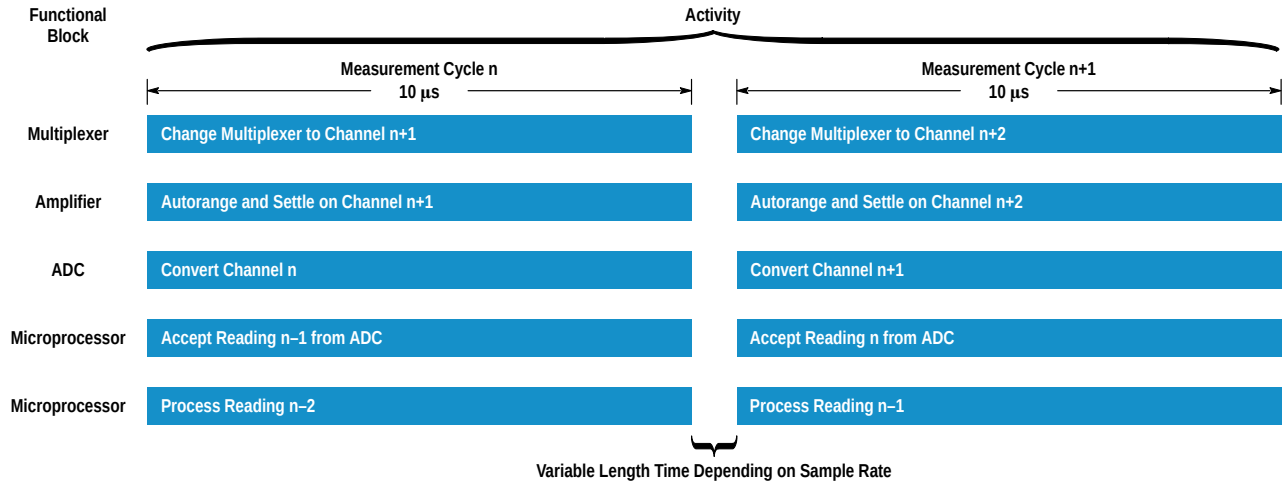

Fig. 7. Timing diagram of an HP 1413 measurement cycle.

Gain and offset correction are interwoven into the measurement cycle such that no speed penalty is incurred. Fig. 7 shows a simplified timing diagram of a typical HP E1413 measurement cycle. An overlapped, or pipelined approach is used so that several operations happen at once.

For example, assume a channel list of eight channels numbered 1 through 8. If at some point during the scan we were to take a snapshot of activity in the HP E1413, we might see the following operations happening simultaneously during a single 10 µs period.

- The multiplexer has switched to channel 6, and the amplifier is autoranging, settling, and applying gain and offset corrections to that channel.
- The sample and hold circuit in the ADC has acquired channel 5, and the ADC is converting this channel to a 16-bit digital word, which will be temporarily stored in the ADC.
- The digital value of channel 4, which has been stored in the ADC since the last measurement cycle, is being transferred to the onboard microprocessor for further processing.
- The onboard microprocessor is processing the reading from channel 3 and transmitting it to the onboard FIFO and current value table* for access by the host computer.

During the next 10-µs measurement cycle, the multiplexer will switch to channel 7 and all other activity will move up one step in the pipeline. This pipelining approach allows the HP E1413 to maintain system throughput at 100,000 readings per second, even though the required operations for a single reading take much longer than 10 µs.

* A current value table is an area of RAM that is accessible to the onboard microprocessor and the host computer. This table stores the most recent reading (current value) for each channel. For monitoring purposes a customer can directly access the most recent readings on any channel without having to sort through possibly hundreds or thousands of readings in the FIFO buffer.

Fortunately, the customer sees none of this complexity. The task of keeping track of all readings and indexing them properly to each channel is taken care of by the onboard microprocessor. This microprocessor also ensures that the pipeline is properly flushed at the beginning and the end of a scan so that no stale readings are transmitted at the beginning of a scan and no good readings are left stranded at a scan's end.

On the HP E1413, a Xilinx FPGA (field-programmable grid array) handles all sequencing and timing of the ADC and amplifier section, including:

- Multiplexer update and channel advance
- Autorange detection and timing
- Calibration RAM interface
- Digital-to-analog converter updates for gain and offset correction
- Start pulse to the ADC.

Using an FPGA for this purpose gave us great flexibility in the design process and reduced the number of required printed circuit board patches and turn-arounds during the prototype phase of the project.

Acknowledgments

Several people deserve thanks for their key roles in this project. They include Don Miller, former section manager, out of whose vision came the whole HP HD2000 effort, Von Campbell, project manager, for his capable management of this project and for keeping us all on track and on schedule, Bert Kolts, test engineer, Vic Anderson, support technician par excellence, and Barb Haas and Anita Helme, who made sure all the parts arrived to build the prototypes on schedule.