Automation of Electrical Overstress Characterization for Semiconductor Devices

An automatic test system has been developed to characterize semiconductor devices and interconnect failures caused by electrical overstress (EOS). Electrical stress in the form of current pulses of increasing amplitude is applied to a device until it reaches a prespecified failure criterion. The system was developed for monitoring EOS robustness in advanced CMOS processes.

by Carlos H. Diaz

Semiconductor devices have a limited ability to withstand electrical overstress (EOS). Device susceptibility to EOS increases as the device is scaled down to submicrometer feature sizes. At present, EOS is one of the major causes of IC failures.[1,2,3] EOS embodies a broad category of electrical threats to semiconductor devices, including electromagnetic pulses (EMP), electrostatic discharge (ESD), system transients, and lightning. However, common use of the terminology puts ESD in a separate category so that EOS means electrical overstress other than ESD. We will follow this convention in this article.

Electrostatic discharge occurs whenever a charged object is grounded, resulting in the release and equalization of the static charge. ESD events are generally in the submicrosecond domain. They may occur any time an IC chip is touched by human hands, held with metal tweezers, or contacted by a grounded metal object such as when the devices slide down plastic tubes in a test engineering environment and an IC's corner pins come into contact with the grounded metal rails.

EOS events, on the other hand, may last several microseconds or even milliseconds and are commonly associated with overvoltage and transient spikes under IC test conditions or in IC applications such as in system boards.

At the chip level, ESD damage can cause increased leakage at the I/O pins, increased standby current, or in extreme cases, full circuit failure. Failures can occur at the board and system levels as well. IC pin failures can range from very small melted filaments at the junctions to gross damage at the pin site.

The physical effects of ESD and EOS on ICs can be categorized as thermally induced or electric field induced failures. Among the thermally induced failure mechanisms are drain junction damage with melted filaments, polysilicon gate filaments, contact metal burnout, and fused metallization. Typical field induced ESD-related failure mechanisms are dielectric breakdown (gate oxide rupture) and latent hot-carrier damage.

Usually, the damage signature indicates whether a failure was ESD-related or EOS-related. In general, ESD-related damage is associated with small failure sites—for example, oxide pinholes, polysilicon filaments, or junction deformation occurring preferentially at diffusion corners.

EOS damage, on the other hand, can be quite drastic and cover most of the area around the pin. This kind of damage is commonly caused by long-lasting (>1 μs) conditions for which the device failure (generally associated with thermal runaway) happens early during the stress event. Thus, what was probably a small failure site just after the onset of thermal runaway invariably grows in size as a result of the additional energy delivered to the structure during the rest of the stress event.

Regardless of whether stress events are ESD-related or EOS-related, the failure sites are in general confined to the protection circuits. However, for certain types of ESD and EOS events, the protection devices or the coordination among the protection structures within an IC may prove to be ineffective, in which case failure sites will also be found in the internal circuitry.

ESD Test Methods

Currently, the most commonly used models for describing various categories of ESD pulses that affect ICs during handling are the human body model, the machine model, and the charged-device model.[4,5,6] The basic model for ESD protection is the human body model (HBM), intended to represent the ESD caused by human handling of ICs. The HBM equivalent circuit is shown in Fig. 1a. The 100-pF capacitor is charged with a high-voltage supply and then discharged through a 1.5-kilohm resistor onto the pin under test. ESD-HBM is the most widely used method of qualifying the ESD performance of on-chip protection circuits and is standardized.[4] Typically, HBM events occur at 2 to 4 kilovolts in the field, so protection levels in this range are necessary.

Contact with machines is also an ESD-type stress event. The ESD machine model (MM) is intended to model the ESD

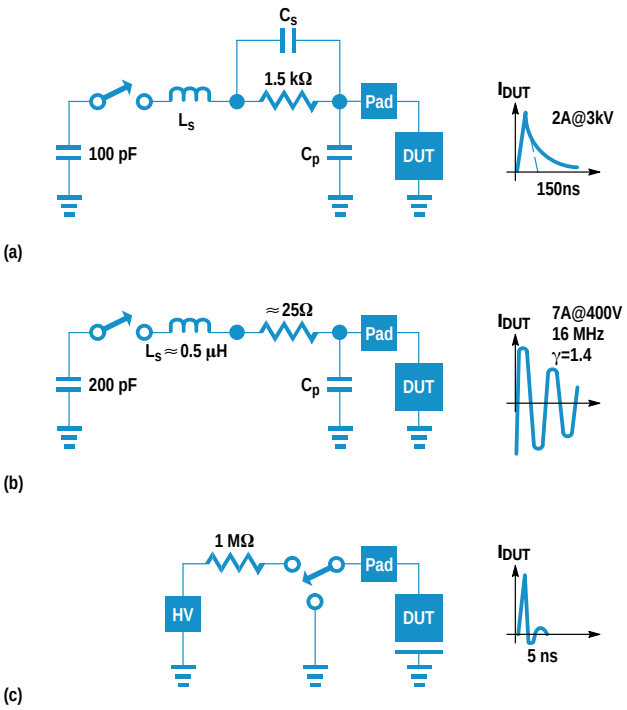

Fig. 1. Equivalent circuits of electrostatic discharge (ESD) models. (a) Human body model (ESD-HBM). (b) Machine model (ESD-MM). (c) Charged-device model (ESD-CDM).

produced by a charged object making contact with ICs during device bonding, assembly, or testing. ESD-MM testers deliver damped, oscillating, 16-MHz stress currents (first peak value in the order of 7A when the 200-pF capacitor is precharged to 400V) to the device under test.[5] A schematic representation of an ESD-MM stress tester is shown in Fig. 1b. In contrast to the ESD-HBM test method, there is no unique definition of the ESD-MM method.

The ESD charged-device model (CDM) (Fig. 1c) is intended to model the discharge of a packaged IC. Charges can be placed on an IC either during the assembly process or on the shipping tubes.[6] ESD-CDM testers electrically charge the device under test (DUT) and then discharge it to ground, thus providing a high-current, short-duration (5-ns) pulse to the device under test. As in the ESD-MM case, there is no industry agreement on the ESD-CDM test method specifications.

EOS Test

The EOS test is more complicated because of the wide spectrum of electrical characteristics of the stress events to which an IC may be subjected in its lifetime.[7] Currently, there exist no EOS standards or quantitative EOS design objectives, thus limiting or delaying the designer's attention to the EOS problem. Constant-current pulses are commonly used for EOS testing.[2,7,8] Such EOS stressing is easy to generate consistently and is also amenable to simple analysis. For thermally induced failures, failure thresholds for any stress waveform can, in principle, be obtained from the failure threshold derived under pulse-stress conditions and given in terms of the relationship of current-to-failure I_f and time-to-failure t_f. For example, constant-current pulses lasting 100 to 250 ns are used to study second-breakdown phenomena in NMOS devices. The failure current levels measured using these short pulses are treated as predictors of the HBM-ESD failure thresholds.[8]

NMOS Transistor

The most commonly investigated and well-understood ESD phenomenon is the ESD behavior of an NMOS transistor. Consider the operation of an NMOS device under high-current conditions. The basic I-V characteristics are shown in Fig. 2 for the gate and substrate tied to ground. Here V_{t1} is the drain junction breakdown voltage. Holes from the drain impact ionization process are injected into the substrate, increasing the substrate potential near the source junction. When enough hole injection is present, the source junction becomes forward-biased and the parasitic n-p-n bipolar transistor enters active mode and causes the snapback phenomenon. During an ESD or EOS event, the device operates primarily in the snapback mode. The device terminal voltage is determined by the snapback voltage V_{sp}, the contact resistances, and the level of device self-heating. At high stress levels, the device could go into second breakdown, the region where the device temperature has increased to such a level that thermal carrier generation is high enough to dominate the conduction process. Second breakdown is a positive feedback process that causes device failure because of current localization. The current level at which the device undergoes second breakdown (I_{t2}) is used as a predictor of the device's current-handling capabilities under ESD events.

The test system introduced here is designed to determine this kind of transient I-V characteristic for devices at both the wafer and package levels. It is an EOS tester, that is, it applies constant-current pulses to the DUT. The ESD performance of the DUT is inferred from the EOS test results. The advantage of this approach is that the EOS test can be applied at the wafer level while direct ESD tests cannot be applied at the wafer level.

Test System Description

In the EOS test system, stress current pulses are generated using a high-power pulse generator or a transmission line system. The HP-IB-programmable HP 8114A pulse generator is used to deliver current pulses of up to 1A amplitude and 50-ns-to-1-s pulse width. For submicrosecond pulses higher than 1A, a coaxial cable charged to a high voltage is used as the stress source.[9] The length of the coaxial cable determines the pulse width at the device under test. To avoid reflections, the line is terminated by a 50-ohm resistor at the near end.

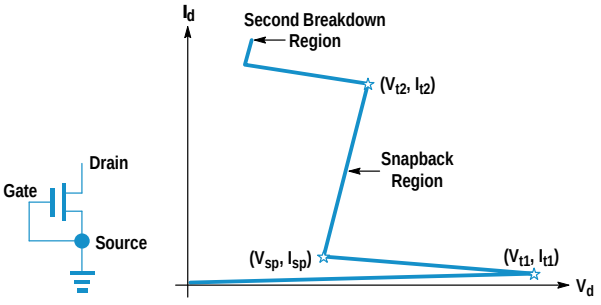

Fig. 2. Schematic I-V characteristics of a grounded-gate NMOS transistor.

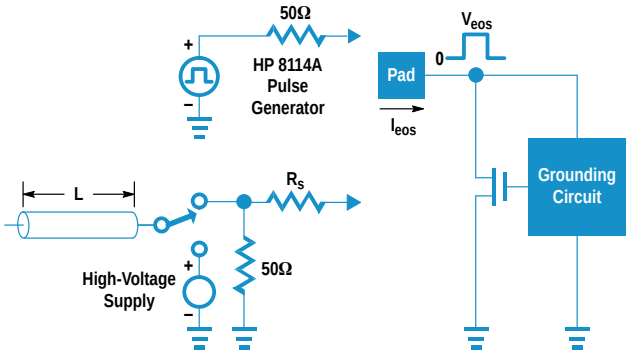

Fig. 3. Basic stress source configuration. The source is an HP 8114A pulse generator for current pulses up to 2A and a coaxial cable charged to a high voltage for pulses greater than 2A.

Additionally, to eliminate the effects of DUT impedance variations and to increase stability in the negative differential region, a 100-to-500-ohm series resistance is used. The basic stress setup is shown in Fig. 3.

Fig. 4 is a schematic of the automated test system. The main components are the stress sources described above, a real-time high-speed digital storage oscilloscope (HP 54720A), a semiconductor parameter analyzer (HP 4142A), a switch matrix control unit (HP 75000 VXI mainframe with a Form-C switch board), and a workstation running the HP IC-CAP circuit and device modeling software package.

New IC-CAP instrument drivers, written in C++ using the IC-CAP open measurement interface, were developed for the HP 8114A pulse generator, the Bertan 225 high-voltage power supply, and the HP 54720A digital oscilloscope. The HP 75000 VXI mainframe and its switch board cannot be made IC-CAP instruments because of their special addressing protocol. To overcome this limitation, C routines were written to perform basic interface and control functions. These C routines are available to the instrument drivers, and are also available as command line functions. Fig. 5 illustrates the IC-CAP instrument option tables for these instruments. These tables provide the user with some of the most frequently used instrument features. For example, the user can choose either real-time or equivalent time acquisition mode and the sampling rate of the HP 54720A. For the HP 8114A pulse generator, the pulse count, trigger mode, output impedance, and other features can be specified. The option tables for the pulse generator and the high-voltage power supply contain fields that specify the base addresses of the switches that isolate the source from the test system (if the system is configured without the VXI mainframe, these instruments can still be used by setting the primary address of the switch fields to an illegal value such as 32).

Fig. 6 shows the IC-CAP window for a typical pulse stress measurement. Once the IC-CAP model variables for the pulse amplitude and width and the time-sweep window are defined, the execution of the measurement command on the IC-CAP pull-down menu causes the device to be stressed and the corresponding current and voltage waveforms to be recorded. Fig. 7 shows such waveforms for a low-voltage silicon controlled rectifier used as on-chip ESD protection in a submicrometer CMOS process. After stressing, the user can

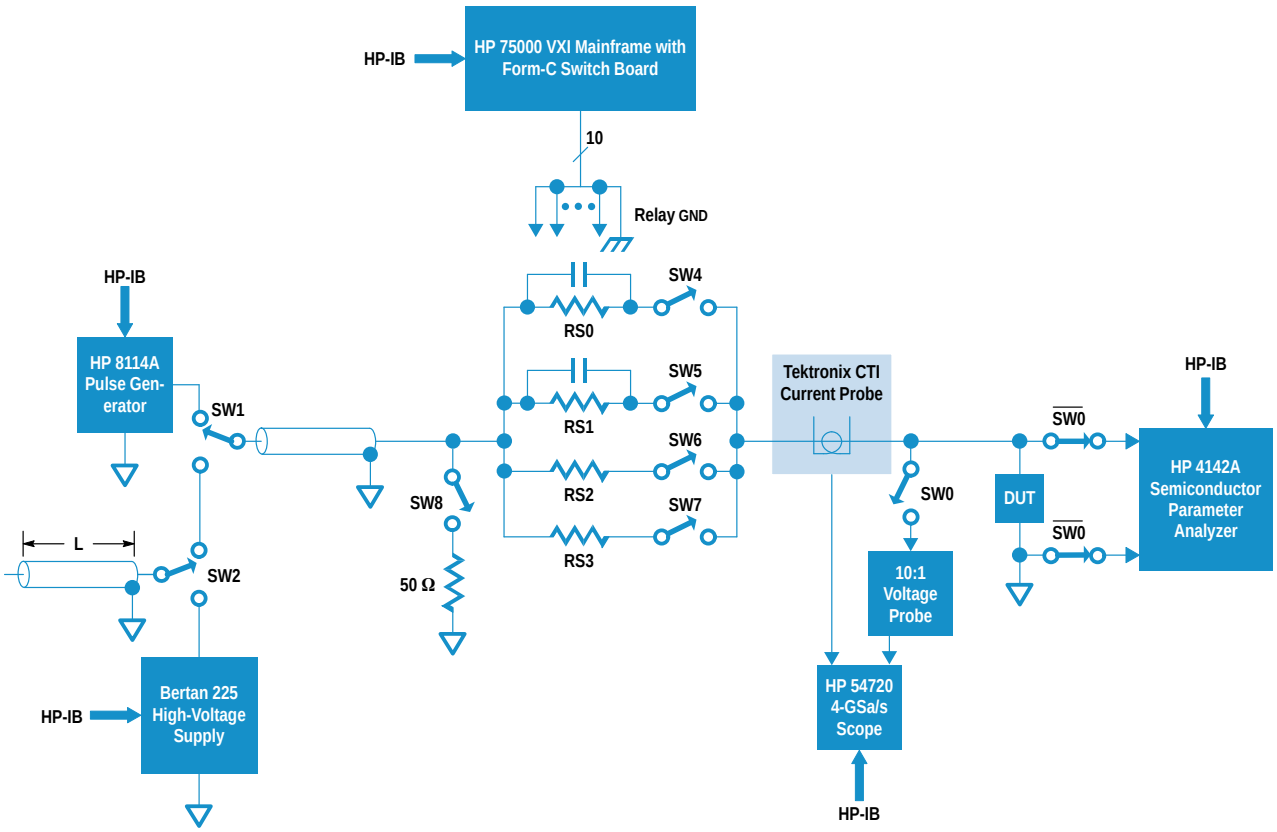

Fig. 4. Schematic diagram of the IC-CAP-based EOS test system.

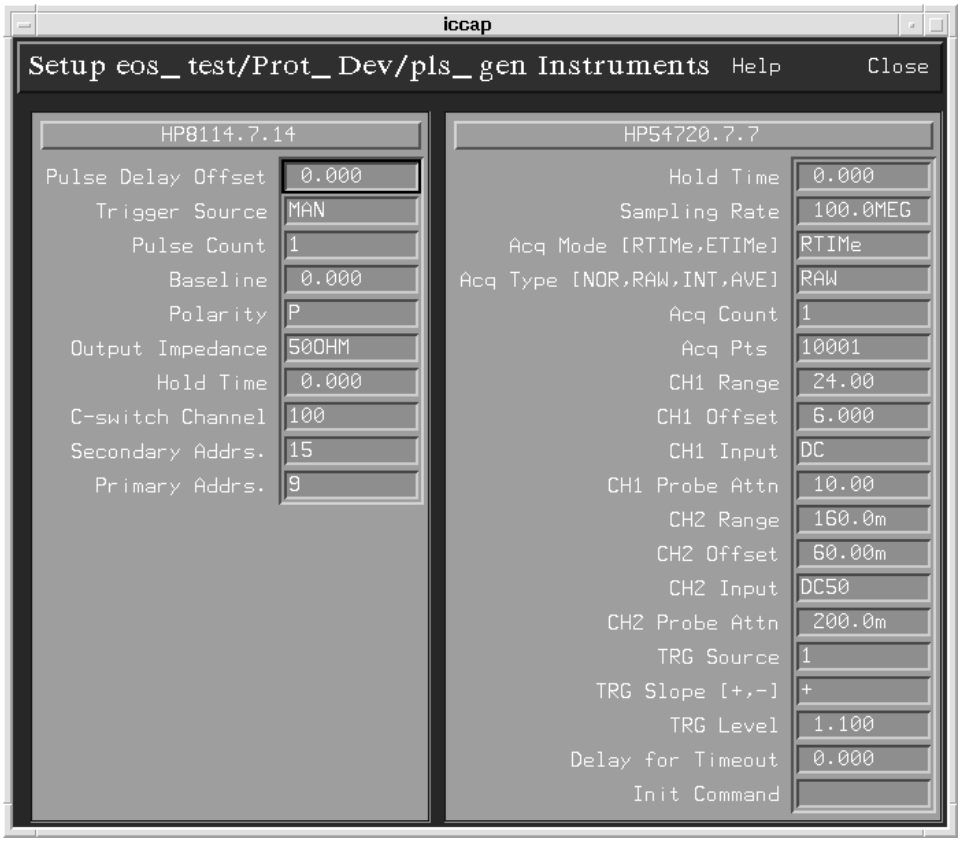

Fig. 5. IC-CAP instrument option tables for the pulse generator and oscilloscope.

perform HP 4142A measurements and compare the results with prestress data to determine if the device has been degraded by the stress event. Test automation to evaluate device failure thresholds is then a simple task of interleaving stress and device parameter measurements in a repetitive fashion.

Test programs are written as IC-CAP macros for characterization of second-breakdown phenomena in semiconductor devices and for pulsed electromigration of interconnect lines in IC processes. Another test macro was written to measure time-dependent dielectric breakdown (TDDB) for CMOS

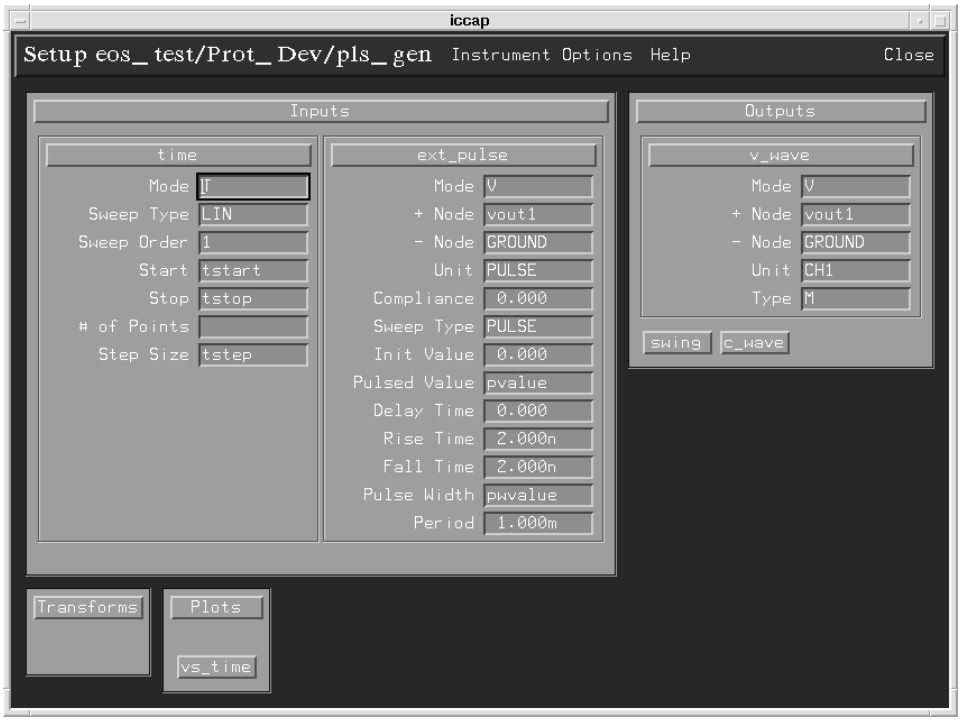

Fig. 6. IC-CAP window for a typical pulse stress measurement.

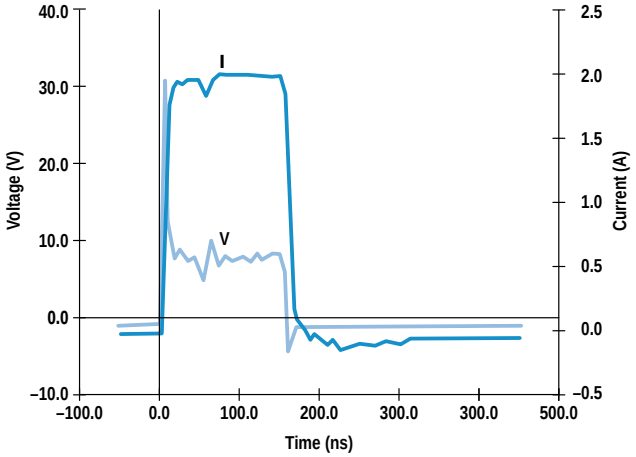

Fig. 7. Current and voltage waveforms recorded in a stress test of a low-voltage silicon controlled rectifier used as on-chip ESD protection in a CMOS process.

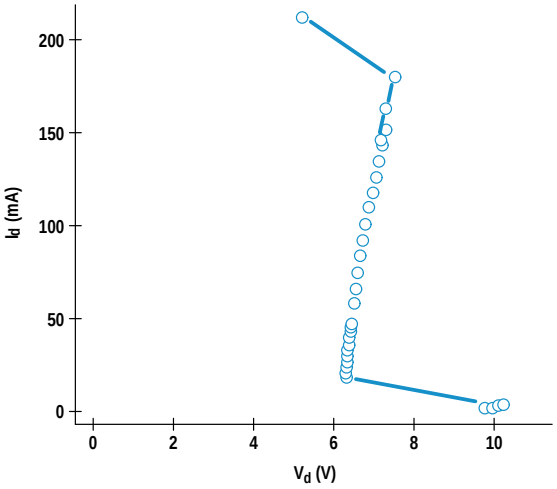

Fig. 9. Pulsed I-V characteristics of a submicrometer NMOS transistor.

gate oxides. These IC-CAP macros determine the test conditions and DUT information, coordinate the stress and measurement sequences, and generate the test reports. A typical report generated by a test macro for a particular batch is shown in Fig. 8. Each line in the device data is the result of a measurement taken after delivering a single pulse to the device and subsequent measurement of the device leakage as a failure condition. From this data, the device transient I-V characteristic can be reconstructed. This is shown in Fig. 9 for an NMOS device in a submicrometer technology. Test files containing raw test data, like the one shown in Fig. 8, can be postprocessed and fed into a database and data analysis package such as S-Plus. Device electrothermal model parameters can be extracted in IC-CAP and fed to circuit-level electrothermal simulators such as iETSIM[10] that are capable of modeling device behavior up to the onset of second breakdown.

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08/04/94      11:27:59
Mask:    1th7b
Lot:     yth15
Wafer:   9
Test:    eos
Ioff Spec =        100e−9 @ Vdut =      4 Volts
2ndBV Spec =       −1
Pulse width =      1.5E−07

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Device cgnch8f
Die 84 Reference leakage current If_rel = 4.812E−11
Vdut_pk  Vdut [V]  Idut [A]  I_off [A]
9.78     9.7826    0.0029     1.18E−11
9.79     7.1804    0.016242   8.138E−11
9.9      6.5744    0.027964   7E−13
10.01    2.957     0.045094   5.0856E−08
9.84     6.0052    0.048454   5.0364E−08
9.34     6.034     0.058052   4.8872E−08
9.01     5.986     0.067442   4.8164E−08
9.22     6.0008    0.077012   4.7708E−08
9.89     6.0238    0.13716    4.7164E−08
11.39    6.0264    0.21542    4.633E−08
12.71    2.6006    0.32224    9.9996E−07
Failed ISpec: Idut = 0.21542, Ioff = 9.9996E−07

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Fig. 8. Typical report generated by the test macro for a particular batch of devices under test.

Another IC-CAP test macro was developed to determine the maximum pulsed current density in metal lines for an advanced CMOS process. Fig. 10 presents the results of this characterization for the three-level-metal system as a function of the stress pulse width.

Conclusion

An automated test system has been developed for the pulse characterization of semiconductor devices and interconnect metal lines in MOS processes. The system is built on a test environment based on the HP IC-CAP circuit and device modeling software. Instrument drivers were written for instruments such as the HP 8114A pulse generator, the HP 54720A digital

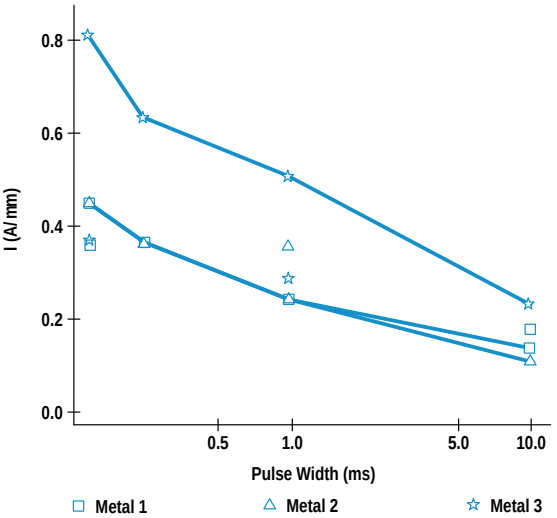

Fig. 10. Pulsed failure current per micrometer width in metal lines for an advanced three-level-metal CMOS process.

storage oscilloscope, and the Bertan 225 high-voltage power supply. The drivers and the IC-CAP environment were supplemented with additional C routines that, at the discretion of the user, enable the IC-CAP open measurement interface to indirectly control a switch matrix in the HP 75000 VXI mainframe system. The test system is currently used by the HP Integrated Circuit Business Division's Technology Development Center as a tool in the development of CMOS processes with built-in EOS/ESD robustness.

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