Vector Error Testing by Automatic Test Equipment

Mixed-signal testers are frequently used as specialized automatic test equipment in various test applications. The real-time digital signal processors in the HP 9493 mixed-signal LSI test system can perform complex tests for next-generation telecommunication devices.

by Koji Karube

In the next generation of wireless communications systems, high-quality telecommunication and compact equipment will be achieved by using new highly integrated, multifunctional, mixed digital and analog devices. Mixed-signal testers like the HP 9493 can test these devices. Many of the newer telecommunication systems use complicated modulation methods such as π/4 DQPSK (differential quadrature phase shift keying), which creates specialized waveforms that are very difficult to analyze. With its built-in digital signal processors (DSPs), the HP 9493 can also be used to solve some of these difficult signal analysis problems.

In general, a mixed-signal LSI tester is not an instrument for measurement but serves as automatic test equipment in the production area. The most important requirement is how quickly failing devices can be rejected from a large number of passing devices. Good repeatability, which is a function of system stability, and usability are also required for high productivity.

Many of the tests performed by mixed-signal testers do not have precise specifications because of the complexity of the device under test. Inside a mixed-signal device are many digital and analog signals, and digital signals may corrupt analog signals and vice versa. As a result, some tests have to be guaranteed statistically or experimentally. The measurement of the vector error, one of the most important test parameters for π/4 DQPSK devices, belongs to this category, so it is not an unfamiliar type of test for a mixed-signal LSI test system like the HP 9493.

We have developed a test application to measure the vector error. The test achieves high throughput and good repeatability.

Roll-off Filter Design

Fig. 1 shows the simplified block diagram of a transmitter baseband device. This device has four signal processing blocks. First, the serial-to-parallel converter converts serial data to two-bit width. The next block encodes the data differentially and maps it into the coordinates of the signal space according to the signal space diagram shown in Fig. 2. The final roll-off filters are a kind of low-pass filter called "root raised-cosine" filters, defined by:

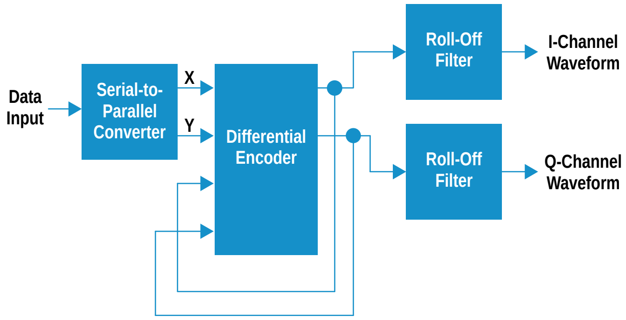
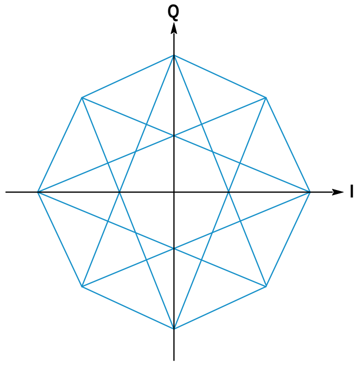


Fig. 1. Baseband transmitter device for π/4 DQPSK modulation.

$$H_\alpha(f) = \begin{cases} 1 & \text{for } 0 < f < \dfrac{1-\alpha}{2T} \\ \sqrt{\dfrac{1-\sin\left[(fT-0.5)\pi/\alpha\right]}{2}} & \text{for } \dfrac{1-\alpha}{2T} \le f \le \dfrac{1+\alpha}{2T} \\ 0 & \text{for } \dfrac{1+\alpha}{2T} < f \end{cases}$$

where f is the frequency in hertz, T is the data symbol period in seconds, and α is the roll-off coefficient.

The π/4 DQPSK receiver also has root raised-cosine filters such that the overall filter characteristic is raised-cosine with an impulse response that results in a state of no intersymbol



X	Y	Rotation
1	1	−3π / 4
0	1	3π / 4
0	0	π / 4
1	0	−π / 4

Fig. 2. Signal space diagram of π/4 DQPSK modulation.

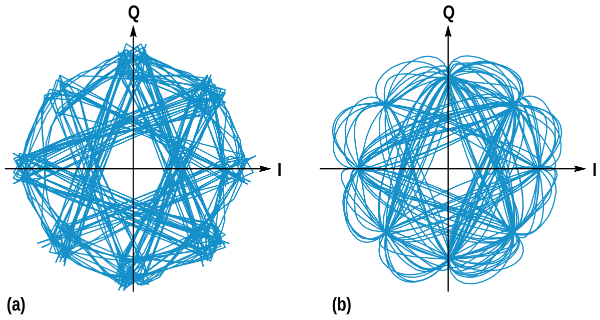


Fig. 3. (a) I-Q signal without filters. (b) I-Q signal with root raised-cosine filters.

interference, as shown Fig. 3b. For this test the receiver filters are emulated in the HP 9493 test system using the digital signal processing capabilities. To obtain the required impulse response, we use 8-symbol-deep FIR (finite impulse response) filters, where 8-symbol-deep means that the duration of the filter impulse response corresponds to eight data symbol times. The design employs virtual oversampling[1] and multirate techniques[1] to achieve high-resolution delay adjustment and high throughput.[2]

Symbol Timing Extraction

The Research and Development Center for Radio Systems in Japan specifies the vector error as follows.[3] The ideal transmitted signal after final filtering is:

$$S(k) = S(k-1)e^{j(\pi/4+B(k)\pi/2)}$$

where B(k) is defined by the following table.

X_k	Y_k	B(k)
0	0	0
0	1	1
1	1	2
1	0	3

The actual transmitted signal after final filtering is:

$$Z(k) = [C_0 + C_1\{S(k) + E(k)\}]W^k$$

where $W = e^{dr+jda}$ for phase offset da (radians/symbol) and amplitude change dr (nepers/symbol)
C_0 = arbitrary complex constant representing the offset of the origin caused by imbalance of the quadrature modulator
C_1 = arbitrary complex constant determined by the phase and power of the transmitter
E(k) = vector error.

Then the sum of the squared vector errors is:

$$\sum_{k=\min}^{\max} |E(k)|^2 = \sum_{k=\min}^{\max} \left|\left\{\left[Z(k)W^{-k} - C_0\right]/C_1\right\} - S(k)\right|^2.$$

System designers attempt to minimize this error by selection of C_0, C_1, and W.

To calculate the vector error, C_0, C_1, and W must be determined. For a baseband transmitter device, the frequency offset described by W is zero because the I and Q signals are observed without quadrature modulation that shifts the signal frequency. The offset of the origin described by C_0 can be obtained easily by statistics. To determine C_1, a method of extracting the phase of the signal (symbol timing) has to be designed. In concrete terms, the function of symbol timing extraction is to find the eight convergence points of the filtered I-Q signal shown in Fig. 3b.

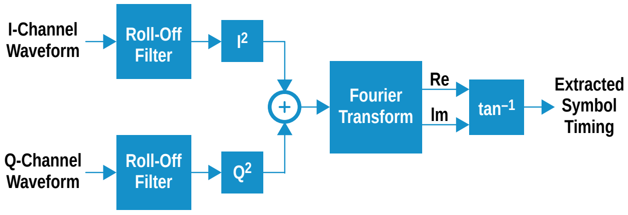


Fig. 4. Conventional method of symbol timing extraction.

The conventional method of extracting symbol timing is envelope detection of the squared signal as shown in Fig. 4. The phase extracted by this method is a little different from the “best phase” because this method observes only a narrow bandwidth around one-half the symbol frequency and ignores the group delay of the actual devices. Fig. 5 shows the timing error for this method of symbol extraction as a function of the calculated vector error, obtained by simulation. According to this figure, timing error must be within 10 ns to achieve repeatability within less than 0.1%. Therefore, instead of the envelope detection method, we adopted a specialized search method that finds the actual minimum vector error.

Implementation

In a π/4 DQPSK receiver, the extracted symbol timing is fed back to the digitizer clock inputs. In the HP 9493, this is simulated by using adjustable-delay filters in front of the signal processing.

Fig. 6 shows the simplified block diagram of the vector error test. The test uses two 16-bit digitizers to digitize the I and Q signals independently and uses two sets of real-time DSPs to process both signals at the same time. Each digitized signal with 16-bit resolution is transferred into the roll-off filters and processed by one of the 8-symbol-deep FIR filters. In effect, there are 512 of these filters, each having a slightly different delay. The delay is selected by feedback from subsequent blocks. Next, gain error and offset are adjusted and then

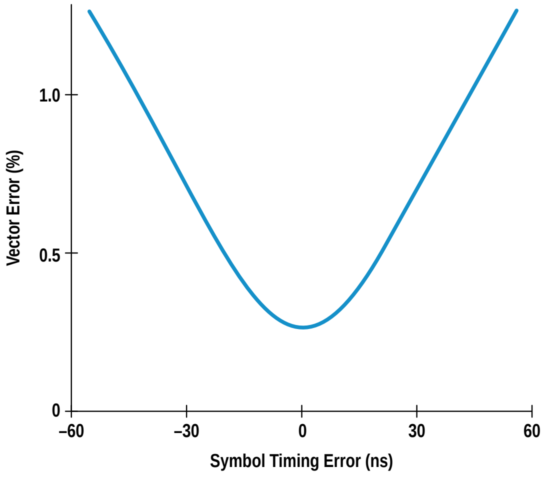


Fig. 5. Symbol timing error as a function of calculated vector error.

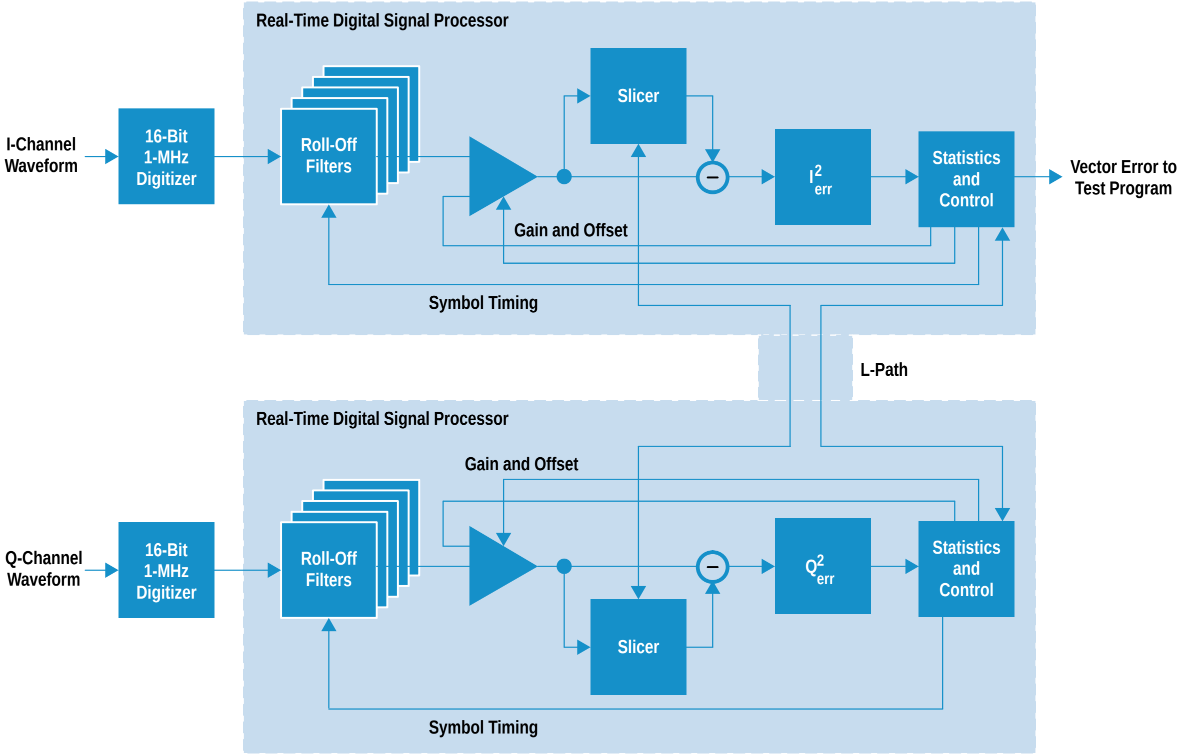


Fig. 6. Block diagram of the HP 9493 vector error test.

squared vector errors are calculated by comparing the actual symbol locations in the I-Q plane with the ideal locations, which are determined by the slicers. The statistics and control block searches for the best symbol timing to minimize the vector error by changing the roll-off filter delay, which changes the symbol timing.

The roll-off filters are designed to have a high virtual conversion frequency of 2048 times the symbol frequency, which corresponds to about 2.5-ns delay resolution in the HP 9493.

Analog Timing Skew

Group delay in the band from zero to the baud rate causes synchronization error. Analog timing skew between digitizers also directly reduces the accuracy of the vector error measurement. In the HP 9493 test system, the effect of timing skew is eliminated by regular calibration, so the user need only make sure that the cable lengths of the I channel and the Q channel are same on the DUT board.

Acknowledgments

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